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Implementation of reconfigurable nth-order filter based on CCII

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Abstract Topologies for realizing voltage and current mode reconfigurable nth-order filters based on the secondgeneration current conveyor (CCII) are assessed. The most compatible structure for field-programmable analog array is identified. A CCII adopting active current division networks are utilized for implementing the proposed filter leading to wide control of its coefficients. Programmability characteristics are demonstrated through experimental results obtained from integrated circuit chips fabricated in a 0.18 µm CMOS process.

Keywords Analog filters · Current mode circuits · Second-generation current conveyor (CCII)

1 Introduction

The transfer function of a general nth-order filter (NOF) response can be expressed as:

$$
T(s) = \frac{N(s)}{D(s)} = \frac{a_n s^n + a_{n-1} s^{n-1} + \dots + a_1 s + a_0}{s^n + b_{n-1} s^{n-1} + \dots + b_1 s + b_0},
$$
(1)

where a_0 through a_n are real numbers, and b_0 through b_{n-1} are positive real numbers. The second-generation current conveyor (CCII) is an essential building block for currentmode (CM) processing. It is one of the most versatile devices [[1\]](#page-5-0). Several NOF based on CCII and its related building blocks are suggested $[2-10]$. A reconfigurable NOF (RNOF) is a versatile filter that can be flexibly used to realize any NOF function without hardware change and hence serves wide range of applications. Such filters are core parts of systems utilizing field-programmable analog array (FPAA) [\[11](#page-5-0)]. This work investigates the use of CCII in the design of RNOF.

Integrated circuit applications require filters to be associated with programmable parameters to adjust the filter frequency response compensating for components, process and temperature variations. The nature of RNOF demands even broader programmability features to accommodate wide range of selectivity requirements. In this regard, NOF filters can be classified based on their TFs coefficients into programmable or not programmable designs. Also, it is important to further classify the programmable filters as those with orthogonally or independently tuned parameters. Independent tuning of the RNOF coefficients allows adjusting one parameter (e.g. accommodating different bandwidths) but also changing the filter type (e.g. low- to bandpass), and modifying the overall response (e.g. Butterworth [BT] to Chebyshev).

Traditional CCII, however, does not exhibit programmability feature obstructing its utilization in integrated VLSI applications involving complete systems on chip. In this work, voltage-mode (VM) and CM structures of RNOF based on CCII are explored. Then, the work addresses possible options for providing tuning characteristics. Section 2 provides summary of the available solutions and identifies those suitable for RNOF designs. The proposed filter is presented in Sect. [3.](#page-2-0) Experimental results obtained from standard 0.18 µm CMOS chips are given in Sect. [4.](#page-2-0)

2 Available solutions

Unlike other techniques such as LC simulation which results in single function with dependent coefficients [\[2](#page-5-0)],

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integrator based filter topologies provide all functions simultaneously with possible independent tuning characteristics. They adopt either distributed inputs (DIs) or summed outputs (SOs) topologies to generate various $N(s)$ terms. In practice, there could be two different circuit realizations these filters based on the availability of the $sⁿ$ function of $N(s)$ from the core circuit. The circuits without $sⁿ$ term are often canonic in the sense that *n* devices are required to realize the *n* integrators. In such cases, s^n is often obtained through subtracting various outputs from the input signal results in a TF with several matching conditions for realizing the $sⁿ$ function. Table 1 summarizes the different characteristics of the available filters [[3–10\]](#page-5-0).

The filter presented in [[3,](#page-5-0) [4\]](#page-5-0) uses $3n - 2$ CCII to realize a VM filter topology while the filter in [\[5](#page-5-0)] employs $n + 2$ current differencing buffered amplifier (CDBA) to construct CM filter topology. A CDBA is realized using two current-feedback amplifiers (CFAs). On the other hand, a CM NOF was presented in [[6\]](#page-5-0) incorporating $3n + 2$ electronically programmable CCII (ECCII). The filter in [[7\]](#page-5-0) employs $n - 1$ current controlled CCII (CCCII) with one output and a CCCII with $n + 1$ outputs whereas the filter of [[8\]](#page-5-0) incorporates $n - 1$ differential difference current conveyor (DDCC) and a fully differential CCII (FDCCII). The filters in [[9\]](#page-5-0) employs only $n - 1$ differential voltage current conveyor (DVCC) with one output and a DVCC with $n + 1$ output to provide the feedback paths. It requires $n + 1$ copies of the input current. Circuit required to generate copies of input current for the filter of [\[9](#page-5-0)] is not counted. On the other hand, filters in [\[10](#page-5-0)] use $2n + 1$ CCIIs with single output and one CCII with $n + 1$ outputs. In addition, realizations of the core NOF based on several different active elements are also suggested. The VM filter in $[12]$ $[12]$ adopts the CFA. The CM filter in $[13]$ is based on dual-output CCCII. The log-domain VM filters of [\[14](#page-5-0), [15\]](#page-5-0) and square root domain filter of [\[16](#page-5-0)].

It can be seen that the filter topologies in $[7-10]$ are incompatible. They lead to transfer functions wherein the coefficients of N(s) cannot be independently controlled.

Also, the filters of [\[7](#page-5-0), [8\]](#page-5-0) have another drawback as they do not provide s^n term function. Although the filters in [[3–6\]](#page-5-0) are less efficient in terms of number of devices they are attractive as they are associated with transfer functions of independent coefficients. The filters [\[3–5](#page-5-0)] lack the programmability feature because traditional CCII does not exhibit programmability feature. The filter of [\[5](#page-5-0)] has another problem as it adopts $2n + 4$ CFAs. A CFA consists of a CCII followed by a voltage buffer (VB). Given that CCII is often realized with a VB and a current mirror, it can be seen that the filter topology of [\[5](#page-5-0)] would approximately employ $4n + 8$ CCIIs and hence less efficient than its counterpart of [\[4](#page-5-0)].

It is possible to change active-RC filters based on the CCII in [\[4](#page-5-0)] to their active-C counterparts utilizing translinear current conveyors such as [[17\]](#page-5-0). In this case, the passive resistors would be replaced by the internal resistance of the X terminals (r_x) of the conveyor. It can be shown that NOF filter developed based on CCCII would exhibit dependent coefficients of $N(s)$ and $D(s)$. A CCII with both voltage and current gain called VCG-CCII was suggested in [\[18](#page-5-0), [19\]](#page-5-0). The voltage gain V_r/V_v , just like any voltage amplifier, suffers from gain-bandwidth product problems. Whereas the current gain I_1/I_x is proportional to the small signal transconductance $[18]$ $[18]$ or output resistance [\[19](#page-5-0)] of current mirroring transistors. The bandwidths of the current transfer characteristics of the VCG-CCII of [\[18,](#page-5-0) [19\]](#page-5-0) are limited to approximately 20 kHz and 1 MHz, respectively. Alternatively, a current amplifier (CA) can be injected in the design of CCII to form ECCII such as [[6\]](#page-5-0). In these topologies, the output current of CCII (I_x) is sensed and then applied to the input of a small signal CA. The CA amplifies I_x and makes it available from a high output terminal Z. However, the main problem with ECCII of [[6\]](#page-5-0) and the ECCII of [\[17–19](#page-5-0)] is that their operations are valid only for small signal processing, resulting in limited tuning range and linearity performance.

Replacing the $3n - 2$ CCIIs in [\[4](#page-5-0)] by ECCIIs would lead to a filter design with independently programmable

Table 1 Summary of NOF using CCII

Works	sn term	Methods	Independent coefficients	Tunable
$[4]$	Yes.	DI using $3n - 2$ CCIIs	Yes	No.
$\lceil 5 \rceil$	Yes.	DI using $n + 2$ CDBAs = $2n + 4$ CFAs = $2n + 4$ CCII plus $2n + 4$ VBs	Yes	No.
$\lceil 6 \rceil$	Yes.	SO using $3n + 2$ ECCIIs	Yes	Yes
$\lceil 7 \rceil$	No	DI using $n - 1$ CCCII plus 1 CCCII with $n + 1$ outputs	No.	No.
$\lceil 8 \rceil$	No	DI using $n - 1$ DDCC = $2n - 2$ CCII plus 1 FDCCII = 2 CCII	N _o	N ₀
$\lceil 9 \rceil$	Yes.	DI using $n - 1$ DVCCII plus 1 DVCCII with $n + 1$ outputs	N ₀	N ₀
$\lceil 10 \rceil$	Yes.	SO using $2n + 1$ CCII plus 1 CCII with $n + 1$ outputs	N ₀	N ₀
	Yes.	SO using $2n + 1$ CCII plus 1 CCII with $n + 1$ outputs	N ₀	N ₀

characteristics. This filter would employ $3n - 2$ CCIIs and -CAs which are less by four CCIIs and four CAs compared with its filter counterpart of [[6\]](#page-5-0). Therefore, it can be seen that this modified filter of $[4]$ $[4]$ and the filter of $[6]$ $[6]$ would be suitable for the design of RNOFs. However, they suffer from three main drawbacks: (1) the large number of active devices, (2) the large number of resistors $3n - 2$ in [[4\]](#page-5-0) and $3n + 3$ in [[6\]](#page-5-0), and (3) the limited tuning range provided by ECCII which is contrary to the wide tuning range requirement of FPAA.

The third problem can be resolved through adopting digitally programmable CCIIs. A digitally programmable CCII was presented in [[20\]](#page-5-0) using several cascaded current division cells. Each cell (one-bit) consists of seven transistors and consumes $150 \mu A$ leading to area and power inefficient solution. Another digitally programmable CCII utilizing the active current division network (CDN) of [[21\]](#page-5-0) was suggested in [[22\]](#page-5-0). It utilizes two CCII and a CDN to form a digitally programmable CCII. This conveyor has a single output and hence it could be used in the design of the filters of $[4]$ $[4]$ or $[6]$ $[6]$. In fact, the work in $[22]$ $[22]$ used the topology of [[6\]](#page-5-0) to realize filters for FPAA.

3 The proposed design

The filter proposed in this work will be shown to employ considerably less number of active devices and passive resistors compared with [[3,](#page-5-0) [4,](#page-5-0) [6](#page-5-0), [22](#page-5-0)]. This would result in significant improvements in power consumption and area. Also, it will be shown that the proposed filter further extends the tuning range without increase in power consumption. These advantages are achieved first by adopting a better filter topology and consequently utilizing an improved digitally programmable current conveyor.

The terminal characteristics of a CCII can be described as follows: $I_y = 0$, $V_x = V_y$ and $I_z = \pm I_x$ where the positive and negative signs denote CCII+ $(I_x$ and I_z have same direction) and CCII-, respectively. The following points should be observed in order to realize filters with independent coefficients. First, it can be seen that distributing the inputs or summing desired outputs using active elements with programmable gains a_0 through a_n inherently result in filters with independent coefficients of $N(s)$. Second, it can be seen that these topologies result in independent tuning of $D(s)$ coefficients if programmable active elements are used to realize the feedback factors (b_0) through b_{n-1}). With the help of the filter of [\[6](#page-5-0)], VM and CM RNOFs based on CCII can be developed. A mixedmode filter (input and output signals can be voltage or current) is shown in Fig. [1.](#page-3-0) It employs $3n + 2$ CCIIs for CM processing while two additional CCIIs are needed for VM signals.

Alternatively, dual- or multi-output CM active devices are often utilized to reduce the number of active elements. A single CCII can be utilized to efficiently develop the integrator such that the feedback factor and output signals can be realized using the same device as shown in Fig. [2.](#page-3-0) This topology is adopted for CM signals since it is more efficient. A similar topology based on OTAs was suggested in [[23\]](#page-5-0).

The remaining issue in the design of Fig. [2](#page-3-0) is introducing the tuning feature to permit adjusting the filter coefficients. Here, it is proposed to utilize the digitally programmable CCII suggested in [[24\]](#page-5-0) instead of its counterpart of [[22\]](#page-5-0). The conveyor of [[24\]](#page-5-0) is formed of a CCII, CDNs, and digitally controlled current followers (DCCFs) as shown in Fig. [3](#page-3-0). This solution provides double the tuning range and better tuning resolution compare to its counterpart of [\[22](#page-5-0)] without additional power consumption and hence it is more attractive for FPAA. The switches involved in the design of the CDN and DCCF are original parts of these devices and hence do not contribute nonlinearity. The DCCF is used to provide current gain (α) , whereas the CDN is utilized to provide attenuation (β) . In filter design, current gains can scale up the frequency characteristics, whereas attenuations can be used for frequency scale down. The tuning range of b_i and a_i would be equal to the product $\beta \alpha$ comprising $2^{16} \approx 65,500$ steps with resolution of 0.0039 and hence it combines both the wide tuning range of digital elements and continuous programmability feature of analog tuning.

The transfer functions of the proposed filter can be expressed as:

$$
\frac{i_m(s)}{i_s(s)} = \frac{s^m \beta_{am} \alpha_{am} \prod_{i=m}^{n-1} \frac{1}{C_{i+1} R_i}}{s^n + \sum_{i=0}^{n-1} \beta_{bi} \alpha_{bi} s^i \prod_{j=i}^{n-1} \frac{1}{C_{j+1} R_j}}
$$
(2a)
for $m = 0$ to $n - 1$,

$$
\frac{i_n(s)}{i_s(s)} = \frac{s^n \beta_{an} \alpha_{an}}{s^n + \sum_{i=0}^{n-1} \beta_{bi} \alpha_{bi} s^i \prod_{j=i}^{n-1} \frac{1}{C_{j+1} R_j}}.
$$
(2b)

Clearly, the coefficients of $D(s)$ and $N(s)$ can be independently adjusted through various $\beta_b \alpha_b$ and $\beta_a \alpha_a$, respectively

4 Experimental results

The 4th-order filter obtained from the topology of Fig. [2](#page-3-0) has been fabricated in a $0.18 \mu m$ N-well CMOS process. Die photograph of the filter is shown in Fig. [4](#page-3-0). The VB and DCCF of [\[25](#page-5-0)] are utilized to realize the widely programmable CCII of Fig. [3.](#page-3-0)

Throughout testing, the supply voltages were set to ± 0.9 V and the currents of the CCII were $I_B = 20 \mu A$ and $I_{SB} = 5 \mu A$. The respective standby currents of a CCII

Fig. 1 Realization of mixed-mode filter topology based on single output CCIIs

Fig. 2 A CM RNOF based on multi-output CCII

Fig. 3 A widely programmable multi-outputs CCII

with three outputs and the DCCF are approximately $3I_B + 6I_{SB}$ and $3I_B + 4I_{SB}$. Since the other CCIIs and DCCFs share the same I_B and I_{SB} , each of these CCII and DCCF is biased with $2I_B + 5I_{SB}$ and $2I_B + 3I_{SB}$, respectively. The corresponding total power consumption of the filter is approximately 1.55 mW. The input- and output currents are converted to voltage signals using passive resistors of 1 k Ω . A VB is also used to drive the output terminal. Equal resistors ($R_0 = R_1 = R_2 = R_3$) of 159 k Ω and equal capacitors $(C_0 = C_1 = C_2 = C_3)$ of 1 pF are used. These values lead to nominal pole frequency (f_o) of approximately 1 MHz. With eight-bit CDN, β can be adjusted from 0 to 0.996 whereas α can be changed from 1.004 to 256. First, CDNs are programmed to realize lowpass BT response with minimum pole frequency. This is achieved by selecting the lowpass output through setting

Fig. 4 Die photograph of the fabricated filter

 β_{a_1} through β_{a_4} to zero. The lowest pole frequency of approximately 250 kHz is obtained by setting $\beta_{b_0} \alpha_{b_0}$ to 0.0039 while the other corresponding values of $\beta_b \alpha_b$ and $\beta_{a_0} \alpha_{a_0}$ are given in Table [2](#page-4-0). The table shows the required theoretical values and the closest available digital word. Then, the pole frequency was varied to its maximum value of 4 MHz by setting $\beta_{b_0} \alpha_{b_0}$ to 256. The corresponding values for other $\beta_b \alpha_b$ and $\beta_{a_0} \alpha_{a_0}$ preserving the BT response and same gain are given in Table [2](#page-4-0). Next, the pole frequency was set to an arbitrary value of 1 MHz through

programming $\beta_b \alpha_b$ and $\beta_{a_0} \alpha_{a_0}$ according to the values given in Table 2. The obtained measurement results demonstrating pole frequency adjustments are shown in Fig. 5. After that, the filter was reconfigured to realize band- and highpass responses by selecting the desired output signals. The bandpass response is obtained by setting β_{a_0} , β_{a_1} , β_{a_2} , and β_{a_4} to zero while the highpass response is realized by making β_{a_0} , β_{a_1} , β_{a_2} , and β_{a_3} equal to zero. Also, gain adjustments are demonstrated by increasing the gain to 12 dB as shown in Fig. 6.

The linearity of the filter was determined by finding the input third-order intercept point (IIP3) determined by performing several intermodulation (IM3) tests using 800 and 900 kHz signals. IIP3 estimation for in-band signals measured at the LPF output is found to be approximately 28 dBm (referenced to 50 Ω). The output noise root spectral density for the LPF at gain of 12 dB was approximately 365 nV/Hz^{1/2} over the passband. Thus, the total in-band noise for the LPF is calculated to be less than -68 Bm over bandwidth of 1 MHz. These values correspond with inband spurious-free dynamic range of 64 dB.

5 Conclusion

The number of active devices can be reduced by using multi-output devices. But that approach traditionally leads to losing the programmability feature of $N(s)$ and/or $D(s)$ coefficients. In order to promote programmability feature, devices having different current gains would be required. This work adopts two CDNs in the design of digitally programmable CCII to provide wide tuning range suitable for FPAA. In general, the available solutions provide simulation results. Performance characteristics of the filters in terms of power consumption (only [[8](#page-5-0)] reported simulation results of 15.4 mW for 3rd-order filter), noise, and linearity are not reported. Hence, numerical performance comparison is not visible. However, it is clear that the proposed filter would provide improved performances due to significant reduction in the number of active devices

Table 2 Various settings to achieve the desired responses

Fig. 5 Measured (thick curve) BT response showing pole adjustments

Fig. 6 Measured (thick curves) band- and highpass responses with gain adjusted to 12 dB

and passive resistors. The proposed filter would require $n + 1$ CCIIs and $2n + 1$ CAs (DCCFs) compared with $3n - 2$ CCIIs and -CAs for its counterpart of [[4\]](#page-5-0). Whereas

BT 250 kHz	$b_0 = 0.0039$	$b_1 = 0.0406$	$b_2 = 0.2126$	$b_3 = 0.6521$	$a_0 = 0.0039$
Closest digital	$\beta_{b_0} = 00000001$	$\beta_{b_1} = 00001010$	$\beta_{h} = 00110111$	$\beta_{h} = 10100111$	$\beta_{a_0} = 00000001$
	$\alpha_{b_0} = 11111111$	$\alpha_{b_1} = 11111111$	$\alpha_{h_2} = 11111111$	$\alpha_{h_1} = 11111111$	$\alpha_{a} = 11111111$
BT 4 MHz	$b_0 = 256$	$b_1 = 10.44$	$b_2 = 54.52$	$b_3 = 166.8$	$a_0 = 256$
Closest digital	$\beta_{h_0} = 11111111$	$\beta_{h} = 11111111$	$\beta_{h} = 11111111$	$\beta_{b_2} = 11111111$	$\beta_{a_0} = 11111111$
	$\alpha_{b_0} = 00000001$	$\alpha_{b_1} = 00001010$	$\alpha_{b_2} = 00110111$	$\alpha_{b_2} = 10100111$	$\alpha_{a_0} = 00000001$
BT 1 MHz	$b_0 = 1$	$b_1 = 2.613$	$b_2 = 3.414$	$b_3 = 2.613$	$a_0 = 1$
Closest digital	$\beta_{b_0} = 11111111$	$\beta_{h} = 11111111$	$\beta_{b_2} = 11111111$	$\beta_{b_2} = 11111111$	$\beta_{a_0} = 11111111$
	$\alpha_{h_0} = 11111111$	$\alpha_{h_1} = 01011110$	$\alpha_{h_2} = 01001011$	$\alpha_{h_2} = 01011110$	$\alpha_{a} = 11111111$

obtained from 0.18 μ m CMOS process.

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proposed filter are supported by experimental results

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