A 2.4-GHz frequency synthesizer based on process and temperature compensated ring ILFD

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Abstract In this paper, a 2.4-GHz frequency synthesizer incorporating a ring-oscillator based process and temperature compensated injection-locked frequency divider (ILFD) is proposed. The synthesizer is implemented in a 0.18-μm standard complementary metal-oxide semiconductor process with a chip area of 3 mm × 3 mm plus the off-chip capacitors for loop filter. With an *LC* oscillator, the output frequency can be tuned from 2.057 to 2.652 GHz, while the settling time is around 36 μs with a loop bandwidth of 60 kHz. Measurements are performed across six different chips to study the circuit performance due to process variation. The worst-case total power consumption is measured to be 2.2 mW with a power supply of 1.8 V. The ILFD block is also tested separately and the test results show a wide locking range of 1.4 GHz over all the process corners and a temperature range from 0 to 80 °C.

Keywords Frequency synthesizer · ISM band · PLL · ILFD · Process compensated · Temperature compensated · Injection-locked

1 Introduction

The 2.4-GHz Industrial, Scientific and Medical (ISM) band [1] has been used for a diverse range of wireless applications such as Bluetooth and Zigbee since it is free and is capable of providing desirable bandwidth with high data rate compared with the other frequency bands. In this band, an important requirement of the wireless communication

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circuits involves operation robustness with very low noise and low-power dissipation.

Among the wireless communications circuits, the frequency synthesizer plays a crucial pole in terms of system performance such as power consumption, chip size, and signal–noise ratio (SNR). In a phase-locked loop (PLL) synthesizer, the most important blocks are the voltage-controlled oscillator (VCO) and the frequency divider, both of which operate at radio frequency (RF) and consume most of the power in a synthesizer. Particularly beyond GHz range, the frequency divider consumes a considerable part of the total power which in some cases can exceed 50 % of the total power consumed by the entire PLL system [2].

For high frequency of 2.4 GHz, the oscillator has been intensively studied and reported. Usually, for wireless communication equipments, the *LC*-tank oscillator is employed for low phase noise and stable operation over process and temperature variations. In some cases, the ring oscillator is also employed, but has poor noise performance, and needs careful compensation over the temperature variations [3]. In [3], the basic idea to overcome the temperature variations is provided by the constant current source generation with '*V-R*' topology. Here '*V*' stands for control voltage, while the resistor '*R*' is carefully selected by multiple comparisons among segmented threshold voltage, reference voltage and the control voltage. An array of comparators is used with several digital bits generated to achieve this. This technique requires precise comparator arrays and digital control bits, which contribute additional power consumption and system complexity.

On the other hand, to divide 2.4 GHz VCO output to a MHz range reference (usually from a crystal oscillator), the divider needs to provide a large division ratio of around several hundreds. Usually a prescaler is used initially to

divide the highest frequency first to a lower frequency so that the frequency output of the prescaler can be easily handled by a digital programmable divider [4]. Therefore, the prescaler is also required to be designed very carefully.

Compared to its digital counterparts, the injection locked frequency divider (ILFD) has recently found a wide acceptance since the ILFD can provide significantly lower power [2]. On the other hand, it also has drawbacks such as limited operation frequency range known as the locking range. An ILFD essentially is an oscillator when there is no frequency applied to its input. Therefore, similar to the oscillators, the ILFD can be also designed based on *LC*-tank or ring architecture.

Although *LC* oscillators have better immunity to process, voltage and temperature (PVT) variations, they are not suitable for prescaler design since the planar inductors require large on-chip surface area. Besides, the ILFD prescaler has very low phase noise when it is injection-locked regardless of its *LC*-tank or ring oscillator based architecture [5]. In addition, the *in-band* phase noise contribution from the divider is much less than those from other sources such as the reference or the VCO [6]. On the contrary, the ring oscillator can be very compact without the need for any inductor or large capacitor while also providing good locking range. Besides, the ring oscillator can consume much less power than its *LC* counterpart. The only drawback of the ring oscillator based ILFD would be the variations from process corners, voltage supply and temperature (PVT). A process and temperature compensated ILFD has been reported in [7]. In this design, a simple compensation technique is devised to compensate the ILFD and keep the locking range tight with process and temperature variations. This ILFD structure is incorporated in this proposed 2.4-GHz frequency synthesizer which is optimized to achieve wide locking range and robust operation over PVT variations for the entire PLL system.

This paper describes the PLL incorporating the ILFD reported in [7], including both brief mathematical derivations and test results. The rest of this paper is arranged as follows: Sect. 2 summarizes the ring oscillator-based ILFD with process and temperature compensation. Section 3 focuses on the other building blocks of the PLL, including VCO, digital programmable divider, phase frequency detector (PFD), charge pump (CP), and loop filter. Section 4 provides the test results for the ILFD and in particular measurement under process and temperature variations, system integration and the measurement of the PLL. Conclusion of this PLL work is provided in Sect. 5.

2 Wideband ring oscillator-based ILFD with process and temperature compensation

Ring oscillator has been employed in a number of implementations for ILFDs. An ILFD based on a five-stage ring of NMOS inverters with PMOS active loads is reported in [8]. This kind of topology has relatively low power consumption and a good locking range and can be extended easily to other odd-numbered division ratios. However, this circuit has single-ended structure which makes it unsuitable for applications requiring fully differential outputs. Besides, single-ended signals are more sensitive to process corners, temperature, power supply variations and common-mode noise interferences compared to the differential architectures. In addition, a fully-differential ring oscillator does not have the limit of odd stages and can have even stages which make it also suitable for even division ratios.

To get fully-differential output and large locking range, the ring oscillator-based topology is employed here with fully-differential inverters. Figure 1 shows the type of four-stage ring oscillator used in this work. It employs a symmetrical load with replica feedback biasing [9, 10]. The replica bias circuitry looks identical to the delay cells when it is switched from one side to the other. It sets the swing of the oscillator between V_{DD} and $V_{DD}-V_{CNTRL}$ using a feedback loop where V_{DD} is the voltage supply and V_{CNTRL}
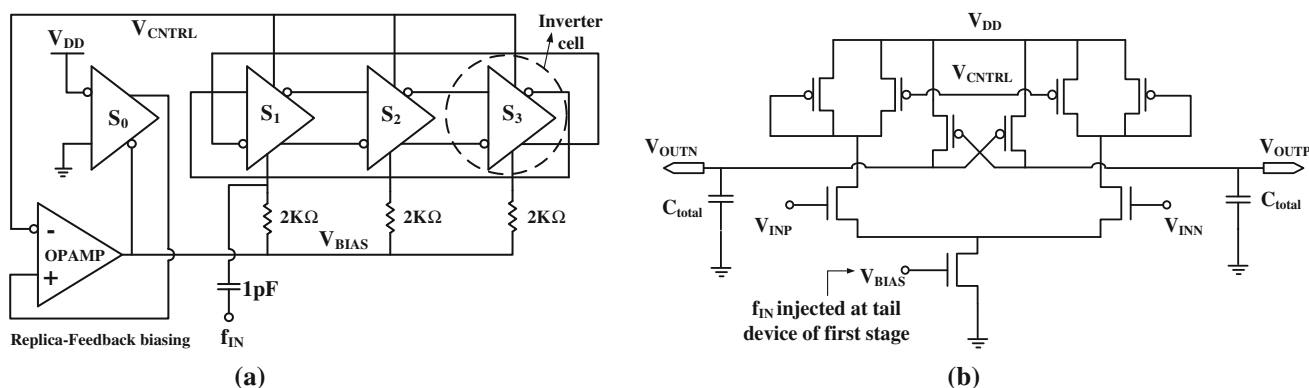

Fig. 1 a A ring oscillator-based ILFD using symmetric load, b an inverter cell with symmetric load

is the control voltage. The load element behaves like a linear resistor (to a first order) when the swing is controlled between these limits. This not only helps minimize the phase noise, but also offers a wide tuning range and reduced sensitivity of the oscillator to the supply and substrate noises [9]. A control voltage (V_{CNTRL}) is used by the replica bias circuitry to generate a bias voltage, V_{BIAS} that is used to vary the frequency of the ring oscillator. This control voltage can also help compensate the changes in the delay current from process variations. In this circuit, the latches are made stronger than those reported in [10]. It has

frequency is expressed in this way since the major contributors to the process and temperature variations are V_{thp}, K_p and C_{total} [11]. Therefore, those terms which are not dependent on process or temperature variations are not shown here. If V_{CNTRL} can be designed in a way that can compensate the variations of these contributors, then the ILFD can be process and temperature compensated.

Suppose the variation of V_{thp} can be expressed as ΔV_{thp}, and the K_p/C_{total} term has a variation of x % in the process corners. Then the oscillation frequency under corners f_{corner} can be expresses by Eq. (2):

$$f_{corners} \propto \frac{\left\{ V_{DD} - (V_{CNTRL} \pm |\Delta V_{CNTRL}|) - (|V_{thp}| \mp |\Delta V_{thp}|) \right\}^2}{\left\{ V_{DD} - (V_{CNTRL} \pm |\Delta V_{CNTRL}|) \right\} \cdot \left[1 + \theta \cdot \left\{ V_{DD} - (V_{CNTRL} \pm |\Delta V_{CNTRL}|) - (|V_{thp}| \mp |\Delta V_{thp}|) \right\} \right]} \left(\frac{Kp}{C_{total}} \right) \qquad (2)$$
$$\times (1 + 0.01x)$$

been observed that increasing the strength of the latch extends the locking range. However, this comes at the cost of reduced natural frequency of oscillation and hence more power consumption for dividing higher frequency signals. In order to alleviate the sensitivity of the oscillator to supply and substrate noises, a symmetric load [9] with replica feedback biasing is used in this work.

The ring oscillator based ILFDs have some good features as mentioned earlier. However, they are also sensitive to process and temperature variations that can cause their locking range to shift from the desired band. The ILFDs reported in literature mainly focus on the locking range and new topologies, but rarely on the process and temperature variations. Here, we present the ILFD with process and temperature compensated characteristics. The nominal oscillation frequency of the ring oscillator (f_{nom}) under typical process corner and temperature can be expressed below [7]:

$$f_{nom} \propto \frac{\left(V_{DD} - V_{CNTRL} - |V_{thp}| \right)^2}{(V_{DD} - V_{CNTRL}) \cdot \left\{ 1 + \theta \cdot \left(V_{DD} - V_{CNTRL} - |V_{thp}| \right) \right\}} \cdot \left(\frac{Kp}{C_{total}} \right)_{nom}$$
$$(1)$$

where K_p is $\mu_p C_{ox}/2$, with μ_p being the low-field mobility and C_{ox} the oxide capacitance per unit area. V_{DD} is the supply voltage, and C_{total} stands for the output capacitance for each stage, and V_{CNTRL} is the control voltage for the oscillator with V_{thp} denoted as the threshold voltage of PMOS. θ represents $1/(LE_{sat})$ with E_{sat} representing the saturation electric field and L is the length of PMOS load device. The oscillation

If the two equations under normal condition Eq. (1) and at process corners Eq. (2) are the same, then we can get the expression for the control signal after some mathematical derivations which are shown in detail in [7]. Therefore, the topology in Fig. 2 is developed to implement the control signal generation.

From the circuit, the control signal can be expressed as,

$$V_{CNTRL} = V_{DD}\left(1 + \frac{R_1}{R_2}\right) - \left(1 + \frac{R_1}{R_2}\right)V_{thp,1} - V_{thp,2}$$
$$- \left\{ V_{ov1}\left(1 + \frac{R_1}{R_2}\right) + V_{ov2} \right\} \qquad (3)$$

where $V_{thp,1}$, $V_{thp,2}$ are the threshold voltages of the transistors M_1, M_2 respectively and V_{ov1}, V_{ov2} are the
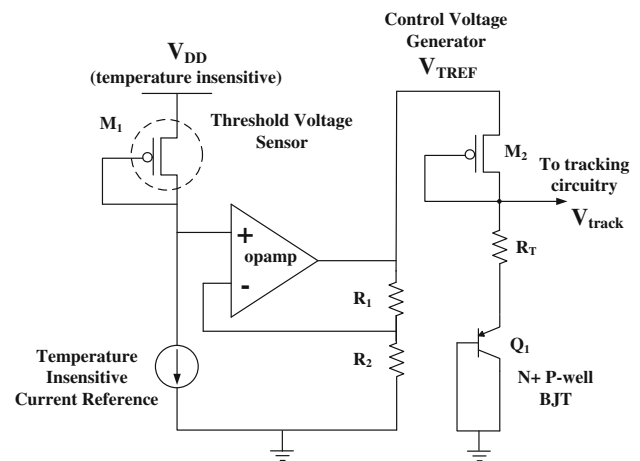

Fig. 2 Circuitry for compensating temperature and process variations
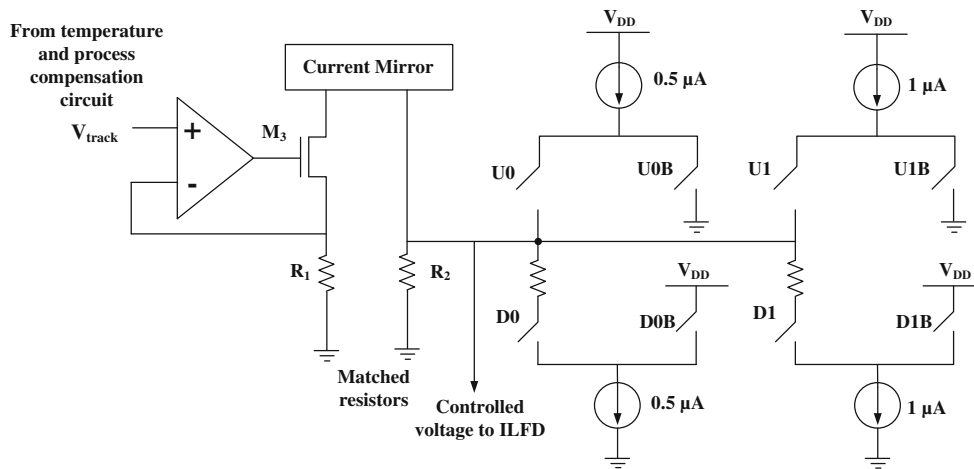
Fig. 3 Schematic of the calibration circuitry

overdrive voltages of M_1 and M_2 respectively. From Eq. (3), the change in V_{CNTRL} with process can be expressed as,

$$\pm \Delta V_{CNTRL} = \mp \left(1 + \frac{R_1}{R_2}\right) \cdot \Delta V_{thp,1} \mp \Delta V_{thp,2}$$
$$\mp \Delta V_{ov1} \left(1 + \frac{R_1}{R_2}\right) \mp \Delta V_{ov2} \qquad (4)$$

The changes in V_{thp} and V_{ov} values of M_1 and M_2 from their typical values of $V_{thp, nom}$ are found out for all the process corners through DC simulation in HSPICE^{TM} using foundry provided BSIM3V3.2 transistor models. This information is used to set ΔV_{CNTRL} such that it matches the value obtained by solving Eqs. (1) and (2) for all the process corners. The aspect ratio of the transistors M_1, M_2 and the resistors R_1, R_2 are used to achieve the required values of ΔV_{CNTRL} over all process corners.

The circuit used to compensate for the process variations (Fig. 2) imparts temperature dependence on V_{CNTRL}. According to Eq. (3), V_{CNTRL} has a positive slope with temperature since threshold voltages of M_1 and M_2 have negative slope with temperature. This can be compensated using the negative slope of the emitter–base voltage (V_{EB}) of a bipolar junction transistor (BJT) [10]. Then the control voltage expression can also be written as,

$$V_{CNTRL} = I_{d,M2} \cdot R_T + V_{EB} \qquad (5)$$

where, $I_{d,M2}$ represent the current flowing through transistor M_2 which is directly proportional to temperature (PTAT current). This in combination with the positive temperature coefficient of R_T imparts a positive slope to the term, $I_{d,M2} \cdot R_T$ with temperature. To keep V_{CNTRL} constant over temperature, the positive temperature coefficient of the first term can be cancelled by the negative slope of the V_{EB} term. In addition, the effective slope of V_{CNTRL} changes with process. This can be addressed by adjusting the aspect ratio of M_2 and the

resistor R_T such that the frequency deviation around the nominal process corners at room temperature is minimized.

The voltage, V_{CNTRL} generated by the process and temperature compensation circuitry is converted to a current in the calibration circuitry as shown in Fig. 3. Logic signals $U (0:1)$ and $D (0:1)$ control the switches of a charge-pump like circuitry. Depending upon the control bits, currents of varying amplitude are pumped in (out) of the resistor R_2. The control voltage is then found by summing the currents through the resistor R_2. This control voltage is then fed to the ILFD to control the locking range. The calibration circuitry can be used to increase the locking range without oversizing the latches.

Table 1 shows the simulated oscillation frequency changes at different frequency corners under room temperature. This ILFD can achieve good process and temperature variations while keeping good locking range and relatively low power consumption [7].

3 Other building blocks

3.1 VCO architecture

The phase noise of the VCO is high-pass filtered in a PLL and therefore the noise contribution to the phase noise of

Table 1 Frequency of oscillation with and without compensation (room temperature)

Process corner	Frequency without compensation (MHz)	Frequency with compensation (MHz)
TT	632	632
FF	772	625
SS	512	642
SF	720	643
FS	548	627

Fig. 4 *LC*-tank VCO based on current-reuse topology and band switching
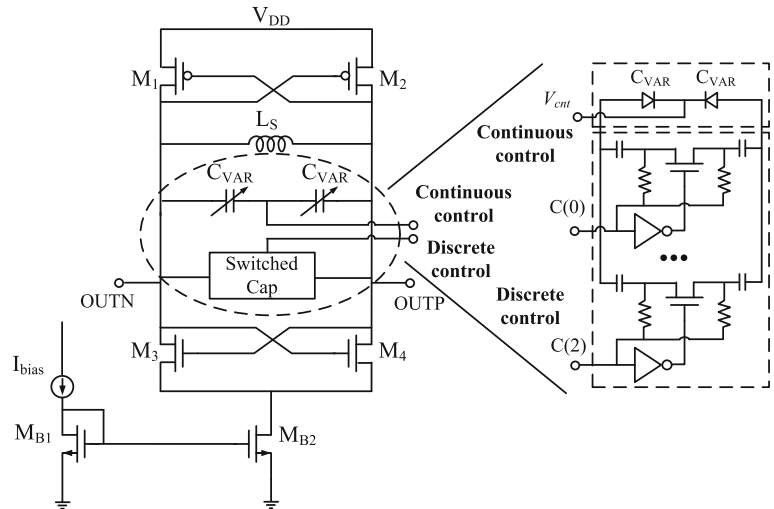
the synthesizer at high offset frequencies (and hence the out-of-band interference) is dominated by the VCO phase noise [6]. Due to the spectral purity demanded by radio applications, cross-coupled *LC*-tank VCO is the most popular choice [12]. The complementary one employs the current-reuse topology consisting of both PMOS and NMOS devices, as shown in Fig. 4. The cross-coupled pairs M_1–M_2 and M_3–M_4 provide the necessary negative resistance required to cancel the loss in the tank. The negative resistance is contributed by both NMOS and PMOS devices and is given by,

$$R = -\frac{1}{g_{m,n} + g_{m,p}} \qquad (6)$$

where $g_{m,n}$ and $g_{m,p}$ are the transconductance of NMOS (M_3, M_4) and PMOS (M_1, M_2) separately.

With both PMOS and NMOS transistors being used, this architecture needs reduced power consumption compared to those with only PMOS or NMOS devices. Increasing the current leads to an increased voltage swing across the tank (current-limited mode) until a point is reached (voltage-limited mode) where increasing the current does not improve the voltage swing anymore. The phase noise of the VCO improves in the current-limited mode and saturates (and may even become worse) in the voltage-limited mode [13]. Therefore, the VCO should be operating in the region between these limits for best phase noise performance for a given power dissipation [12]. The PMOS and NMOS devices are sized to have an equal transconductance to achieve symmetry and minimize flicker noise up-conversion. The current-reuse architecture causes the voltage swing to be limited by the power supply rails.

In sub-micron complementary metal-oxide semiconductor (CMOS) processes, with low supply voltages, the gain of the VCO (K_{VCO}) needs to be very high to generate the wide
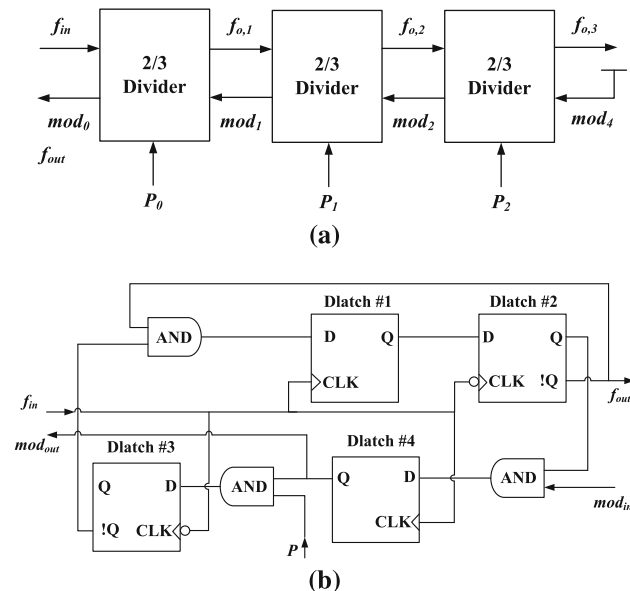

Fig. 5 Schematic block diagram of: **a** digital programmable dividers, **b** 2/3 divider cell in **a**
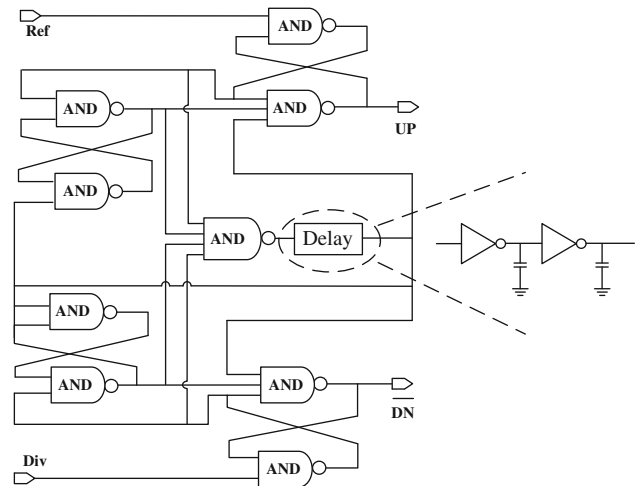

Fig. 6 Schematic of the phase frequency detector for minimizing the 'dead-zone' of the PLL
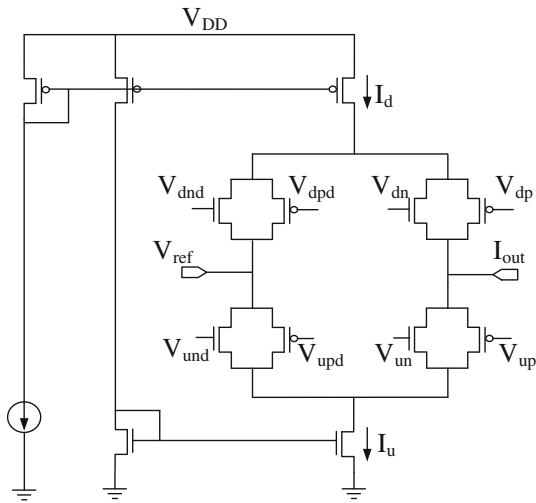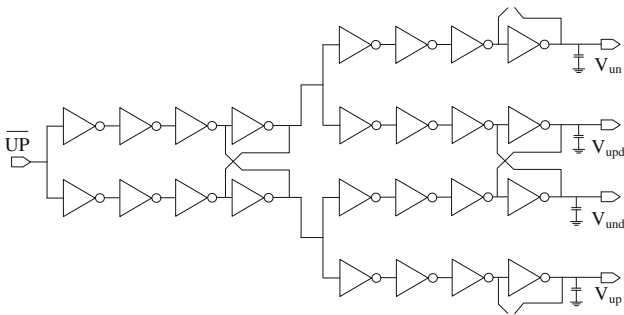
Fig. 7 Schematic of the charge pump circuit
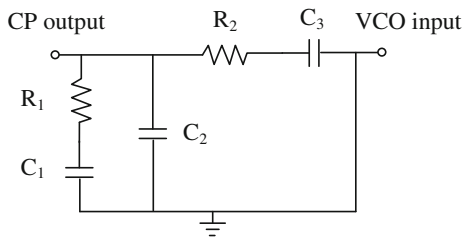

Fig. 8 Timing circuitry for th charge pump

Fig. 9 Circuit diagram of the loop filter used in the PLL system

Fig. 10 Linearized frequency model of the PLL system

Table 2 Parameters of components in the loop filter

Loop-bandwidth	60 kHz
I_{CP}	80 μA
C1	7 nF
C2	353 pF
C3	353 pF
R2	1.4 KΩ
R3	1.4 KΩ
K_{VCO}	200 MHz/V
Phase margin	56°
f_{ref}	50 MHz
Division modulus	8–15

range of frequencies to cover the frequency band of interest under process and temperature variations. An increased K_{VCO} renders the VCO very sensitive to flicker noise up-conversion and also to power supply and substrate noises [14, 15]. Supply and substrate noises can reach extremely high levels in a fully-integrated environment and can bring the VCO jitter in the time domain resulting in spurious sidebands in the frequency domain [10, 16, 17]. The spurs in the frequency domain leads to increased RMS phase errors [16]. The magnitude of the spurs g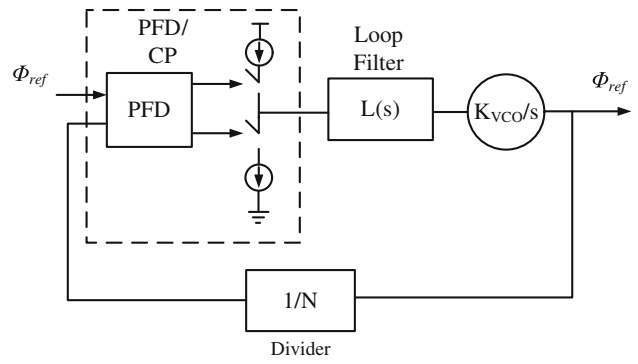enerated by the VCO is directly proportional to K_{VCO}. The impact of supply and substrate noises on the performance of the PLL is dealt in [17, 18]. Also, the reference noise caused due to the charge pump is a direct function of the VCO gain [16]. The VCO will therefore be implemented using the popular band-switching topology,
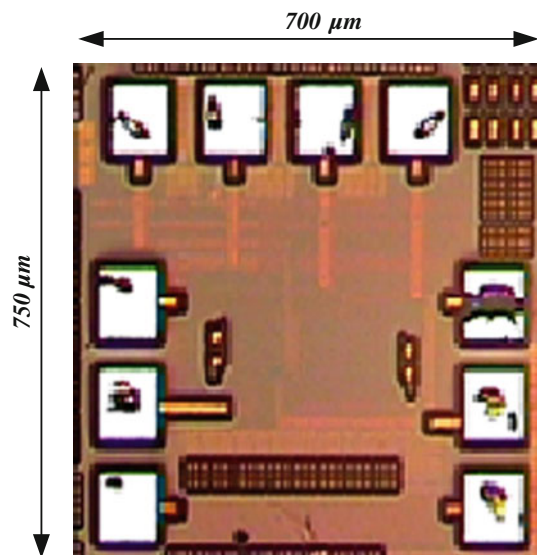

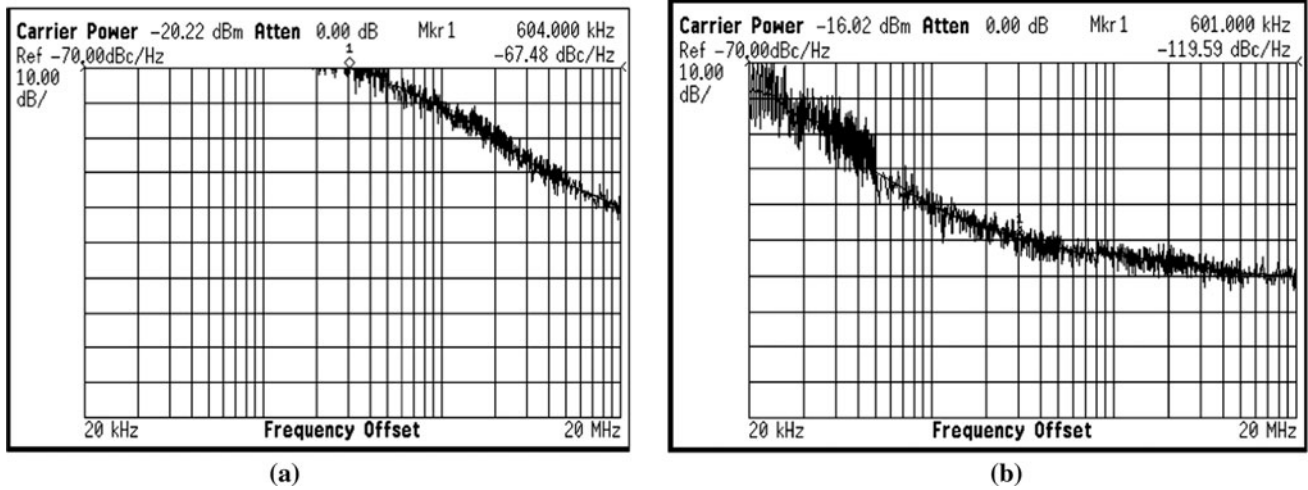Fig. 11 Chip microphotograph of the ILFD

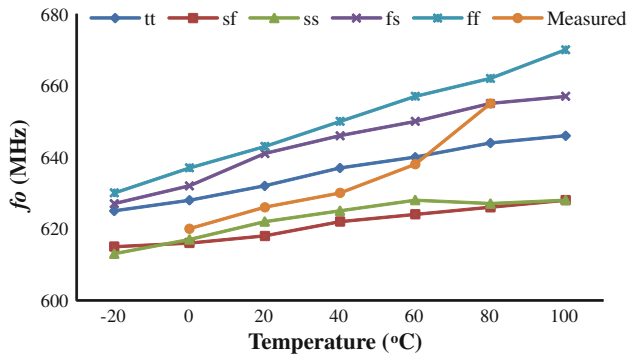**Fig. 12** Phase noise performance of **a** free running oscillator, **b** ILFD

Fig. 13 Frequency variation of the PATS ring oscillator with process and temperature compensation

Table 3 Summary of the performance of the ILFD

Locking range	1.4 GHz
Max. input frequency	3.5 GHz
Power consumption	0.6 mW
Input power	0 dBm
Division	4
Calibration	Yes
Sensitivity of delay elements to noise	Low
Temperature, process sensitivity	Low
Technology	0.18 μm

which uses both discrete and continuous control as shown in Fig. 4 [19]. The band-switching topology uses a digital word $C(0)$–$C(2)$ (coarse tuning) to shift the frequency range of operation and a fine tuning to tune control voltage V_{cnt} (or lock) to a particular frequency.

3.2 Digital programmable dividers

The architecture of the multi-modulus divider is shown in Fig. 5(a) [16]. It consists of a chain of 2/3 divider cells connected in a ripple-counter fashion. The divider is capable of achieving a division ration from 8 to 15, depending on the digital control bits P_0–P_2. This topology offers at least two advantages: lower power dissipation as the clock lines are fed to the adjacent divider cells only and

Table 4 Frequency of oscillation with and without compensation (room temperature)

Works	Dehghani and Atarodi [21][a]	Samavati et al. [22]	Lee et al. [23]	Lee et al. [24]	This work
Technology (μm)	0.25	0.24	0.18	0.13	0.18
Topology	Differential ring	Differential LC	Differential LC	Single-ended ring	Differential ring
Locking range (GHz)	0.4	0.1	3.6	1.46	1.4
Max. input frequency	2.6	5	11.63	5	3.5
Power dissipation (mW)	1	0.8	19.92	0.42	0.6
Division ratio	4	2	2	4	4
Temperature, process variation	Large	Small	Small	Large	Small
LROP (GHz/mW)	0.4	0.125	0.18	3.47	2.333

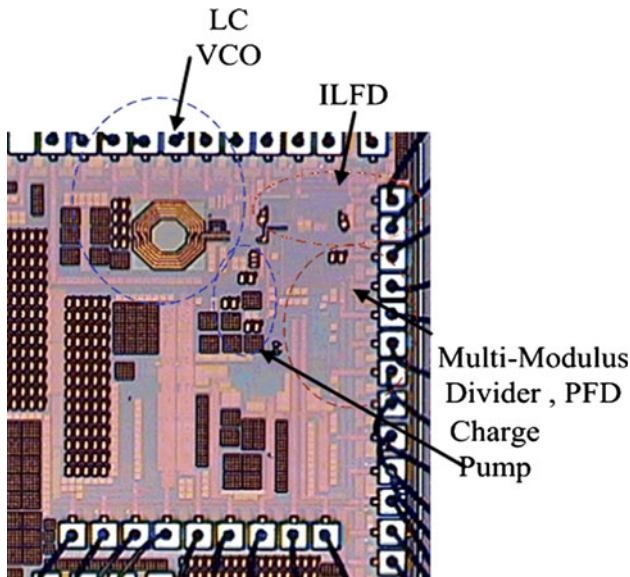[a] All data is from simulation result, no test result is reported

Fig. 14 Chip microphotograph of the complete PLL system

highly modular design, resulting in the same circuit for adjacent divider cells which enables layout reuse.

The block diagram of the 2/3 divider is shown in Fig. 5(b). If the signal 'P' is high the divider divides its input by 3, otherwise it divides by 2. To minimize the noise due to jitter accumulation in the asynchronous divider, the signal mod_0 is used to clock the PFD input. The signal mod_4 is set to logic 'high'. Each 2/3 divider cell here is implemented using true single phase clocking (TSPC) D-latches to minimize power consumption and to provide a larger swing compared to source coupled logic (SCL) structure [13]. The larger swing also minimizes the phase noise of the divider. The division ratio in Fig. 5(a) is given by,

$$N = 2^N + P_{N-1}2^{N-1} + P_{N-2}2^{N-2} + \cdots + P_0 \tag{7}$$

3.3 Phase frequency detector and charge pump

Figure 6 shows the schematic of the phase frequency detector (PFD) including a delay stage to avoid the 'dead-zone'. It is implemented by inverters stage with capacitor at the load. The reference frequency of 50 MHz results in a period of 20 ns. Therefore the delay stage is designed to provide about 2 ns time delay in the simulation.

The charge pump (CP) should be very carefully designed to minimize the reference spurs in the output. Ref. [13] describes the charge pump design in more details. A special timing circuitry is developed prior to the CP to minimize the effects caused by the mismatches in the 'UP'/'DN' currents of the CP, such as gain mismatch, dynamic mismatch, and propagation delay
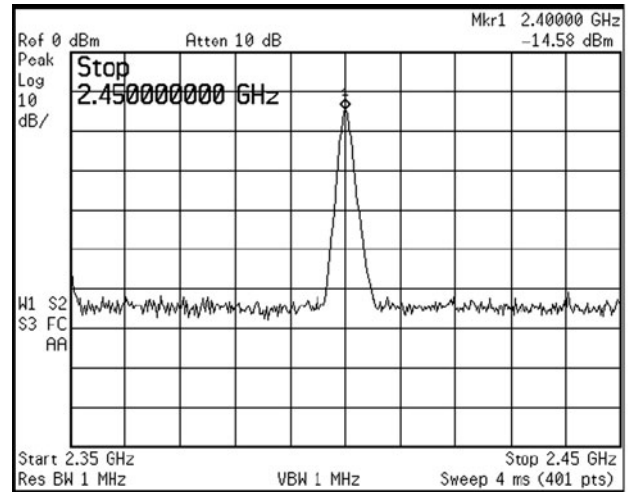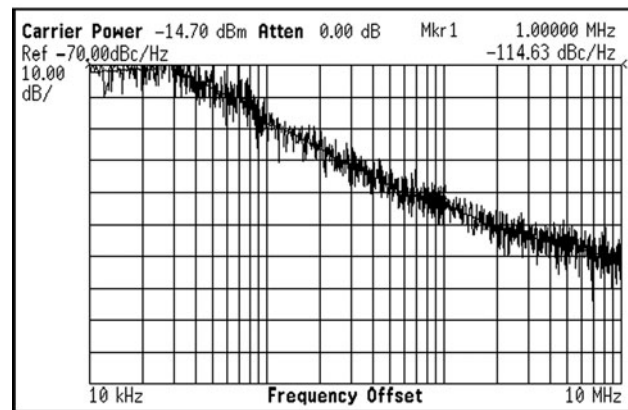
Fig. 15 PLL test results showing a output spectrum of the PLL centered at 2.25 GHz, b phase noise of PLL at 2.25 GHz output frequency, the phase noise level at 1 MHz offset is −114.63 dBc/Hz

Table 5 Summary of the performance of the PLL

Technology		0.18 μm
Frequency range		2.057–2.652 GHz
Reference frequency		50 MHz
Phase noise	10 kHz offset	−72 dBc/Hz
	1 MHz offset	−114.63 dBc/Hz
	10 MHz offset	−132.13 dBc/Hz
Power supply		1.8 V
DC power consumption at 2.4 GHz		2.2 mW
Settling time		36 μs
Loop bandwidth		60 kHz
Silicon area on chip		3 mm × 3 mm

mismatch and so on. It converts the 'UP' and 'DN' from single to differential signals, which can improve the charge pump switching dynamics and therefore suppress

Table 6 Comparison among this work and other published PLLs

Work	Process	Power supply (V)	Power (mW)	Frequency (GHz)	Divider topology	Variation over frequency	
						Temperature	Process corner
Rategh and Lee [2]	0.5 μm	2.5	3	1.8	ILFD	No PVT compensation	
Chong et al. [3]*	0.13 μm	1.8	N/A	2.56	Digital	±3.9 %	±0.6 %
Kondou and Mori [25]	90 nm	1.2	1.7	0.15	N/A	±2 dBc/Hz within 10 MHz offset under any PVT condition	
Chen et al. [26]**	0.13 μm	0.5	0.37	0.4	Digital	N/A	14 %
Lin and Liu [27]	65 nm	1.35	120.8	132.6	ILFD	No PVT compensation	
This work	0.18 μm	1.8	2.2	2.4	ILFD	4.2 %	4.6 %

* All data is from simulation result, no test result is reported

** All data is from simulation result, no test result is reported

the spurs furthermore. Figure 7 shows the schematic of the charge pump. Figure 8 shows the timing circuitry for 'UP' signal which can obtain fast switching and high spurious suppression, and this circuitry is applied to 'DN' signal as well.

In addition, the current sources in CP are never switched off to prevent current switching effects on the drains of the current sources. When the charge pump is in the 'off' state, current is re-directed into a dummy branch. Since the current sources are always 'on', no start-up delay occurs and the charge pump responds immediately to changing control signals. Spurs are also caused due to charge injection from the switches as they are turned 'on' and 'off' [20]. Using NMOS and PMOS switches in parallel (transmission gate) and controlling them with signals that change sufficiently fast serve to minimize the spurs.

3.4 Loop filter

Figure 9 shows the loop filter used in this PLL system. To provide better noise filtering, a third-order filter is employed here. With the simple loop frequency model shown in Fig. 10, the phase margin (PM) can be expressed as:

$$PM = \tan^{-1}(\tau_1 \omega_c) - \tan^{-1}\left(\frac{A(\tau_1 \omega_c)}{1 - B(\tau_1 \omega_c)^2} \right) \quad (8)$$

where, $A = \frac{C_2/C_1 + C_3/C_1 + (1 + C_2/C_1) * \tau_2/\tau_1}{1 + C_2/C_1 + C_3/C_1}$, $B = \frac{C_2/C_1 + \tau_2/\tau_1}{1 + C_2/C_1 + C_3/C_1}$, $\tau_1 = R_1 C_1$, $\tau_2 = R_3 C_3$, and ω_c is the cross-over frequency.

The components parameters are finalized considering trade-offs between the bandwidth and the phase margin. Table 2 shows the components values for the achieved phase margin of 56°.

4 Implementation and measurement

4.1 ILFD measurement

Figure 11 shows the chip microphotograph of the ILFD. It occupies a silicon area of 700 μm × 750 μm. The maximum measured locking range is 1.4 GHz centered at 2.5 GHz. Figure 12 shows the phase noise of the free running oscillator (without input) and the ILFD with an input signal frequency of 2.4 GHz and a power of −3 dBm. From the figure, it can be clearly seen that the phase noise has an obvious improvement with the injection locking.

Figure 13 shows the post-layout simulation and the measured frequency variation of the 3-stage ring oscillator with process and temperature compensation. The worst-case frequency variation (simulated) is reduced from 26 % (without compensation) to 4.6 % (with compensation) over process corners and a temperature range of −20 to 100 °C. Six different chips are measured from various corners of the wafer. The worst-case frequency deviation from 625 MHz is 4.4 %. Also, the measured oscillation frequency of one of the chips varies only by 3.6 and 2 % at 80 and 0 °C, respectively, compared with a value of 632 MHz under room temperature [7].

Table 3 shows the summary of the performance of the ILFD. Table 4 compares the performance of this ILFD with some published works. The most widely-used figure-of-merit (FoM) for an ILFD is locking range over power (LROP). This work shows good LROP with very small temperature and process variation. The works in [22] and [23] also have small PVT variations due to the LC oscillator topology, but the locking rang or power consumption performance is not good. While the work in [24] uses single-ended ring oscillator, which has good LROP, but the

PVT variation is large compared with this differential work with compensation.

4.2 PLL system measurement

Figure 14 shows the chip photograph for the entire PLL chip, which occupies 3 mm × 3 mm as the total silicon area.

Figure 15 shows the output spectrum of the PLL when it outputs a 2.4 GHz frequency with an output spectrum level of −14.58 dBm. In this figure, the spurs can be also found with a level of −57 dBm at 50 MHz offset, which is around 42 dB lower than the signal spectrum.

A summary of the performance of this PLL work is shown in Table 5. Table 6 shows the comparison among this work and some recently published works [25–27]. There are not many publications with PVT compensated PLL, especially with ILFD as prescaler. From the table, this work demonstrates a good trade-off among power consumption and PVT tolerance. It also provides another good example of PVT compensated low-power and compact ILFD design.

5 Conclusion

A PLL targeted for 2.4 GHz ISM is designed and fabricated in a 0.18-μm CMOS technology. This PLL is designed with a process and temperature compensated ILFD based on full-differential ring oscillator. Test results show that this ILFD can work with very low sensitivity to process and temperature variations. With the robust ILFD and *LC* oscillator, the PLL can work with good stability over process corners and temperature variations. Future goal focuses on the further design improvements for applications of the proposed PLL in portable medical devices.
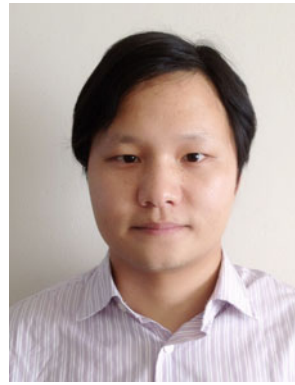
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