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A broadband, differential transimpedance amplifier in 0.35 μm SiGe BICMOS technology for 10 Gbit/s fiber optical front-ends

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Abstract This study focuses on 10 Gbit/s differential transimpedance amplifier. At the beginning of the work, the amplifier circuit is deeply analyzed and is optimized for the best phase linearity over the bandwidth resulted in a group delay variation less than 1 ps. The amplifier circuit is designed with 0.35 μm SiGe heterojunction bipolar transistor BICMOS process. 9 GHz bandwidth, almost 58 dBΩ transimpedance gain with less than 11.18 pA/$\sqrt{\text{Hz}}$ averaged input-referred noise current are achieved. Electrical sensitivity is 15 μA_{pp}. Power consumption is 71 mW at 3.3 V single power supply.

Keywords Transimpedance · SiGe · Fiber optic · Amplifier · Optical receiver · Front-end

1 Introduction

Transimpedance amplifier (TIA) is the most critical part of the fiber optical front-ends and its design is the most challenging and care demanding part of the optical amplifier design, because it is located at the right after photodiode and converts electrical current to the voltage. Very high bandwidth and low-noise TIAs are needed for 10 Gbit/s and beyond data rates applications. These applications, therefore, require devices with high transition frequencies (f_T). Until recent years, high-cost III–V semiconductor technologies, such as GaAs and InP, dominated the optical front-ends and receivers [1, 2] because they exhibited excellent performance in speed and noise. These technologies also have high junction break-down voltage which is not strictly necessary for TIAs, because the output swing of the fiber optical amplifiers usually lower than 1 V. Silicon based bipolar TIAs were also presented. The major demerit of the Si-bipolar TIAs was that they generally showed poor noise performance and lower sensitivity [3]. CMOS process is also becoming a low cost, low power choice for lower data rates [4]. Bipolar transistors, however, are faster than CMOS transistors for the same size and higher transconductance can be achieved. SiGe heterojunction bipolar technology (HBT) has recently provided a cost-effective alternative and higher integration levels, especially in BICMOS process, with improved sensitivity for 10 Gbit/s fiber optical front-ends and for the development of photoreceivers. One of the most important advantages of the SiGe BICMOS technology is that it enables analog and digital parts of the optical receiver to be integrated in the same chip. In that case, output drivers and output impedance matching networks are avoided. Since SiGe simultaneously enables high speed and low power consumption, it is becoming an important choice for the realization of high speed fiber optical receivers.

Block diagram of a typical fiber optical receiver is shown in Fig. 1. The optical signal is detected and converted to an electrical current by a photodiode. A TIA converts the electrical current to a voltage and amplifies it. This quantity of amplification is not sufficient for signal processing. Therefore, right after TIA, a main amplifier (MA), which is voltage amplifier, amplifies the signal higher amplitudes. This makes data pulses coming from fiber optics safely be detectable and processed at the subsequent stages. MA could be in the form of automatic gain control amplifier (AGC) enabling transimpedance gain of

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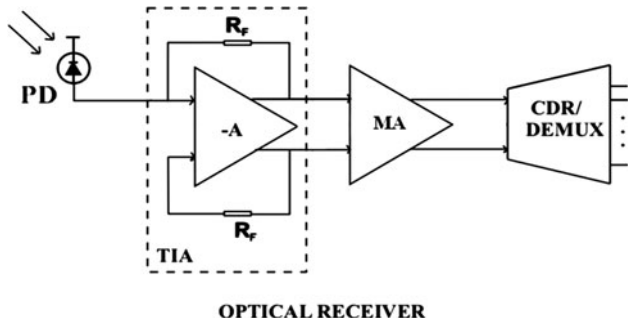

Fig. 1 A typical fiber optical front-end with shunt-feedback TIA

the front-end to be lowered for large input signals or in the form of limiting amplifier (LA) which limits the output signal for large input signals. If low distortion is strictly necessary, then AGC must be preferred. In other case, where distortion can be ignored, then LA is preferred because of its simplicity.

Clock and data recovery (CDR) extracts the digital data and clock information from the received signal. This is done by defining threshold voltage. The pulse is assigned to "1" when the pulse amplitude above the threshold voltage. In other case, pulse amplitude is lower than threshold voltage, the pulse is assigned to "0". During extraction of clock data from the signal, CDR decides at the mid-point of the pulse in order to lower bit error rate (BER). The recovered data are finally demultiplexed as parallel channels having lower data rates.

In addition to low power and single supply operation, TIA must exhibit low-noise and linear phase response in order to be used for 10 Gbit/s applications. Trade-off between noise, speed, gain and supply voltage present many challenges in TIA design. Since TIA dominates noise of the overall receiver, its bandwidth should be limited to minimize noise. On the other hand, because of the limited bandwidth, TIA can produce intersymbol interference (ISI) which lowers BER. A group delay variation of the frequency response over the specified bandwidth is another important performance parameter. Typical group delay variation for 10 Gbit/s applications to minimize data-dependent jitter is $|\Delta\tau| < 10$ ps [5, 6]. The overall sensitivity of the receiver is determined by the TIA, because TIA is the first electrical part of the receiver after photodiode. Sensitivity of an optical front-end is defined in terms of electrical and optical. As given in (1), electrical sensitivity i_{sens} is the required minimum peak-to-peak current at the input of the receiver to achieve specified BER. Optical sensitivity P_{sens} in Eq. (2) includes responsivity of the photodiode and is defined in terms of averaged optical power necessary to achieve minimum specified BER. In Eqs. (1) and (2), R is the responsivity of the photodiode, $\overline{i_n}$ is the total integrated input-referred noise current of the receiver; Q is a measure of the ratio between signal and noise. Minimum required BER at 10 Gbit/s bit rate is 10^{-12}, and Q is 7.035 at BER of 10^{-12} [6].

$$i_{\text{sens}} = 2Q\overline{i_n} \tag{1}$$

$$P_{\text{sens}} = \frac{Q\overline{i_n}}{R} \tag{2}$$

This study presents a differential, low-noise transimpedance amplifier for 10 Gbit/s fiber links using 0.35 μm SiGe HBT BICMOS process, which is well suited for 10 Gbit/s photoreceivers. In Sect. 2, theoretical basics of the proposed TIA are investigated and design is achieved. Section 3 gives the simulation results and Sect. 4 concludes the study.

2 Circuit design

As a first stage, TIA must have a very little group delay deviation from the low frequencies up to high frequencies, because time jitter caused by excessive group delay variation cannot be compensated for at the succeeding stages. In contrast, a drop in signal magnitude at higher frequencies can be improved by using MA after the TIA. For that case, lowering the group delay variation over the bandwidth was one of the major issues during the design. Since MA is differential, differential operation must be fulfilled. For single-ended output TIA, this can be done by applying reference voltage to the one input of the MA and applying TIA output to the other input [7]. This technique requires design of reference voltage generator circuit. In other case, TIA is designed in differential architecture having differential outputs. The latter makes the TIA immune to any common mode noise so in this case it is preferred over the single-ended structure. However, the input-referred noise power of the differential TIA is twice than that of the single-ended structure.

Cascode [8] and inductive peaking [9] techniques including active inductive peaking [10] were the alternative choices to reach desired bandwidth (around 8–9 GHz) for the TIA. Broadband operation, however, has been fulfilled without using these techniques since f_T of the technology, which is around 70 GHz, relatively enough for 10 Gbit/s speed to achieve desired bandwidth. Common-emitter with shunt-feedback resistor is used in the design because of its good noise performance over the common-base structure.

Differential SiGe TIA schematic is shown in Fig. 2. The PIN photodiode with the intrinsic capacitance of 100 fF is assumed at the input of the front-end. Since photodiode output is single-ended, current from the photodiode is directed to the only one input of the TIA (T_1). In this case, photodiode capacitance C_P is replicated at the other input (T_2) to achieve fully symmetrical operation. This can be

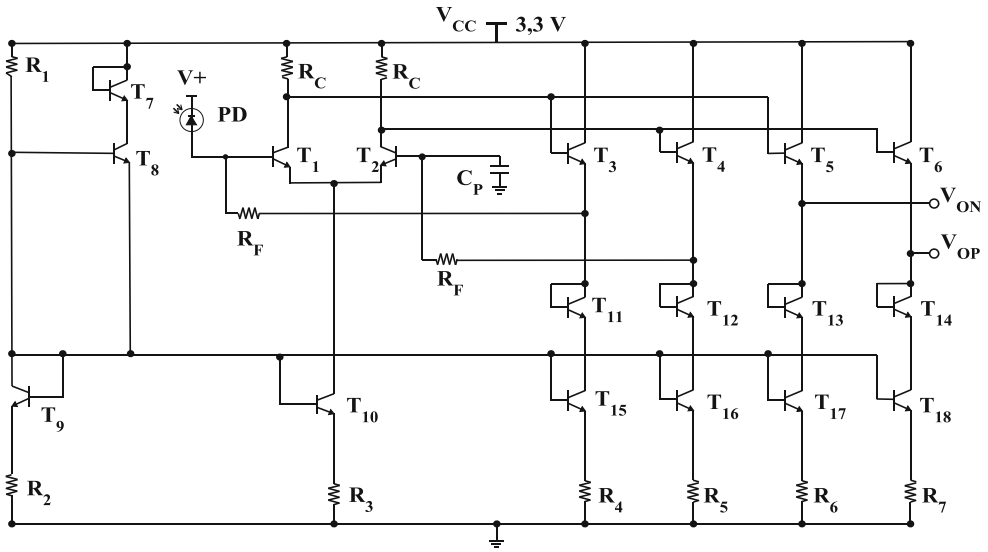

Fig. 2 Proposed differential SiGe TIA schematic

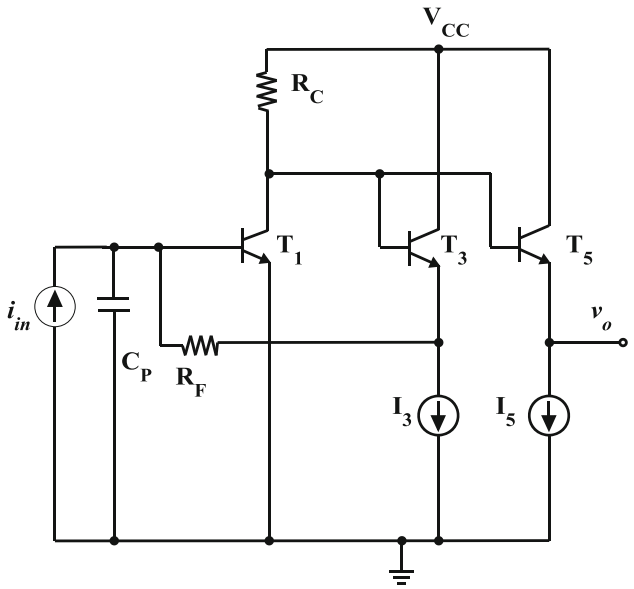

Fig. 3 Half-circuit model of the differential SiGe TIA with photodiode equivalent circuit

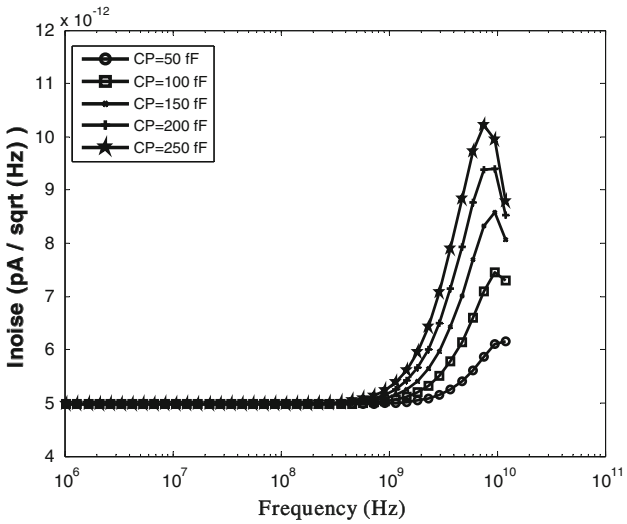

Fig. 4 Photodiode capacitance effect on noise

done during chip design by placing dummy photodiode to the unused input (T_2) or by calculating the total capacitance at the input (T_1), including parasitic capacitances, and placing that total capacitance at the unused input (T_2) [11]. The dominant pole of the TIA is determined by the time constant at the input node of the TIA. Shunt-feedback resistors R_F are applied around voltage amplifier to reduce input impedance, which also reduces time constant at the input nodes allowing -3 dB cut-off frequency to be higher. Emitter followers (T_3, T_4, T_5, T_6) are used for DC level shifting and as buffer to drive next stages. The outputs are isolated from the feedback networks in order to prevent transimpedance gain and bandwidth from degradation because of the loading effect of the subsequent stage. Current mirrors are used as loads in order to neglect high value resistors from the design. All diode connected transistors are needed for level shifting in order to keep V_{CE} less than break-down voltage. Beta helper (T_8) and emitter degeneration resistors are used at the biasing circuit in order to improve current matching performance of the current mirrors.

For extracting transfer function and noise equations, half-circuit model of the differential TIA is used as shown in Fig. 3. The TIA has a voltage amplifier and a shunt-feedback resistor R_F. I_3 and I_5 are the current sources representing the current mirrors. Voltage gain of the emitter follower at the last stage is assumed approximately one. T_1 and T_3 are accepted as the same transistors. Voltage amplifier is only modeled with dominant pole. With the help of [6, 12–14] transimpedance Z_T is

$$Z_T(s) = -\frac{A_o R_{eff}}{1 + s\frac{R_{eff}}{R_f'}\left(\tau_c + C_t R_f'\right) + s^2 \tau_c C_t R_{eff}} \quad (3)$$

where,

$$A_o = -g_m R_c \frac{r_\pi}{r_b + r_\pi} \quad (4)$$

$$R_{eff} = \frac{r_\pi R_f}{r_\pi(1 + A_o) + R_f} \quad (5)$$

$$C_t = C_p + C_\pi + C_\mu(1 + A_o) \quad (6)$$

$$\tau_c = R_c\left(2C_\mu + C_{cs}\right) \quad (7)$$

$$R_f' = \frac{R_f r_\pi}{R_f + r_\pi} \quad (8)$$

C_μ is the base–collector capacitance; C_{cs} is the collector–substrate capacitance and C_t is the total capacitance at the input of the TIA. r_b is the intrinsic base resistance; r_π and C_π base–emitter resistance and capacitance, respectively. A_o is the open loop DC voltage gain. From (3), DC transimpedance gain R_T is

$$R_T = \frac{v_o}{i_{in}} = -A_o R_{eff} \quad (9)$$

In a second order system, the damping factor must be equal to $\frac{\sqrt{3}}{2}$ in order to obtain Bessel response which has a maximally flat group delay in the pass band. Using $\frac{\sqrt{3}}{2}$ in Eq. (3), bandwidth of the TIA is as follows;

$$f_{-3dB} = \frac{1.07 A_o}{2\pi R_{eff} C_t} \quad (10)$$

This result mandates that bandwidth of the voltage amplifier must be a factor 3 larger than the unity-gain frequency of the open-loop response [12]. Since, input transistors T_1 and T_2 are biased for highest f_T, R_C and R_f are the major design parameters to obtain maximally linear phase response. R_f is also restricted by the transimpedance gain and noise parameters. Since input impedance directly affects stability of the TIA, HBT with 2 base contacts are chosen in order to make a compromise between base resistance and base parasitic capacitance. R_C and R_f are chosen as 900 and 150 Ω, respectively [13].

Equivalent input-referred noise current spectrum $\overline{i_{n,in}^2}$ of the half-circuit of the proposed shunt-feedback TIA given in Fig. 2 can be written as;

$$\frac{\overline{i_{n,in}^2}}{\Delta f} = \frac{4KT}{R_f} + 4KTr_b\left|sC_p\right|^2 + 2q\frac{I_{C1}}{\beta} + \frac{1}{g_{m1}^2\left|Z_{\pi 1}\right|^2}\left[2qI_{C1} + \frac{4KT}{R_c} + \frac{\overline{v_{n3}^2}}{\Delta f}\frac{1}{R_c^2} + \frac{\overline{v_{n5}^2}}{\Delta f}\frac{1}{R_c^2}\right] \quad (11)$$

where,

$$\frac{\overline{v_{n5}^2}}{\Delta f} = 2qI_{C5}\left|Z_{e5}\right|^2 + 2qI_{B5}\left|\frac{1}{sC_{\mu 4}}||Z_{\pi 5}\right|^2 + 4KTr_b \quad (12)$$

$$\frac{\overline{v_{n3}^2}}{\Delta f} = 2qI_{C3}\left|Z_{e3}\right|\left|R_f\right|^2 + 2qI_{B3}\left|\frac{1}{sC_{\mu 3}}||Z_{\pi 3}\right|^2 + 4KT(r_b + R_f) \quad (13)$$

k is the Boltzmann constant, T is the temperature in kelvin and q is the electric charge. $\overline{v_{n3}^2}$ and $\overline{v_{n5}^2}$ are the equivalent input-referred noise voltage generators at the input of the T_3 and T_5, respectively. For complete circuit $\overline{i_{n,in}^2}$ is twice that given in Eq. (11). Dominant noise sources are base and collector shot noise sources of the input transistors T_1 and T_2 [3rd and 4th terms in Eq. (11)] and thermal noise sources from R_f feedback resistors and intrinsic base resistances r_b [first and second terms in Eq. (11)]. Since low frequency corner of fiber communications is a couple of kHz, flicker and popcorn noise sources can be neglected. Increasing the value of R_f will decrease the noise and bandwidth but also will increase the low-frequency transimpedance gain. Photodiode capacitance, C_P, directly affects noise performance of the TIA as shown in Eq. (11). This is also depicted in Fig. 4. In this case, C_P is swept from 50 fF to the 250 fF. As C_P becomes higher, noise of the circuit increases for the same operating frequency after around 1 GHz.

3 Simulation results

Simulation is performed with the technology of 0.35 μ SiGe HBT BICMOS process whose f_T is about 70 GHz. Figure 5 shows differential transimpedance gain of the SiGe TIA. Flat frequency response is obtained. Bandwidth is 9 GHz and low frequency differential transimpedance gain is 57.93 dBΩ. Figure 6 depicts group delay variation

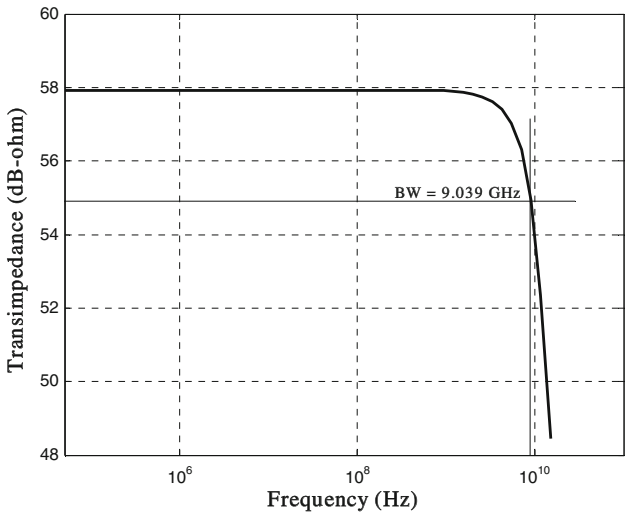

Fig. 5 Differential transimpedance gain of the TIA

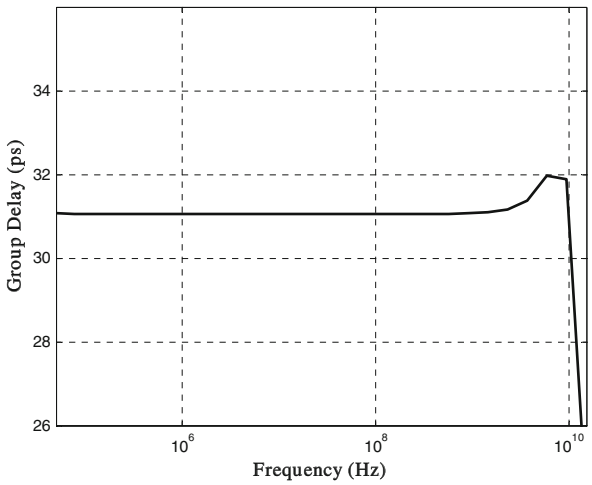

Fig. 6 Group delay variation of the frequency response over the bandwidth

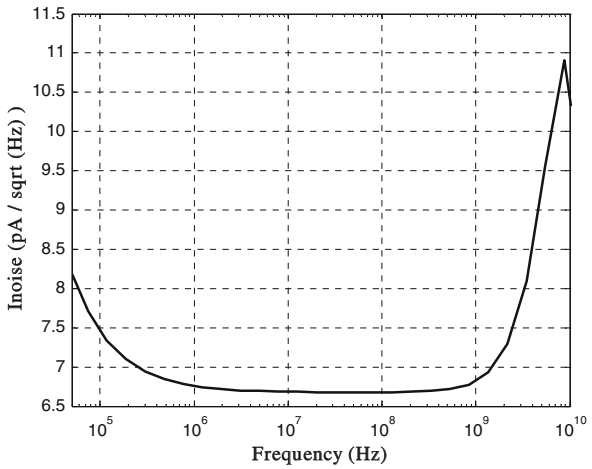

Fig. 7 Total input-referred noise current spectrum of the differential TIA

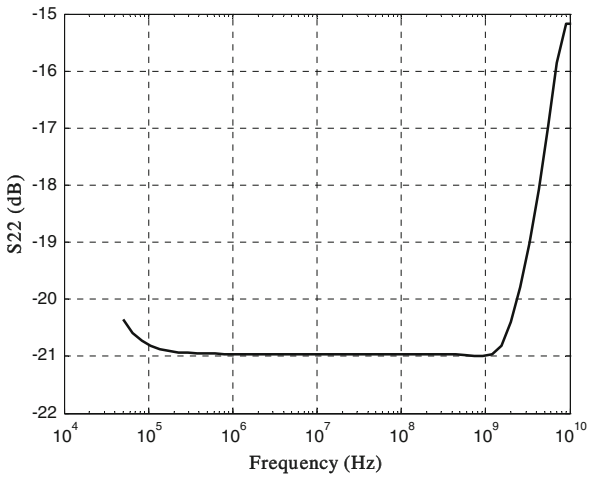

Fig. 8 Single-ended S_{22} parameter of the proposed TIA. 30 Ω resistors are added to the both outputs for 50 Ω impedance matching

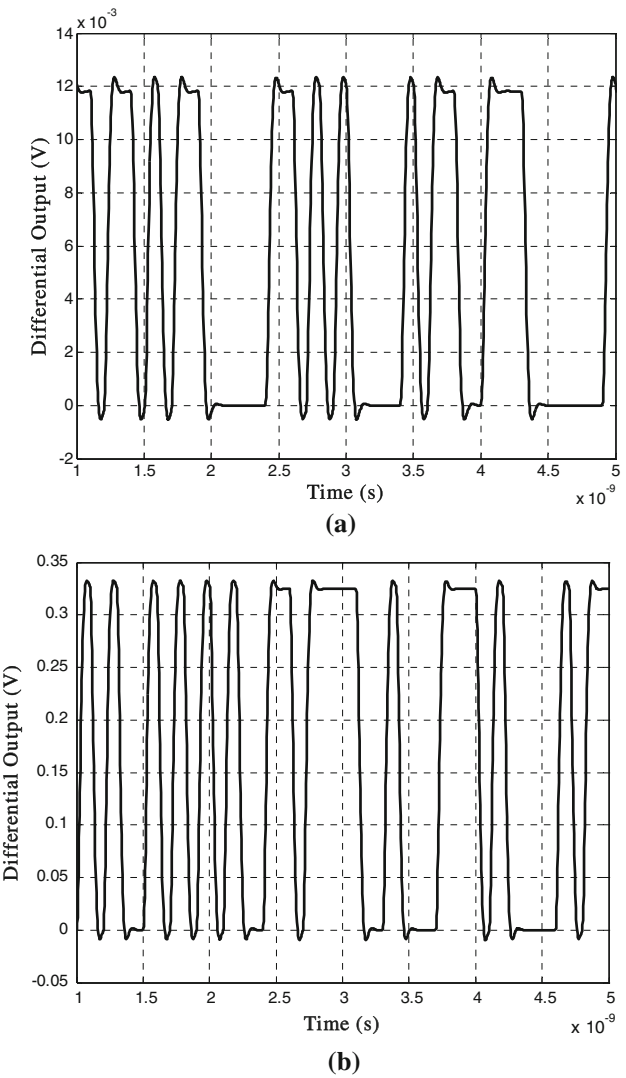

Fig. 9 Differential output waveform of the proposed TIA. The input data stream is NRZ 10 Gbit/s $2^{31}-1$ PRBS. **a** Input current is 15 μA_{pp}. **b** Input current is 400 μA_{pp}

over the frequency. Less than 1 ps variation over the bandwidth is obtained.

Input-referred noise current simulation is shown in Fig. 7. Noise current is below 7 pA/$\sqrt{\text{Hz}}$ up to 1 GHz, and it is below 11 pA/$\sqrt{\text{Hz}}$ between 1 and 9 GHz. Total integrated input-referred noise current $\overline{i_n}$ is calculated as 1.061 μA. 14 GHz noise bandwidth is taken into account to calculate $\overline{i_n}$. As expected, noise is dominated by base and collector shot noise and thermal noise of the base resistance of the input transistors T_1 and T_2 (66 % of the total noise). Feedback resistors R_f contribute to the noise around 22 %. Using the Eq. (1), sensitivity of the differential TIA at BER of 10^{-12} is calculated as 15 μA_{pp}. Maximum peak-to-peak input current of the TIA is 400 μA_{pp}. Although linearity of the signal is preserved up to 1 mA_{pp} input current levels, higher peak-to-

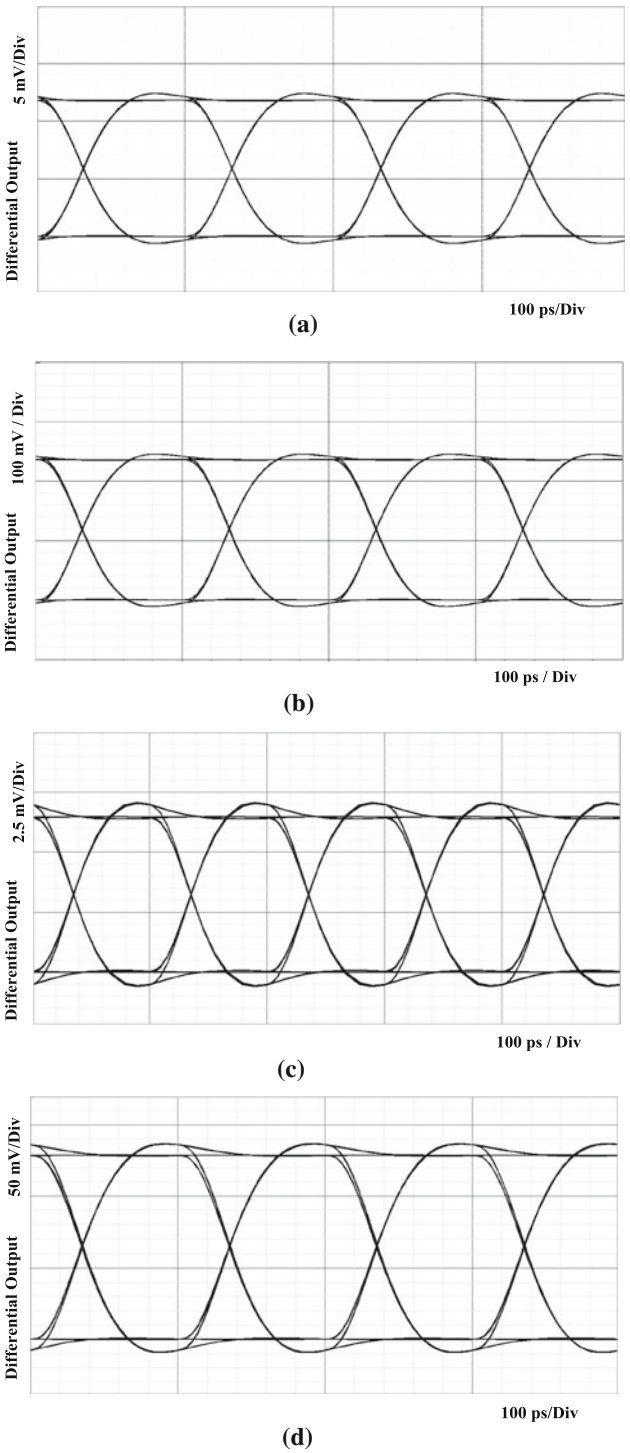

Fig. 10 Eye diagrams of the differential output at 10 Gbit/s $2^{31}-1$ PRBS data stream. **a** Input current is 15 μA_{pp}, both outputs are loaded with 100 fF capacitors. **b** Input current is 300 μA_{pp}, both outputs are loaded with 100 fF capacitors. **c** Input current is 15 μA_{pp}, both outputs are loaded with 50 Ω resistors. **d** Input current is 300 μA_{pp}, both outputs are loaded with 50 Ω resistors. In the case of **c** and **d** 30 Ω matching resistors are added to the both outputs

peak currents than 400 μA_{pp} will cause V_{CE} of the T_1 and T_2 to exceed collector–emitter junction break-down voltage.

Figure 8 shows single-ended S_{22} parameter of the proposed circuit. The proposed differential TIA is intended for integrated receiver compromising both TIA and MA on the same chip. If differential TIA is not implemented on the same chip with the MA, then TIA must have capability to drive 50 Ω loads. Hence, 30 Ω resistors are added to the both outputs for impedance matching. Good matching is achieved with S_{22} less than −15 dB over the bandwidth. Adding matching resistors causes 5 dBΩ loss to the mid-band transimpedance gain for a single-ended output.

Differential output waveform of the TIA is depicted in Fig. 9. The TIA input is driven with a NRZ data stream of 10 Gbit/s and $2^{31}-1$ pseudo random bit sequence (PRBS) with the amplitude of 15 and 300 μA_{pp}. Differential output swing is 12 and 320 mV_{pp}, respectively. Eye diagram simulations resulted in a wide eye opening shown in Fig. 10. The TIA outputs are loaded with 100 fF capacitors in the first case [15] and loaded with 50 Ω loads in the second case. In the latter, 30 Ω matching resistors are added to the both outputs. The eye openings are clear for both horizontal and vertical openings.

Table 1 shows simulation performance of the proposed circuit with some existing circuit and designs. III–V technologies such as GaAs and InP has recently not preferred in photoreceivers because they are power hungry devices for the same speed. They are also generally not cheap. In Refs. [16] and [17], there are not noise and sensitivity results. CMOS has lower transimpedance for the same speed. Another performance parameter of TIAs is group delay variation. The proposed circuit has very good group delay variation performance (less than 1 ps). This is shown with transient waveforms having little distortion.

4 Conclusions

The differential SiGe transimpedance amplifier and simulation results for 10 Gbit/s fiber optical receivers are presented. No inductor is used to achieve wideband operation. 0.35 μ SiGe HBT BICMOS technology enables TIA to be a cost-effective alternative and to be combined with digital blocks of the fiber optical receiver. The differential structure of the TIA makes it immune to the effect of the supply and substrate noise. Table 1 summarizes the simulation results of the proposed differential SiGe TIA. The TIA bandwidth is 9 GHz with little non-linear phase response and differential transimpedance gain is almost 58 dBΩ. The electrical sensitivity of the proposed TIA is 15 μA_{pp}. Power consumption

Table 1 Simulation performance summary and comparison with the other works

References	[16]	[17]	[18]	[This study]
Technology	0.35 μm SiGe	60 f_T GaAs	0.18 μm CMOS	0.35 μm SiGe
Transimpedance	60.49 dBΩ differential	28 dBΩ differential	40 dBΩ differential	57.9 dBΩ
Bandwidth	10.42 GHz	10.5 GHz	8.69 GHz	9 GHz
Group delay variation	–	–	–	<1 ps
Averaged input noise	–	–	96.48 pA/$\sqrt{\text{Hz}}$	11.18 pA/$\sqrt{\text{Hz}}$
Sensitivity (@ BER = 10^{-12})	–	–	–	15 μA_{pp} Electrical
Max. differential output swing	466 mV	–	–	320 mV
Supply voltage	3.3 V	−5.2 V	1.8 V	3.3 V
Power dissipation	148 mW	368 mW	15.33 mW	71 mW
Work	Simulation	Fabricated chip	Simulation	Simulation

is 71 mW and maximum differential output swing is 320 mV_{pp}. It is shown that the differential TIA is well-suited for 10 Gbit/s data rate fiber optical receivers.

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