Analog Integr Circ Sig Process (2013) 74:91–96
DOI 10.1007/s10470-012-9946-0

Basic circuits for multi-valued sequential logic

Fatma Sarica · Avni Morgül

Received: 11 January 2012 / Revised: 14 June 2012 / Accepted: 4 August 2012 / Published online: 29 August 2012

Abstract Multi-valued logic circuits were presented as an alternative to well known binary logic. It has the potential of reducing the number of active elements and interconnection lines. More data may be transferred trough a single wire using logic signals having more than two levels. However, in spite of their potential advantages, developments in multi-valued systems are not satisfactory. In particular, it is very difficult to find circuits to implement the multilevel sequential circuits. The flip-flop is the basic building block of sequential circuits and may be used to design sequential circuits such as counter/dividers and other sequential circuits. In this regard, a new multilevel flip-flop, called the AB flip-flop, was developed and published by the authors recently (Sarica and Morgul, Electron Lett 47(5):297–298, 2011). In this paper we present a new latch and restoration circuit which improves the performance of the previously designed flip-flop circuit. It is also shown that any sequential circuit may be implemented by using this flip-flop.

Keywords Multivalued logic · Sequential logic · Multivalued flip-flop · Current mode CMOS logic

F. Sarica
Electrical & Electronics Engineering Department, Bogazici University, Istanbul, Turkey
e-mail: fatma.sarica@boun.edu.tr

A. Morgül (✉)
Electronics & Communication Engineering Department, Beykent University, Istanbul, Turkey
e-mail: avnimorgul@beykent.edu.tr

1 Introduction

The use of circuits with more than two logic levels has been offered as a solution to the interconnection and routing problems. Such circuits, named as multiple-valued logic (MVL) circuits, have a potential for reducing the chip area consumed by interconnection wiring and functional units in very-large scale integration (VLSI). Applying signals having more than two levels to a single wire, reduces the number of wires for the same range of data, and this reduction results in a decrease in number of required IC pins. As the interconnection length and number of wires used is reduced, the space between any two wires increases without increasing the total silicon area, leading to a decrease in resistance and capacitance of contacts and interconnections.

Due to the limited supply voltages, higher radices cannot be obtained using voltage mode circuits. On the other hand, current mode circuits have the advantages of current scaling, copying and sign changing with a simple current mirror. So, the current-mode logic is chosen because of their potential in implementing higher radices.

However, in spite of their potential advantages, developments in multi-valued systems are not satisfactory. There are two important drawbacks of the current mode multi-valued circuits. These circuits consume a static DC power continuously, since the input or the output variable is a current and this current usually has non-zero values. The second disadvantage is the difficulty of finding circuits to implement the multilevel sequential circuits. With the addition of multilevel sequential circuits almost every type of binary logic circuits can be realized using the multiple-valued approach, like adder/multiplier circuits, memory circuits, sequential circuits, decoders/encoders, current/voltage comparators, programmable devices and etc. Some of these circuits may be compatible with their binary counterparts.

Flip-flops are well known basic elements of sequential circuits and can be realized using multiple-valued logic circuits. Characteristic equations and next-state tables of the multi-valued conventional flip-flops such as RS and JK are defined in the Ref. [1, 2]. Studies about implementation of these flip-flops can be found in the literature but they are very limited and complicated [3, 4]. In addition, these conventional flip-flops use input values, current state output and inverse of current state output for calculating the next-state output. In current-mode multi-valued circuits, inversion operation is performed by subtracting the input signal from $(r-1) \times I_b$, where r is the radix (number of logic levels) and I_b is the reference current level and other logic levels are determined as integer multiples of this reference current. In this study, we use 4-level logic with the $I_b = 5$ µA reference current level. So the logic levels 0, 1, 2 and 3 correspond to 0, 5, 10 and 15 µA respectively. The inverter circuit needs to use the maximum current and it consumes a lot of power. Therefore it must be avoided to keep the power consumption at minimum level.

2 AB flip-flop

We propose a new flip-flop structure named as *AB flip-flop* due to its A and B inputs, and its next-state equation is defined as follows [5];

$$Q_{n+1} = A + B \times Q_n$$

the idea behind this definition is that, it does not involve any inversion operation. The inversion operation should be avoided in the current mode logic design, because it increases the power consumption of the circuit considerably. Because, inversion is performed by subtracting the current from the maximum allowable current.

The state transition table of the AB flip-flop is given in Table 1. Table clearly shows that the flip-flop can successfully change its state for any input combination.

Block diagram of the AB flip flop is shown in Fig. 1. It is composed of a MIN circuit to perform AND operation, a MAX circuit to perform OR operation and a LATCH/RESTORER circuit to hold the current state and to restore the output current.

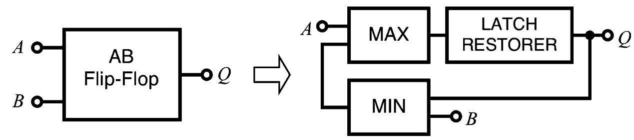


Fig. 1 AB flip-flop

The MIN and MAX circuits are current-mode, multi-input circuits, working based on *winner/loser-takes-all* principle [6, 7]. (Fig. 2).

2.1 The new latch/restorer circuit

The main drawback of current-mode multi-valued logic circuits is that they are not self restored unlike the binary logic circuits. The predefined current levels can be deviate from their original values due to some variations in active element dimensions, power supplies, technology parameters, etc. This variation on the output signal is carried to next stages. It can be tolerated and output can be detected correctly for a range of value that is called *noise margin* (i.e., $\pm I_b/2$ for this application). But the signal must be restored to its original value before it exceeds this limit, in order to obtain a correct output. The flip-flop circuits have positive feedback in nature, which prohibits any variation from the predefined levels. Otherwise this variation forces the output to shift either to ground or power supply voltage. So it is necessary to use a restoration circuit in the flip-flop to avoid this problem.

The restoration circuit given in Fig. 3 is based on the upper threshold circuit given in Ref. [8, 9].

$$a|_b^c = \begin{cases} c & \text{if } a \geq b \\ 0 & \text{otherwise} \end{cases}$$

For a 4-level logic system ($r = 4$) the restoration algorithm may be expressed as follows:

$$\langle x_1 \rangle = x|_{r/2}^{r/2} = x\,[\text{mod}\ (r/2)]$$
$$\langle x_2 \rangle = x_1\,[\text{mod}\ (r/4)] \quad x_1 = (x - \langle x_1 \rangle)$$
$$\langle x \rangle = \langle x_1 \rangle + \langle x_2 \rangle$$

here x is the input, and $<x>$ is the restored output.

Table 1 Transition table of the AB flip-flop

Q_n	AB															
	00	01	02	03	10	11	12	13	20	21	22	23	30	31	32	33
0	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3
1	0	1	1	1	1	1	1	1	2	2	2	2	3	3	3	3
2	0	1	2	2	1	1	2	2	2	2	2	2	3	3	3	3
3	0	1	2	3	1	1	2	3	2	2	2	3	3	3	3	3

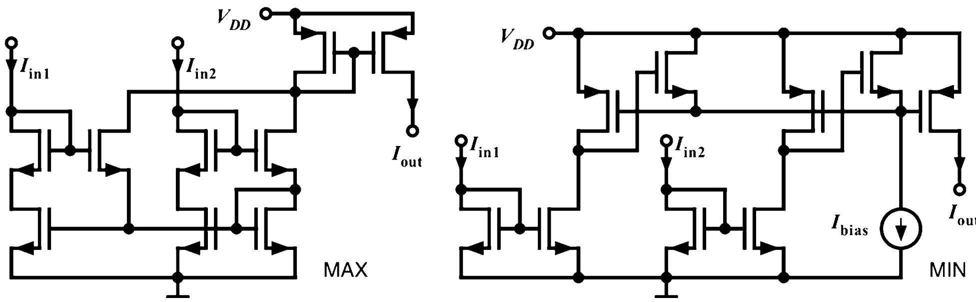
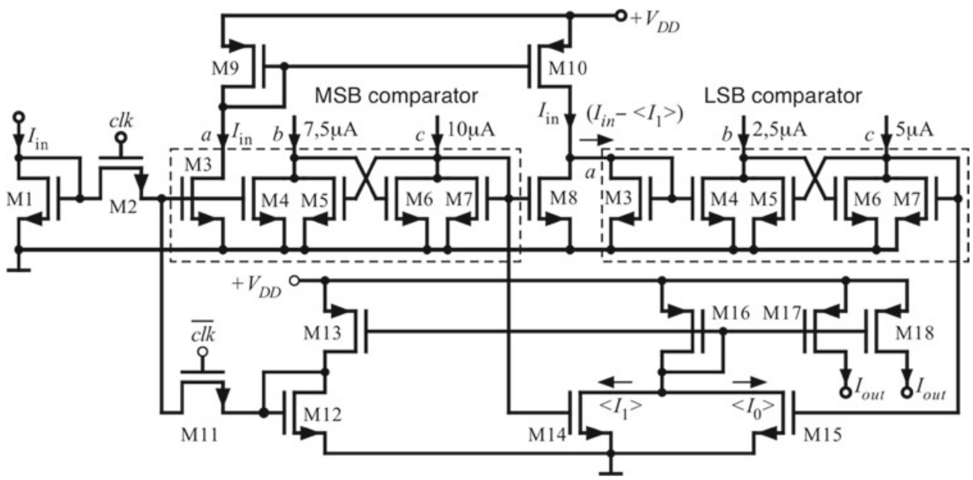


Fig. 2 MAX and MIN circuits based on winner/loser takes all principle



Transistor dimensions: $(W/L)_{1,2,3,4,7,8,11,12,14,15}$=5/4, $(W/L)_5$=1/4, $(W/L)_6$=5/1, $(W/L)_{9,10,13,16,17,18}$=15/4

Fig. 3 The new latch and restoration circuit

The input current is first compared to $I_{max}/2$ and if the current is greater than 15/2 = 7.5 μA the MSD of the restored signal $<I_1>$ is set to logic 2 (i.e. $<I_1> = 10$ μA) otherwise it is set to zero. Then $<I_1>$ is subtracted from the input current and the reminder is compared to 2.5 μA. If it is smaller than 2.5 μA the LSD of the restored signal $<I_0>$ is set to zero, otherwise it is set to logic 1 (i.e. $<I_0> = 5$ μA).

We can summarize the operation of the restoration circuit as follows:

$$\begin{aligned} <I_1> &= 10\,\mu\text{A} \quad \text{if } I_{in} \geq 7.5\,\mu\text{A} \\ <I_1> &= 0 \quad \text{if } I_{in} < 7.5\,\mu\text{A} \\ <I_0> &= 5\,\mu\text{A} \quad \text{if } (I_{in} - <I_1>) \geq 2.5\,\mu\text{A} \\ <I_0> &= 0 \quad \text{if } (\text{I}_{in} - <\text{I}_1>) < 2.5\,\mu\text{A} \\ I_{out} &= <I_1> + <I_0> \end{aligned}$$

Both HOLD and RESTORE operations are performed at the same time, by using the circuit given in Fig. 3. The restoration circuit is modified as latch/restorer circuit, by adding two pass transistors M2 and M11.

The opposite phase voltage mode clock signals (clk, $\overline{clk}$) stimulate the pass transistors and perform the timing of the flip-flop circuit. In order to keep the restored data, the first pass transistor M2 is turned off and the output current is mirrored to the input trough the second pass transistor M11 during the second half of the clock signal. Using current mode clock signals does not improve the circuit performance, but requires additional circuitry and increases the power dissipation.

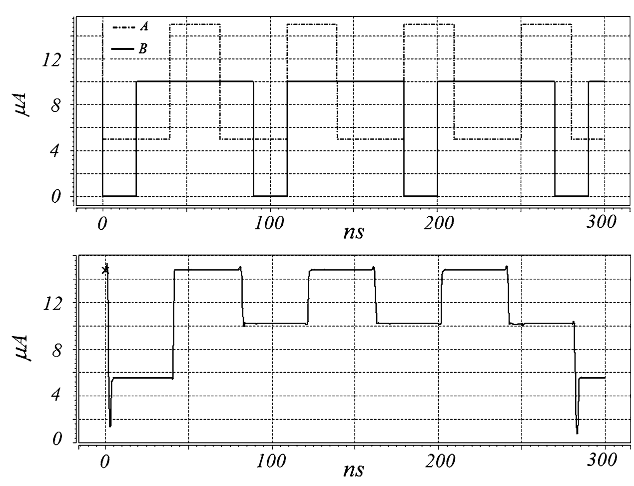


Fig. 4 The inputs and Q output signal of the AB flip-flop

Table 2 Comparison of the circuits in Ref. 5 and the new circuits

	Logic levels	No. of transistors	Layout area	Used technology	Supply voltage	Power consumption
Latch circuit in Ref. [5]	4	29	16.92 × 7.47 μm	0.18 μm	1.8 V	116 μW
New latch circuit	4	26	21.33 × 6.39 μm	0.18 μm	1.8 V	130 μW
Latch circuit in Ref. [5]	8	53	30.96 × 7.47 μm	0.18 μm	1.8 V	329 μW
New latch circuit	8	38	29.7 × 6.39 μm	0.18 μm	1.8 V	305 μW
New AB flip-flop	4	44	42 × 6.39 μm	0.18 μm	1.8 V	193 μW

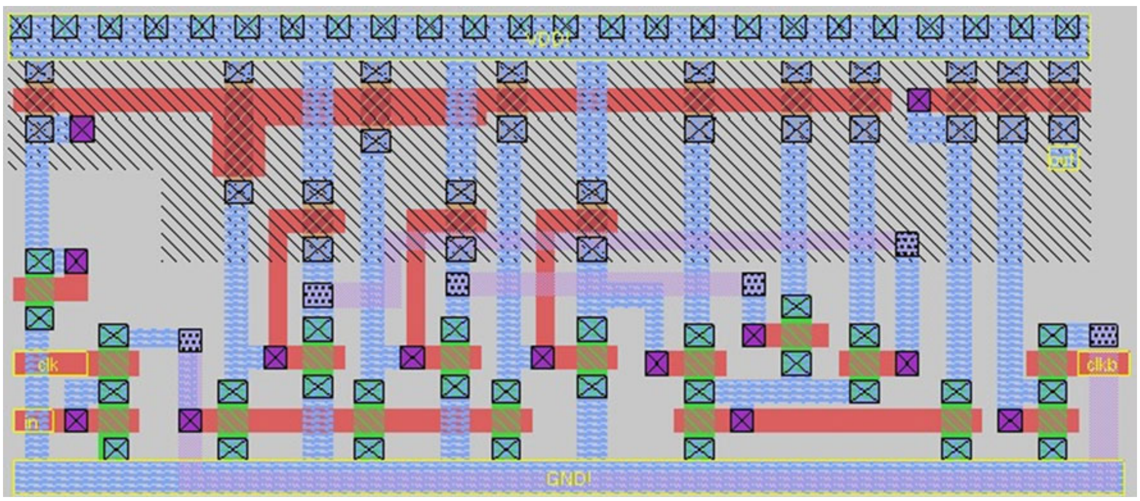


Fig. 5 The IC layout of the 8-valued latch circuit in Ref. [5]

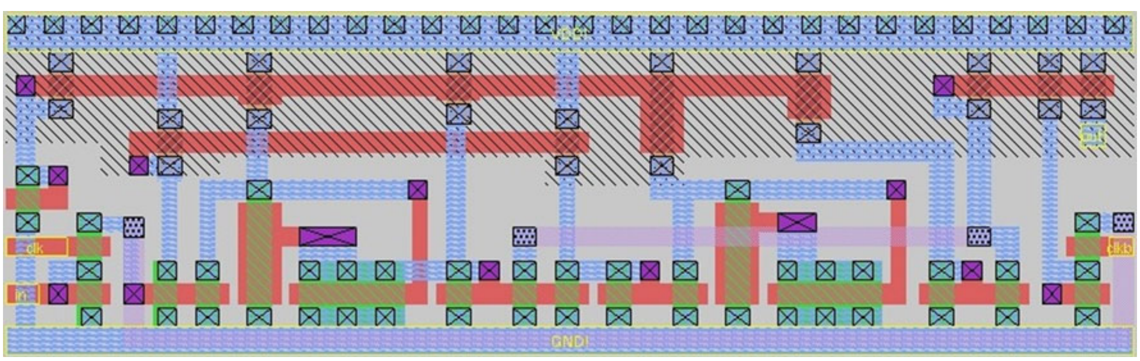


Fig. 6 The IC layout of the 8-valued latch circuit in this paper

The number of Q outputs (I_{out}) can be increased by adding more current mirrors to the final stage.

The 4-valued AB flip-flop circuit is simulated using H-Spice, UMC 0.18um technology, level 49 transistor parameters and 1.8 V power supply voltage. Applied input signals and the resulting simulation output are given in Fig. 4 and it is fully compatible with Table 1.

The new latch/restorer circuit is optimized for new application to obtain smooth transitions. Comparison of the previous [5] and the new circuit is given in Table 2. The layouts of 8-valued implementations are given in Figs. 5, 6 respectively. The new circuit uses 26 transistor for 4-valued implementation and 38 transistors for 8-valued multiple-level implementation. The previous latch circuit needs 29 transistors for 4-valued implementation and 53 transistors for 8-valued implementation. Although there is a slight advantage in terms of transistor count and the area for 4-valued circuits, but, the most important advantage of the new circuit is reducing spikes during the level transitions, which can be clearly seen in Figs. 9, 10. However, the area advantage also becomes evident in 8-valued circuit implementations.

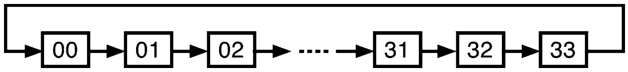


Fig. 7 Counting sequence for 2-digit modulo-16 counter

circuit may be built as shown in Fig. 8. Although the output waveforms show the correct counting sequence, the waveform has large spikes during the transitions in the first circuit given in Ref. [5]. The number of transistors and the spikes are highly reduced with the new restorer-latch circuit presented here.

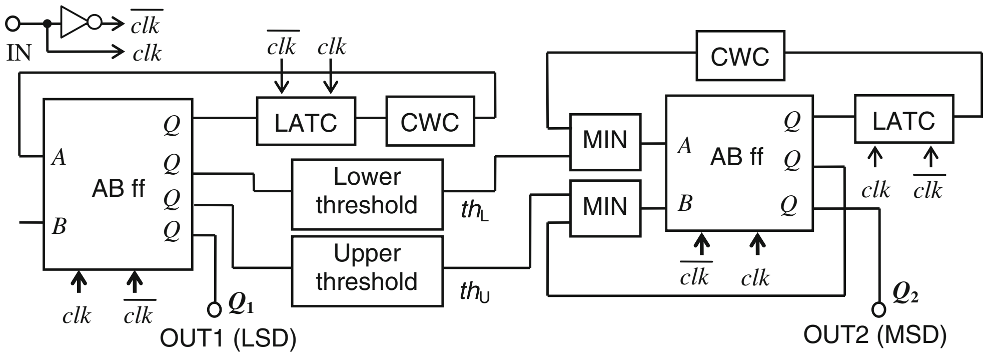


Fig. 8 The block diagram of the 2-digit modulo-16 counter

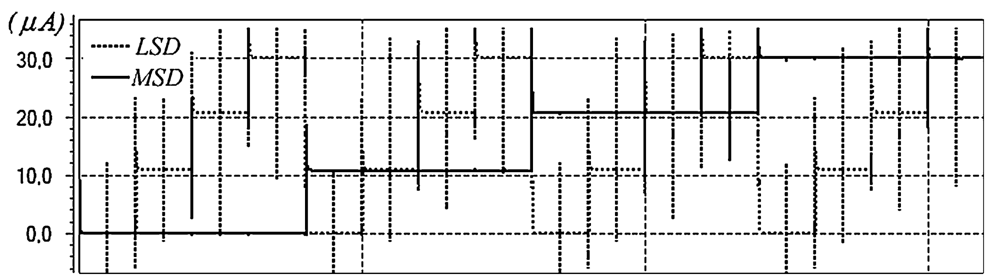


Fig. 9 Outputs of 2-digit modulo-16 counter with the restorer-latch circuit given in Ref. [5]

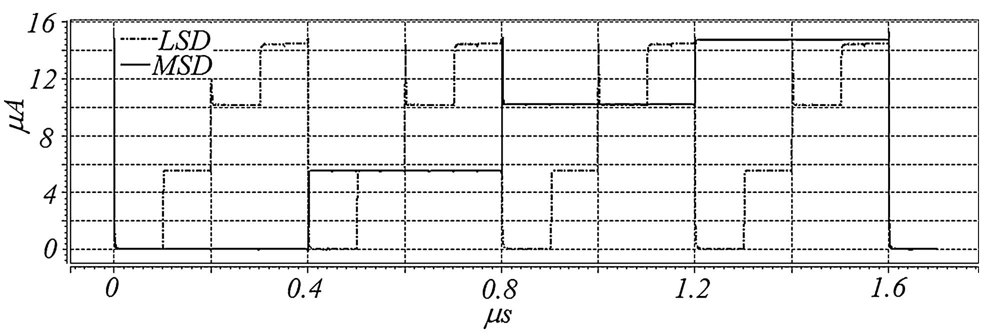


Fig. 10 Outputs of 2-digit modulo-16 counter with the new restorer-latch circuit

3 Counter circuit

In order to show the usefulness of the proposed AB flip-flop, 2-digit modulo-16 counter is designed. The counting sequence is given in Fig. 7. The counter may be realized by either using two 4-valued AB flip-flops or a single 8-valued AB flip-flop. But it is necessary to use at least three D-type flip-flops if the voltage mode binary realization were used. Figure 8 shows 4-valued realization by using two AB flip flops.

Using this counting sequence and state transition table of the AB flip-flop, the next-state equations of the *A* and *B* inputs can be obtained by inspection and the counter

All the simulations are performed by using H-Spice, UMC 0.18 μm technology. Level 49 transistor parameters are used.

4 Conclusions

In this study, a new version of the current-mode, multi-valued sequential flip-flop circuit and its application to a synchronous 2-digit modulo-16 up counter are presented. The new circuit uses fewer transistors than the previously published flip-flop circuit and the output waveforms of the new flip-flop and counter circuit does not have very high spikes during the transitions as the previous version. The radix of the circuit is taken to be 4 in these applications, but it can be increased to 8 with minor modifications. It is not very useful to use more than 8-levels since the noise margin becomes very small.

Designing equivalent circuits in binary logic rather than the multiple-valued logic requires approximately 60 % increase in transistor count and 40 % increase in the area. On the other hand, current-mode multi-valued circuits have constant current consumption, regardless of the switching activity, which makes the power consumption higher than the binary circuits.

Multi-valued logic design is still an open area, especially the sequential design part. Unfortunately there are not available algorithms or methods for the simplification of multilevel logic equations and design of sequential circuits. This study is just a step to that open area and needs improvements in circuit level and extended system level implementation.

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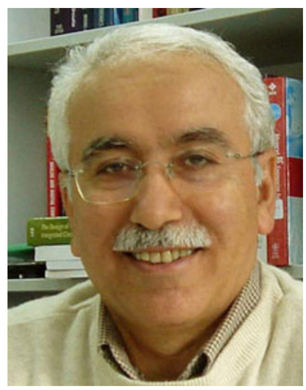
Fatma Sarica Fatma Sarica has received the B.S. degree in Electronics and Communication Engineering from Istanbul Technical University in 2001 and got her M.Sc. degree in 2004 from Bogazici University. She is currently a Ph.D. candidate in Bogazici University and expected complete her work by 2012. Her research area is mainly focused on VLSI design and implementation of multiple-valued logic circuits.



Avni Morgül Avni Morgül has been graduated from Istanbul Technical University in 1970 and got his Ph.D. degree in 1981 from the same university. He joined Bogazici University after a one year Post doc. research in the University of Edinburgh, Scotland, and he had been a full time academic staff there, until 2008. He is the Head of Electronics and Communications Department of Beykent University in Istanbul, Turkey, since then. He worked as a consultant and directed the research in R&D departments of some companies manufacturing satellite TV receivers, RF equipment and radar systems. Professor Morgül's research is concentrated on high frequency, microwave and satellite communication electronics, analog and digital IC design, implementation of multivalued logic circuits. He is member of IEEE, IET, Chamber or Turkish Electrical Engineers (EMO), Turkish Radio Amateurs Society (TRAC). Dr. Morgül is married and has 4 children. He likes swimming, playing table tennis, taking photographs and listening classical music.