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New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA

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Abstract In this paper, a new active element called voltage differencing inverting buffered amplifier (VDIBA) is presented. Using single VDIBA and a capacitor, a new resistorless voltage-mode (VM) first-order all-pass filter (APF) is proposed, which provides both inverting and non-inverting outputs at the same configuration simultaneously. The pole frequency of the filter can be electronically controlled by means of bias current of the internal trans-conductance. No component-matching conditions are required and it has low sensitivity. In addition, the parasitic and loading effects are also investigated. By connecting two newly introduced APFs in open loop a novel second-order APF is proposed. As another application, the proposed VM APF is connected in cascade to a lossy integrator in a closed loop to design a four-phase quadrature oscillator. The theoretical results are verified by SPICE simulations using TSMC 0.18 μm level-7 CMOS process parameters with ±0.9 V supply voltages. Moreover, the behavior of the proposed VM APF was also experimentally measured using commercially available integrated circuit OPA860 by Texas Instruments.

Keywords Analog signal processing · All-pass filter · Electronically tunable circuit · Four-phase quadrature oscillator · Loading effect · Resistorless filter · Voltage-mode · Voltage differencing inverting buffered amplifier (VDIBA)

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1 Introduction

All-pass filters are used to correct the phase shifts caused by analog filtering operations without changing the amplitude of the applied signal. In the literature, although many first-order voltage-mode (VM) all-pass filters (APFs) were proposed (e.g. [1–23] and references cited therein), only circuits in [3–23] are resistorless i.e. no external resistor is required and electronically tunable simultaneously. Table 1 summarizes the advantages and disadvantages of previously reported VM APFs in [1–23]. It is important to mention that we do not rule out the importance of the discussion on all the given criterions in the Table 1, however, in this part we concentrate on comparison of each circuit only regarding their tunability feature. In general, the tunability feature of circuits is solved in four different ways. After the current-controlled conveyor (CCCII) was introduced [24], a new period has been opened with respect to electronic tunability in the analog filter design. Here the intrinsic input resistance of the CCCII and other versatile analog building blocks (ABBs) is controlled via an external current or voltage, as shown in [3–11]. Similarly, the output resistance control of the CMOS inverting amplifier is demonstrated in [12]. Another

Table 1 Comparison with previously published VM all-pass filters

Reference	ABB type[b]	No. of ABBs	No. of transistors[c]	No. of *R*/*C*	Tunability	No passive/active matching constraints	Type of response	Technology (μm)	Power supplies (V)
[1][a]	DVCC+	1	12	1/2	No	No	Non-inverting	0.5	±2.5
[2]	DVCC+	2	24	1/1	No	Yes	Both[g]	0.18	±1.5
[3]	CCCII−	2	34[d]	0/1	Yes	No	Inverting	BJT	±2.5
[4]	CCCII+/OpAmp	2	14[d]/D	0/2	Yes	No	Inverting	BJT/D	±2.5/−
[5][a]	CCCII+/OpAmp	3	28[d]/D	0/2	Yes	No	Inverting	BJT/D	±2.5/−
[6]	DVCC−	2	26	0/1	Yes	Yes	Non-inverting	0.5	±2.5
[7]	C-CDBA	3	65[d]	0/1	Yes	No	Inverting	0.35	±2.5
[8]	CCCII+/DV-VB	2	D	0/1	Yes	Yes	Non-inverting	D	–
[9]	C-ICDBA	1	30[d]	0/1	Yes	Yes	Non-inverting	0.35	±2.5
[10]	CC-VCIII−	1	22[d]	0/1	Yes	Yes	Non-inverting	0.35	±2.5
[11]	CCCII+/FD-OpAmp	2	13[d]/D	0/1	Yes	Yes	Both simultaneously	BJT/D	±1.5
[12]	IUGA	1	5[d]	0/1	Yes	Yes	Inverting	0.35	±1.5
[13]	DDCC	2	34[f]	0/1	Yes	Yes	Non-inverting	0.35	±1.5
[14]	UVC	1	41[d,f]	0/1	Yes	Yes	Both simultaneously	0.35	±2.5
[15]	UVC	1	44[d,f]	0/1	Yes	No	Both simultaneously	0.35	±2.5
[16]	IVB	2	5[f]	0/1	Yes	Yes	Both[g]	0.18	±0.9
[17]	VD-DIBA	1	D	0/1	Yes	Yes	Non-inverting	D	–
[18]	OTA	1	D	0/2	Yes	No	Inverting	D	–
[19]	OTA	3	12[d]	0/1	Yes	Yes	Non-inverting	0.5	±3
[20]	CCCDTA	1	25[d]	0/1	Yes	No	Inverting	BJT	±1.5
[21]	UVC/OTA	2	33[d,e]	0/1	Yes	Yes	Both simultaneously	BJT	±2
[22]	MO-CCCCTA	1	29[d]	0/1	Yes	No	Non-inverting	BJT	±2
[23]	OTA/UGDA	2	22[d]	0/1	Yes	Yes	Inverting	0.35	±2.5
This work	VDIBA	1	6[d]	0/1	Yes	Yes	Both simultaneously	0.18	±0.9

– Not mentioned; *D* Discrete ICs used: [4] μA741; [5] OP-27; [8] and [17] OPA860 and AD8130; [11] LTC6403-1; [18] CA3080E

[a] Considered circuit: [1] simulated circuit '8'; [5] simulated circuit shown in Fig. 4

[b] Refer Sect. 8 for nomenclature of the ABBs

[c] Minimal configuration assumed

[d] Ideal current sources assumed

[e] Ideal voltage buffers assumed

[f] Including MOSFETs replacing voltage-controlled resistor

[g] By interchanging the resistor and capacitor

technique is given in [13–16], where the appropriate resistor is replaced by MOSFET-based voltage-controlled resistor. In recently presented voltage differencing-differential input buffered amplifier (VD-DIBA)-based VM APF [17] and in other circuits [18–23] the tunability property of the operational transconductance amplifier (OTA) [25] is used to shift the phase response of the circuits. In fact, although the active element VD-DIBA, which belongs to the group of 'voltage differencing' elements [26], is new, it is composed of an OTA and a unity gain differential amplifier (UGDA), an interconnection that is done in [23] separately.

This paper reports another 'voltage differencing' element, namely the voltage differencing inverting buffered amplifier (VDIBA), which has simpler active structure than VD-DIBA [17], because there is no need of a difference amplifier at its second stage. Moreover, the proposed resistorless first-order VM APF using single VDIBA and one capacitor provides both inverting and non-inverting all-pass responses simultaneously at two different output

nodes. It is worth mention that only circuits in [11, 14, 15], and [21] have such exclusive advantage. To validate the applicability of the new APF, a second-order APF and four-phase quadrature oscillator circuits are presented. SPICE simulation and experimental measurement results are included to support the theory.

2 Circuit description

The voltage differencing inverting buffered amplifier (VDIBA) is a new four-terminal active device with electronic tuning, which circuit symbol and behavioral model are shown in Fig. 1(a), (b), respectively. From the model it can be seen that the VDIBA has a pair of high-impedance voltage inputs $v+$ and $v-$, a high-impedance current output z, and low-impedance voltage output $w-$. The input stage of VDIBA can be easily implemented by a differential-input single-output OTA, which converts the input voltage to output current that flows out at the z terminal. The output stage can be formed by unity-gain IVB. Since both stages can be implemented by commercially available integrated circuits (ICs), and moreover it contains OTA, the introduced active element is attractive for resistorless and electronically controllable circuit applications.

Using standard notation, the relationship between port currents and voltages of a VDIBA can be described by the following hybrid matrix:

$$\begin{bmatrix} I_{v+} \\ I_{v-} \\ I_z \\ V_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -\beta & 0 \end{bmatrix} \begin{bmatrix} V_{v+} \\ V_{v-} \\ V_z \\ I_{w-} \end{bmatrix}, \tag{1}$$

where g_m and β represent transconductance and non-ideal voltage gain of VDIBA, respectively. The value of β in an ideal VDIBA is equal to unity.

The CMOS implementation of the VDIBA is shown in Fig. 2. The circuit is composed of an active loaded differential pair (transistors M_1–M_4) cascaded with a unity-gain inverting voltage buffer (matched transistors M_5 and M_6). The input/output terminal resistances of the CMOS VDIBA shown in Fig. 2 can be found as:

$$R_{ow-} \cong \frac{1}{g_{m5}} \| r_{o6}, \tag{2a}$$

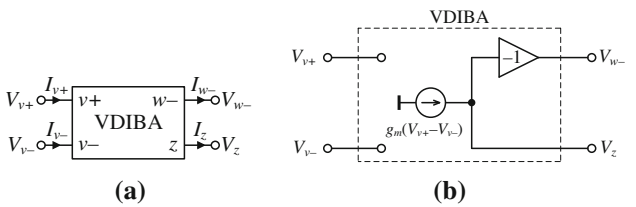


Fig. 1 **a** Circuit symbol and **b** behavioral model of VDIBA

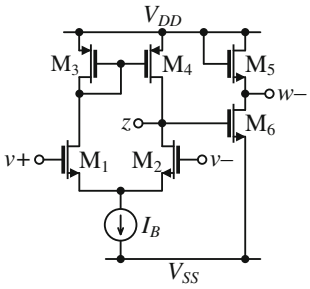


Fig. 2 CMOS implementation of VDIBA

$$R_{oz} \cong r_{o4} \| r_{o2}, \tag{2b}$$

$$R_{v+} = R_{v-} \cong \infty, \tag{2c}$$

where g_{mi} and r_{oi} represent the transconductance and output resistance of the i-th transistor, respectively. From Eqs. (2a)–(2c) it can be seen that while the output terminal ($w-$) can exhibit low resistance by selecting large transistor M_5 (and M_6 due to the matching condition requirement), the input terminals ($v+$ and $v-$) as well as the z terminal have high resistances.

The proposed new first-order VM APF using single active element and a capacitor is shown in Fig. 3. Considering an ideal VDIBA ($\beta = 1$), routine analysis of the circuit gives the following transfer functions (TFs):

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{sC - g_m}{sC + g_m}, \tag{3a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{sC - g_m}{sC + g_m}. \tag{3b}$$

The phase responses of the TFs (3a) and (3b) are calculated as:

$$\varphi_1(\omega) = 180^\circ - 2\tan^{-1}\left(\frac{\omega C}{g_m}\right), \tag{4a}$$

$$\varphi_2(\omega) = -2\tan^{-1}\left(\frac{\omega C}{g_m}\right). \tag{4b}$$

Hence, from the above equations it can be seen that the proposed configuration can simultaneously provide phase shifting both between π (at $\omega = 0$) to 0 (at $\omega = \infty$) and 0 (at $\omega = 0$) to $-\pi$ (at $\omega = \infty$), at output terminals V_{o1} and V_{o2}, respectively.

From Eqs. (3a) and (3b), the pole frequency ω_p is expressed as:

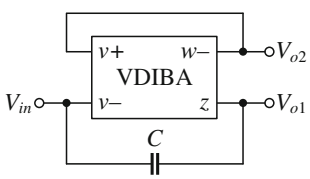


Fig. 3 Proposed resistorless dual-output VM all-pass filter with electronic tuning

$$\omega_p = \frac{g_m}{C}. \tag{5}$$

Note that the ω_p can be easily tuned by adjusting the transconductance of VDIBA. The pole sensitivities of the proposed circuit are given as:

$$S_{g_m}^{\omega_p} = -S_C^{\omega_p} = 1, \tag{6}$$

which are not higher than unity in magnitude.

3 Non-ideal and parasitic effects analysis

Taking into account the non-ideal voltage gain β of the VDIBA, TFs in Eqs. (3a) and (3b) convert to:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{sC - g_m}{sC + \beta g_m}, \tag{7a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\beta T_1(s), \tag{7b}$$

and non-ideal phase responses from TFs (7a) and (7b) are given as:

$$\varphi_1(\omega) = 180^\circ - \tan^{-1}\left(\frac{\omega C}{g_m}\right) - \tan^{-1}\left(\frac{\omega C}{\beta g_m}\right), \tag{8a}$$

$$\varphi_2(\omega) = -\tan^{-1}\left(\frac{\omega C}{g_m}\right) - \tan^{-1}\left(\frac{\omega C}{\beta g_m}\right). \tag{8b}$$

Consequently, the pole frequency of the presented filter is found as:

$$\omega_p = \frac{\beta g_m}{C}. \tag{9}$$

From Eq. (9) it can be realized that the single non-ideality of the VDIBA slightly affects the filter parameters, however, this influence can be easily compensated by the transconductance of the VDIBA.

For a complete analysis of the circuit in Fig. 3, it is also important to take into account parasitic effects of the VDIBA. Detailed numerical simulation of the filter indicated that the main source of non-idealities is due to the finite output admittance Y_z of the involved OTA stage of the VDIBA. Considering that this admittance is modeled by a parallel RC circuit consisting of a non-ideal output resistance R_z and a non-ideal output capacitance C_z and assuming the non-zero output resistance R_{w-} of the $w-$ terminal, the matrix relationship of (1) changes as follows:

$$\begin{bmatrix} I_{v+} \\ I_{v-} \\ I_z \\ V_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & sC_z + \frac{1}{R_z} & 0 \\ 0 & 0 & -\beta & R_{w-} \end{bmatrix} \begin{bmatrix} V_{v+} \\ V_{v-} \\ V_z \\ I_{w-} \end{bmatrix}. \tag{10}$$

Re-analysis of the proposed filter in Fig. 3, the ideal TFs (3a) and (3b) turns to be:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{C}{C + C_z} \cdot \frac{s - g_m/C}{s + \left(\beta g_m + \frac{1}{R_z}\right) \Big/ (C + C_z)}, \tag{11a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\beta T_1(s). \tag{11b}$$

From Eq. (11a) it is noted that the filter has a constant magnitude slightly lower than unity, which is equal to $C/(C + C_z)$ provided that the following condition is met:

$$\beta = 1 + \frac{C_z}{C} - \frac{1}{g_m R_z}. \tag{12}$$

Therefore, by replacing the involved unity gain IVB stage with an adjustable amplifier with the prescribed gain in Eq. (12), the above discussed non-ideal effects can be fully compensated, at the cost of having a constant magnitude slightly lower than unity.

At this point, we want to note an interesting and useful property of the proposed filter. The filter has a very accurate unit magnitude at very low and very high frequencies. To be specific, owing to the fact that there is a capacitor connected between the filter's input and output terminals and the capacitor behaves as a short-circuit element at the very high frequencies, the filter has very accurate unit magnitude in this frequency region, inherently. It is also worth mention that the circuit in [12] has an identical feature.

On the other hand, at very low frequencies, the filter magnitude approximates to:

$$\left.\frac{V_{o1}}{V_{in}}\right|_{s=0} = \frac{-g_m R_z}{1 + \beta g_m R_z}, \tag{13}$$

which is the gain of the feedback loop in Fig. 3. This gain also is very close to unity since typical value of R_z is much larger than $1/g_m$.

From Eqs. (11a) and (11b) the non-ideal zero ω_z and pole ω_p frequencies including parasitics can be calculated as:

$$\omega_z = \frac{g_m}{C}, \tag{14a}$$

$$\omega_p = \frac{\beta g_m + \frac{1}{R_z}}{C + C_z}. \tag{14b}$$

From Eq. (14b) it is clear that pole ω_p frequency is affected by the parasitics and non-idealities of the active element used, however, they can be minimized by:

(i) making the β very close to unity and/or,
(ii) choosing $C \gg C_z$ and/or,
(iii) choosing $g_m \gg 1/R_z$.

4 Loading effect analysis

In addition, the loading effects at both output terminals are also worth to be investigated. Assuming equal load $R_{L1} = R_{L2} = R_L$ and considering the non-idealities and parasitics of the VDIBA in Eq. (10), straightforward analysis gives the following voltage transfer functions:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{(sC - g_m)(R_L + R_{w-})R_z}{s(CR_LR_z + C_zR_LR_z + CR_zR_{w-} + C_zR_zR_{w-}) + R_L + R_{w-} + R_z + \frac{R_zR_{w-}}{R_L} + \beta R_LR_zg_m}, \tag{15a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\beta T_1(s). \tag{15b}$$

Assuming $R_L \gg R_{w-}$, TFs in Eqs. (15a) and (15b) turn to:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{sC - g_m}{s(C + C_z) + \beta g_m + \frac{1}{R_z} + \frac{1}{R_L}}, \tag{16a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\beta T_1(s). \tag{16b}$$

Finally, considering $R_z \gg R_L$, TFs in Eqs. (16a) and (16b) change to:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{sC - g_m}{s(C + C_z) + \beta g_m + \frac{1}{R_L}}, \tag{17a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\beta T_1(s), \tag{17b}$$

and hence, the pole ω_p' frequency in Eq. (14b) turns to be:

$$\omega_p' = \frac{\beta g_m + \frac{1}{R_L}}{C + C_z}. \tag{18}$$

The active and passive sensitivities of the ω_p' can be calculated as:

$$S_C^{\omega_p'} = -\frac{1}{1 + \frac{C_z}{C}}, \quad S_{C_z}^{\omega_p'} = -\frac{1}{1 + \frac{C}{C_z}}, \quad S_\beta^{\omega_p'} = S_{g_m}^{\omega_p'} = \frac{1}{1 + \frac{1}{\beta g_m R_L}}, \quad S_{R_L}^{\omega_p'} = -\frac{1}{1 + \beta g_m R_L}. \tag{19}$$

Additionally, using (9) in (18), between ω_p' and ω_p the following relationship can be calculated:

$$\omega_p' = \frac{1}{R_L(C + C_z)} + \frac{C}{C + C_z}\omega_p. \tag{20}$$

To illustrate the effect of the load, Eq. (20) was further investigated, as it is shown in Fig. 4. The calculation has been done for three different values of $R_L = \{1;\ 10;\ 100\}$ kΩ while keeping the C and C_z values identical with in the Sect. 5 listed once. From Fig. 4 it can be realized that for lower pole frequencies the effect of R_L on the deviation of the pole frequency from its original value becomes dominant with respect to the parasitic effect (C_z). Hence, lower values of R_L restrict the proper operation of the proposed APF at lower pole frequencies, where a phase shift of 90° must be obtained.

5 Performance verifications

5.1 Simulation results

To verify the theoretical study, the behavior of the introduced VDIBA shown in Fig. 2 has been verified by SPICE simulations with DC power supply voltages equal to $+V_{DD} = -V_{SS} = 0.9$ V. In the design, transistors are modeled by the TSMC 0.18 µm level-7 CMOS process parameters ($V_{THN} = 0.3725$ V, $\mu_N = 259.5304$ cm^2/(V·s), $V_{THP} = -0.3948$ V, $\mu_P = 109.9762$ cm^2/(V·s), $T_{OX} = 4.1$ nm) [2]. The aspect ratios of the OTA (M_1–M_4) and the IVB (M_5 and M_6) were chosen as $W/L_{(M1–M4)} = 18$ µm/1.08 µm and $W/L_{(M5,\ M6)} = 54$ µm/0.18 µm, respectively. Note that the W/L ratio of the transistors M_5 and M_6 should be selected sufficiently high to decrease the loading effect.

First of all, the performance of the VDIBA was tested by AC and DC analyses. The AC simulation results for both transconductance and voltage transfers of the VDIBA are shown in Fig. 5(a), (b), respectively. In the simulations the

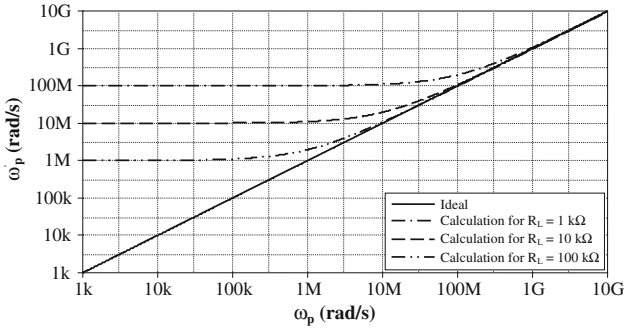


Fig. 4 ω_p' versus ω_p for different values of load

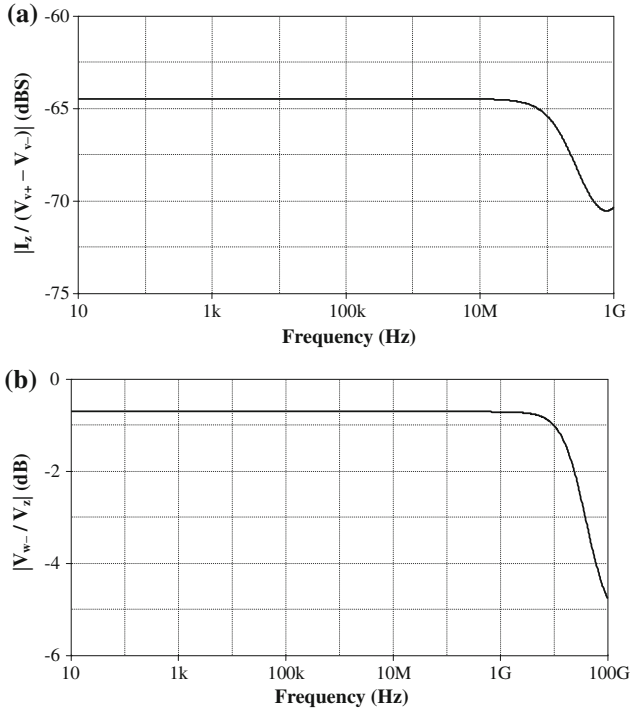


Fig. 5 AC analysis of VDIBA in Fig. 2: (**a**) transconductance gain and (**b**) voltage gain versus frequency

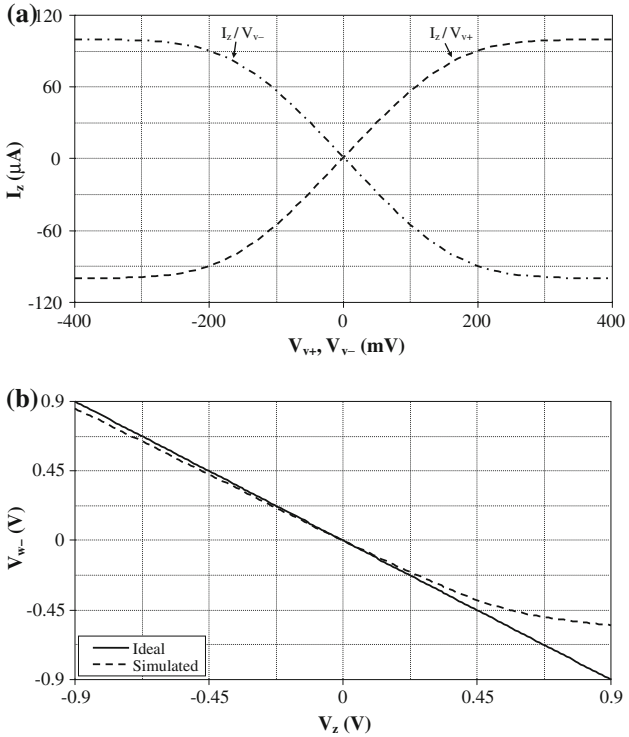


Fig. 6 DC analysis of VDIBA in Fig. 2: (**a**) I_z versus V_{v+} and V_{v-}, (**b**) V_{w-} versus V_z

bias current was selected as $I_B = 100$ μA, which results in g_m approximately equal to 600 μA/V with $f_{-3\text{dB}}$ frequency of 226.32 MHz. Subsequently, the obtained gain of the IVB voltage transfer shown in Fig. 5(b) is equal to $\beta = 0.922$ and its $f_{-3\text{dB}}$ frequency is found to be 51.93 GHz. Hence, the maximum operating frequency of the VDIBA is $f_{max} = \min\{f_\beta, f_{gm}\} \approx 226.32$ MHz. In addition, the z and $w-$ terminal parasitic capacitance and resistances were found as $C_z = 367$ fF $\| R_z = 131.93$ kΩ and $R_{w-} = 42.36$ Ω, respectively. The DC characteristics such as plots of I_z against both V_{v+} and V_{v-}, when $g_m = 600$ μA/V and DC voltage characteristic of V_{w-} against V_z for the proposed VDIBA are shown in Fig. 6(a), (b), respectively. The maximum values of terminal voltages without producing significant distortion are approximately computed as ±200 mV for the OTA and −0.9 to +0.5 V for the IVB, respectively.

In order to verify the workability of the proposed VM APF in Fig. 3, it has been further analyzed using the designed CMOS implementation of the VDIBA in SPICE software. Fig. 7(a), (b) show the ideal and simulated gain and phase responses illustrating the electronic tunability of the proposed filter. The pole frequency is varied for $f_0 \cong \{1.07; 1.84; 3.31; 5.67; 9.44\}$ MHz via the bias current $I_B = \{6; 11; 22; 45; 100\}$ μA, respectively. In all simulations the value of the capacitor C has been selected as 9.6 pF. Note that the external capacitor C appears parallel with C_{gs6} parasitic capacitance of the transistor M_6, which value is equal to 461 fF. Theoretically, therefore, its total value equal to $C \approx 10$ pF should be taken into account. Hence, considering $I_B = 100$ μA ($g_m = 600$ μA/V), the 90° phase shift is at pole frequency $f_0 \cong 9.44$ MHz, which is close to the ideal f_0 equal to 9.54 MHz. The obtained gains for the first and the second outputs are equal to 1.075 and 0.987, respectively. The small discrepancy between ideal and simulated gain results can be attributed to the non-ideal voltage gain β and the non-idealities of the active element used and hence in practice a precise design of the VDIBA should be considered to alleviate the non-ideal effects. Using the INOISE and ONOISE statements, the input and output noise behavior for both responses with respect to frequency have also been simulated, as it is shown in Fig. 8(a), (b). The equivalent input/output noises for the first and the second responses at operating frequency ($f_0 \cong 9.44$ MHz) are found as 6.02/6.39 and 6.03/5.91 nV/$\sqrt{\text{Hz}}$, respectively.

To illustrate the time-domain performance, transient analysis is performed to evaluate the voltage swing capability and phase errors of the filter as it is demonstrated in Fig. 9 while keeping the $I_B = 100$ μA ($g_m = 600$ μA/V) and $C = 9.6$ pF. Note that the output waveforms are close to the input one. The total harmonic distortion (THD) variations with respect to amplitudes of the applied sinusoidal input voltages at 9.44 MHz are shown in Fig. 10. An input with the amplitude of 100 mV yields THD values of 1.81 % and 1.86 % for the first and second output of the proposed filter, respectively. In addition, the +90° and −90° phase

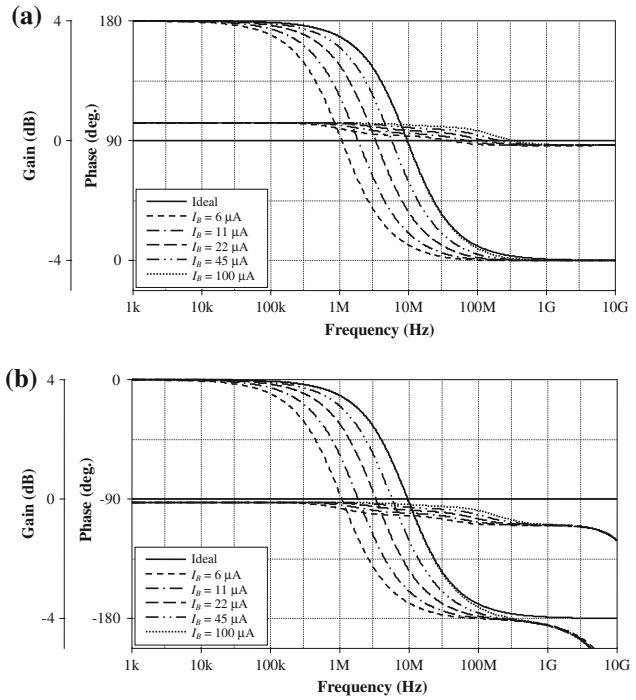


Fig. 7 Electronical tunability of the pole frequency by the bias current I_B: (**a**) inverting, (**b**) non-inverting VM first-order all-pass filter responses

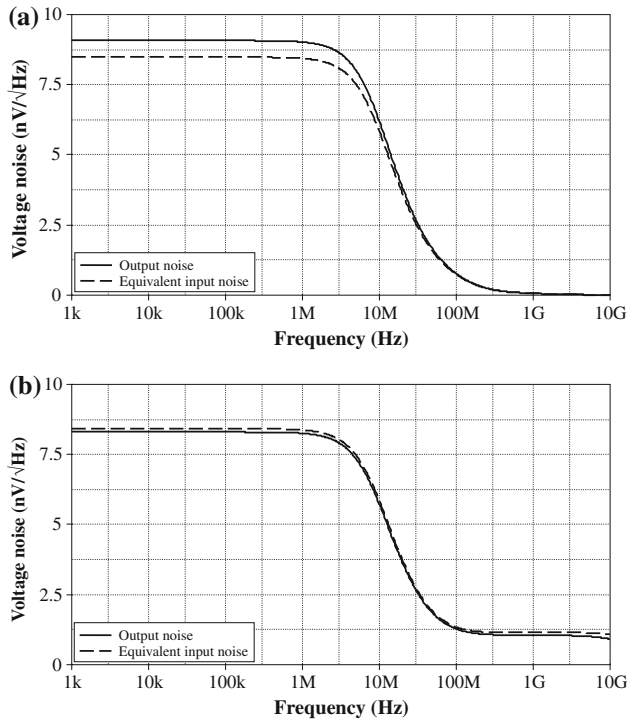


Fig. 8 Input and output noise variations for (**a**) V_{o1} and (**b**) V_{o2} versus frequency

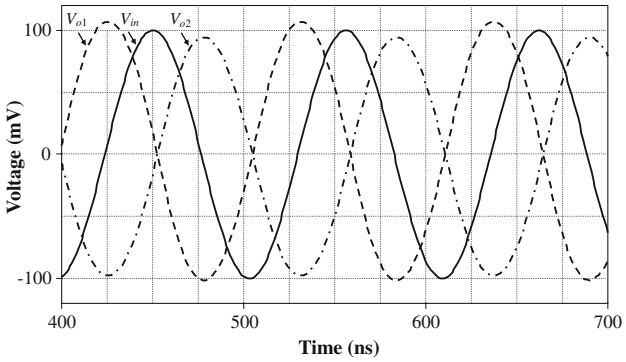


Fig. 9 Time-domain responses of the proposed all-pass filter at 9.44 MHz

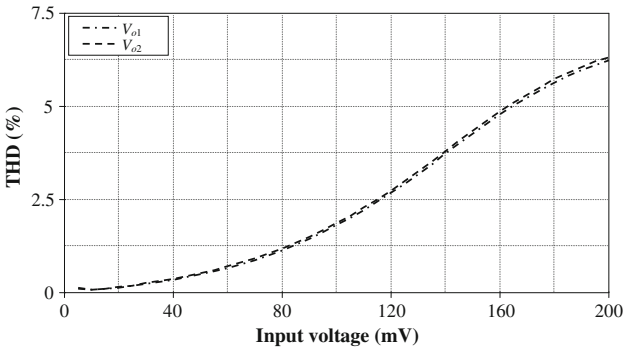


Fig. 10 THD variation of the proposed all-pass filter for both responses against applied input voltage at 9.44 MHz

shifts in the first and the second outputs against the input at pole frequency 9.44 MHz are also illustrated in the Lissajous patterns shown in Fig. 11(a), (b), respectively. The total power dissipation of the circuit is found to be 10.5 mW.

5.2 Measurement results

In order to confirm the theoretical results, the behavior of the proposed APF has also been verified by experimental measurements using network-spectrum analyzer Agilent 4395A, function generator Agilent 33521A, and four-channel oscilloscope Agilent DSOX2014A. In measurements the VDIBA was implemented based on the structure illustrated in Fig. 12 using readily available ICs OPA860 [27] by Texas Instruments. The DC power supply voltages were equal to ± 5 V and the resistor R_{ADJ} (see [27]) was chosen as 270 Ω. The OPA860 contains the so-called 'diamond' transistor (DT) and fast voltage buffer (VB). In the input stage, in order to increase the linearity of collector current versus input voltage V_d, the DT_1 is complemented with degeneration resistor $R_G \gg 1/g_{mT}$, added in series to the emitter, where the g_{mT} is the DT transconductance. Then the total transconductance decreases to the approximate value $1/R_G$ [17]. The DT_2 together with R_E and R_C represent the IVB

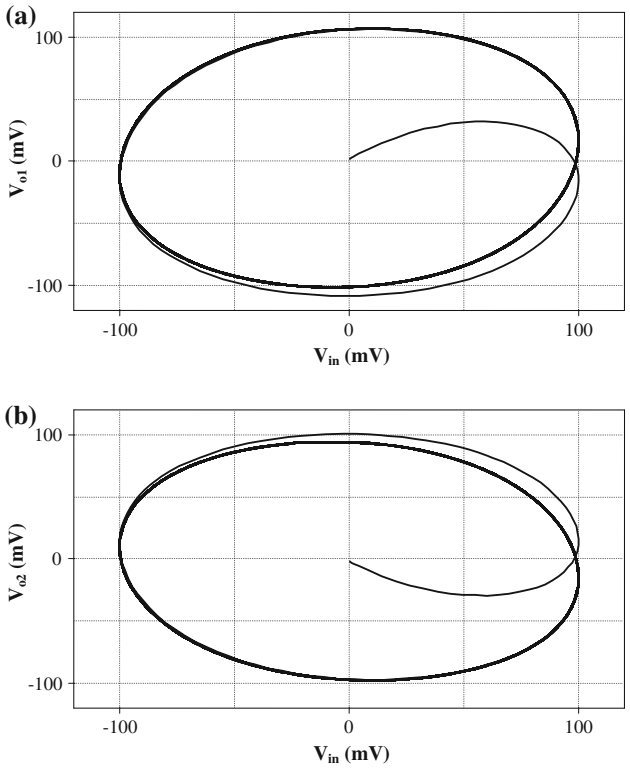


Fig. 11 Lissajous patterns showing (**a**) +90° phase shift of V_{o1} and (**b**) −90° phase shift of V_{o2} against input voltage at 9.44 MHz

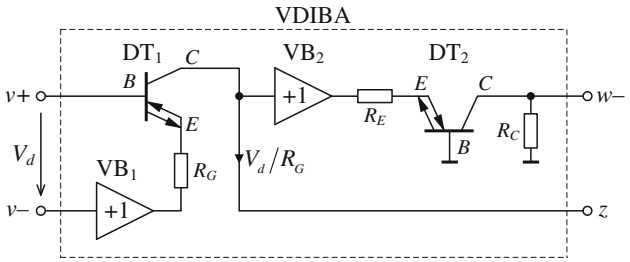


Fig. 12 VDIBA implementation by two Texas Instruments ICs OPA860

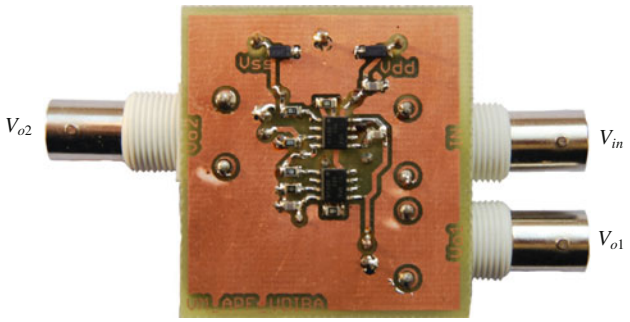


Fig. 13 The PCB prototype of the proposed all-pass filter based on VDIBA implementation from Fig. 12

with the gain of the amplifier calculated as $\beta \cong -R_C/R_E$ [17]. The input stage and the IVB are separated by the VB_2.

The developed PCB (printed circuit board) is shown in Fig. 13. In all measurements the values of the resistors R_E and R_C have been chosen as 157 and 172 Ω to improve the gain of the IVB, respectively. In the proposed filter, the value of the capacitor C has been selected as 150 pF and value of the degeneration resistor R_G was set to 1 kΩ. In this case the 90° phase shift is at $f_0 \cong 1$ MHz and the results are shown in Fig. 14(a), (b), respectively. The time-domain responses of the measured APF are shown in Fig. 15 in which a sine-wave input of 500 mV amplitude and frequency of 1 MHz was applied to the filter. Subsequently, the Fourier spectrum of both output signals, showing a high selectivity for the applied signal frequency, is shown in Fig. 16(a), (b), respectively. The THDs at this frequency are found as 1.19 % and 1.11 % for the first and second output of the proposed filter, respectively.

From the simulation results and experimental measurements it can be seen that the final solution is in good agreement with the theory.

6 Applications of the proposed filter

In this section, the proposed VM APF in Fig. 3 is used as basic building block of more complex circuits. To the best of the authors' knowledge, the given applications based on the new APF topology are also new and unpublished.

6.1 Second-order all-pass filter

To illustrate the utility of the proposed first-order APF, a new dual-output second-order all-pass filter is proposed by connecting in cascade two APFs in an open loop. The proposed circuit in Fig. 17 only employs two VDIBAs and two capacitors. Taking into account the non-ideal voltage gain β_i ($i = 1, 2$) of VDIBAs, routine analysis gives the following voltage TFs:

$$T_3(s) = \frac{V_{o1}}{V_{in}} = -\beta_1 \frac{s^2 - s\left(\frac{g_{m1}}{C_1} + \frac{g_{m2}}{C_2}\right) + \frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\left(\frac{\beta_1 g_{m1}}{C_1} + \frac{\beta_2 g_{m2}}{C_2}\right) + \frac{\beta_1\beta_2 g_{m1}g_{m2}}{C_1C_2}}, \tag{21a}$$

$$T_4(s) = \frac{V_{o2}}{V_{in}} = -\beta_2 T_3(s). \tag{21b}$$

Hence, the designed second-order APF configuration can simultaneously provide phase shifting both between $+\pi$ (at $\omega = 0$) to $-\pi$ (at $\omega = \infty$) and 0 (at $\omega = 0$) to -2π (at $\omega = \infty$), at output terminals V_{o1} and V_{o2}, respectively.

From Eqs. (21a) and (21b), the angular resonance frequency (ω_0) and the quality factor (Q) are given by:

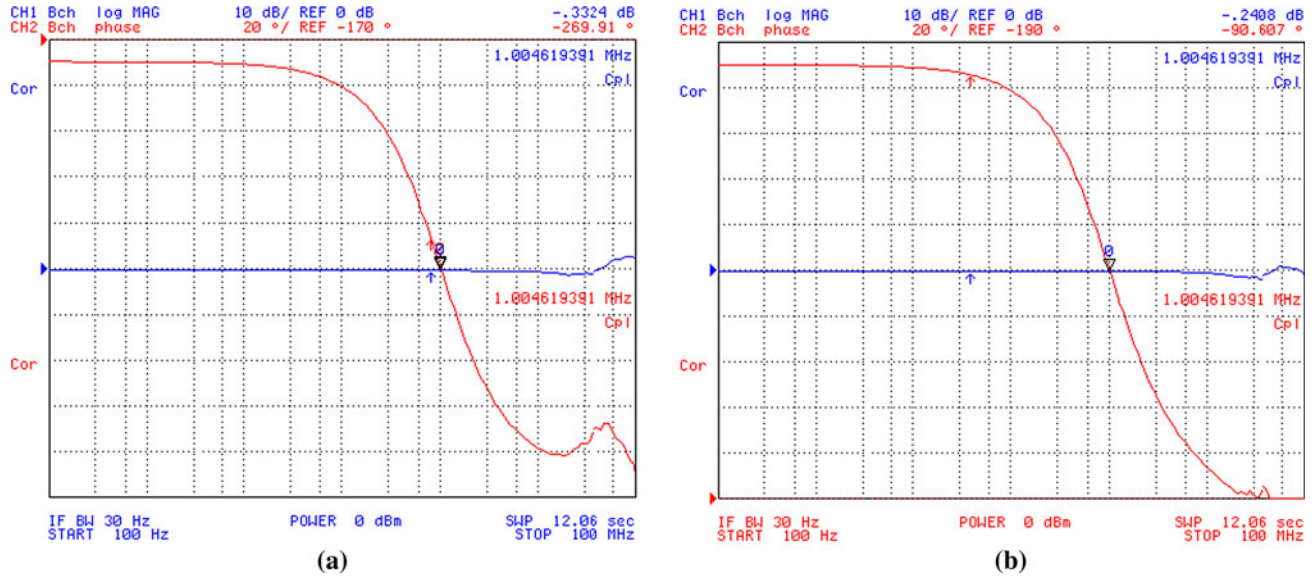


Fig. 14 Measured gain and phase characteristics of the proposed all-pass filter: (**a**) $T_1(s)$, (**b**) $T_2(s)$

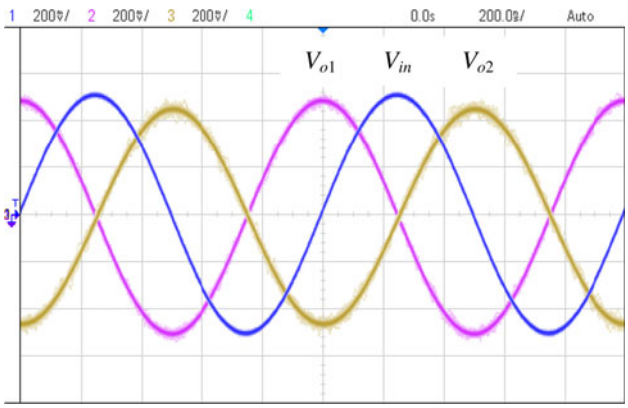


Fig. 15 Measured time-domain responses of the proposed all-pass filter at 1 MHz

$$\omega_0 = \sqrt{\frac{\beta_1\beta_2 g_{m1}g_{m2}}{C_1C_2}}, \quad Q = \frac{\sqrt{\beta_1\beta_2 g_{m1}g_{m2}C_1C_2}}{\beta_1 g_{m1}C_2 + \beta_2 g_{m2}C_1}. \tag{22}$$

From Eq. (22) it is evident that the proposed filter circuit realizes only relatively low Q values and hence the new circuit is not suitable for synthesis of higher-order filters. It may be noted that the realized ω and Q values can be changed electronically through g_{m1} and g_{m2}. However, considering equal transconductances of both VDIBAs ($g_{m1} = g_{m2}$) and constant passive elements, the Q value of the circuit in Fig. 17 is fixed. Hence, this makes the circuit good for fixed Q applications [28]. It is thus to be concluded that the new proposed circuit provides useful active-C dual-output VM second-order all-pass filtering option with minimum components and low transistor count.

The SPICE verification of the new filter is given in Fig. 18, which show the ideal and simulated gain and phase responses for both outputs. In the simulations the values of capacitors $C_1 = C_2$ have been selected as 9.6 pF with consideration of parasitic capacitance of $C_{gs6i} = 461$ fF of the transistor M_6 for ith VDIBA ($i = 1, 2$). Hence, theoretically their total value are equal to $C_1 = C_2 \approx 10$ pF. Considering $I_{B1} = I_{B2} = 100$ µA ($g_m = 600$ µA/V), the theoretical angular resonant frequency is $f_0 \cong 9.51$ MHz, whereas the simulated value is 9.32 MHz, which is 1.9 % in relative error. The THD variations with respect to amplitudes of the applied sinusoidal input voltages at 9.32 MHz are shown in Fig. 19. An input with the amplitude of 100 mV yields THD values of 1.75 % and 1.74 % for the first and second output of the proposed second-order all-pass filter, respectively.

6.2 Four-phase quadrature oscillator

As another application example, a VM four-phase quadrature oscillator is given by connecting the proposed APF in cascade to a lossy integrator in a closed loop. It is well-known that quadrature oscillators are important circuits for various communication applications, wherein there is a requirement of multiple sinusoids that are 90° phase shifted, e.g. in quadrature mixers and single-sideband modulators, or for measurement purposes in the vector generator or selective voltmeters. Here proposed new circuit shown in Fig. 20 consists of two VDIBAs, two capacitors, and a single resistor. Routine circuit analysis yields the following characteristic equation (CE):

$$\text{CE}: \quad s^2C_1C_2R + s(C_1 + C_2g_{m1}R - 2C_1g_{m2}R) + g_{m1} = 0. \tag{23}$$

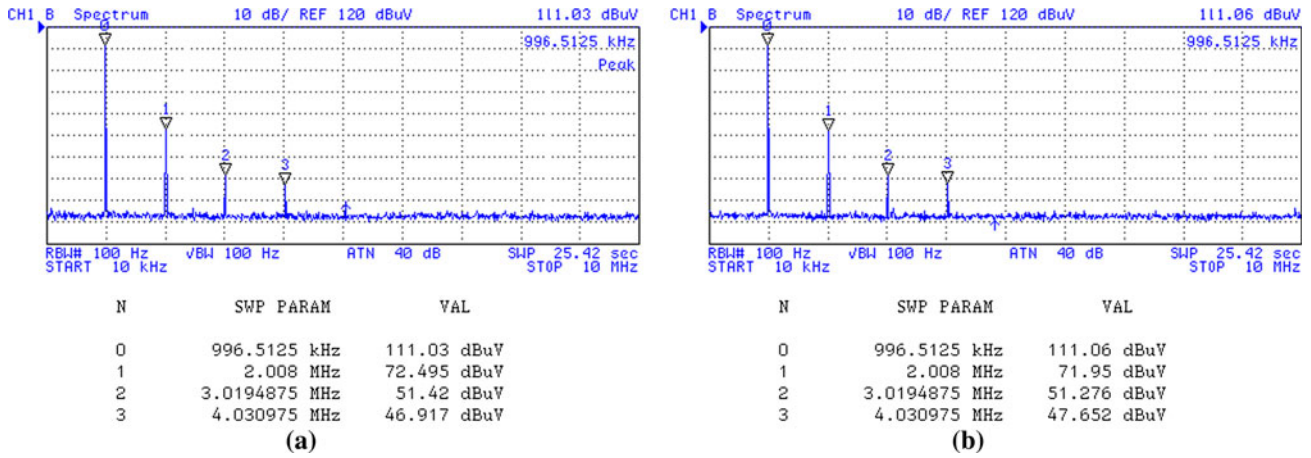


Fig. 16 Measured Fourier spectrum of the output signals: (**a**) V_{o1}, (**b**) V_{o2}

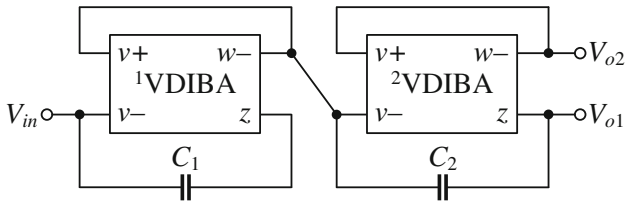


Fig. 17 Proposed resistorless dual-output VM second-order all-pass filter

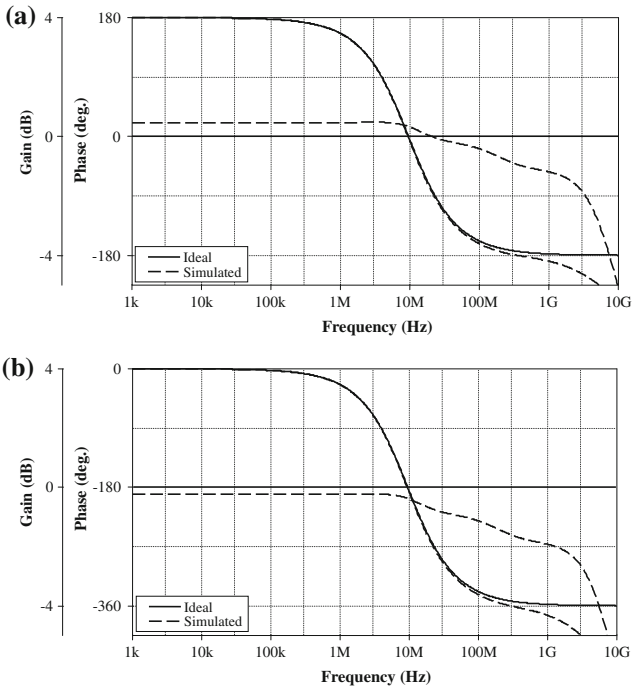


Fig. 18 Ideal and simulated gain and phase responses of the proposed VM second-order all-pass filter: (**a**) inverting (V_{o1}), (**b**) non-inverting (V_{o2}) responses

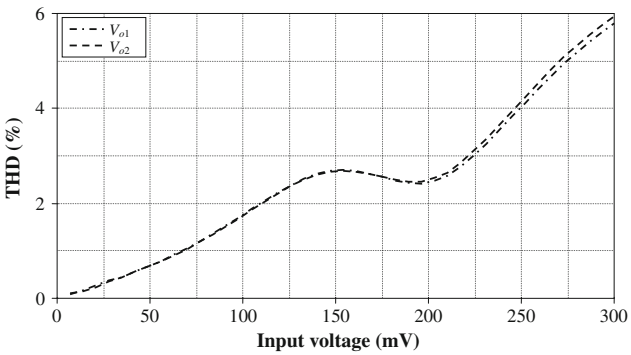


Fig. 19 THD variation of the proposed second-order all-pass filter for both responses against applied input voltage at 9.32 MHz

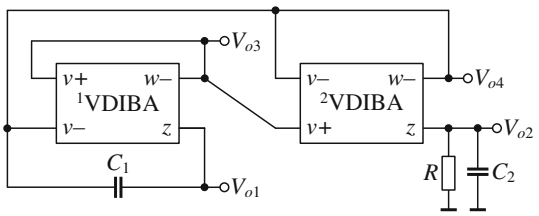
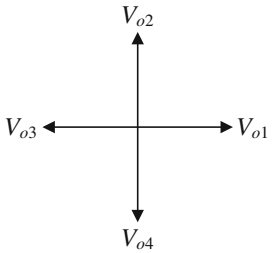


Fig. 20 Proposed VM four-phase quadrature oscillator

Fig. 21 Phasor diagram of four-phase oscillator



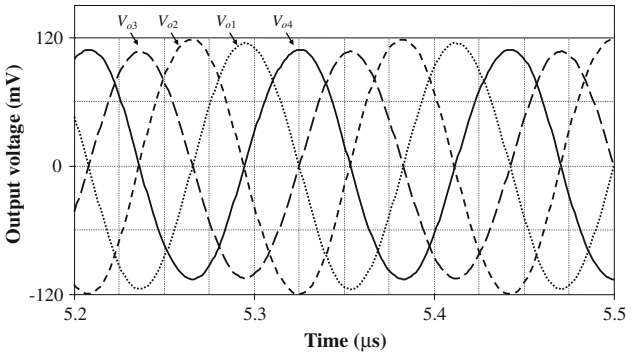


Fig. 22 Simulated output waveforms of the proposed four-phase oscillator in Fig. 20

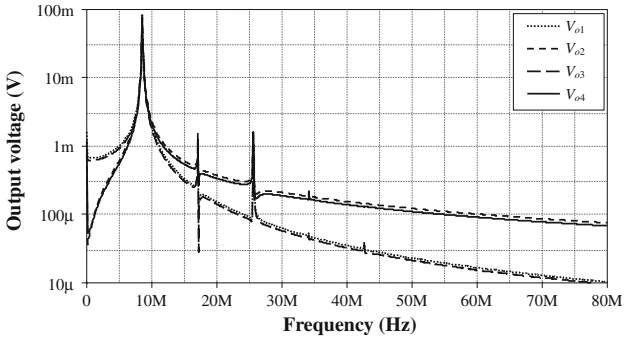


Fig. 23 Simulated frequency spectrums of outputs $V_{o1} - V_{o4}$

Table 2 THD analysis of the proposed VM four-phase quadrature oscillator

Harmonic number	Frequency (Hz)	Fourier component	Normalized component	Phase (°)	Normalized phase (°)
Output V_{o1}					
1	8.500E + 06	1.146E − 01	1.000E + 00	1.722E + 02	0.000E + 00
2	1.700E + 07	1.646E − 03	1.436E − 02	4.775E + 01	−2.966E + 02
3	2.550E + 07	9.645E − 04	8.417E − 03	4.870E + 01	−4.679E + 02
4	3.400E + 07	2.835E − 04	2.474E − 03	−3.536E + 00	−6.923E + 02
5	4.250E + 07	2.144E − 04	1.871E − 03	1.120E + 00	−8.598E + 02
6	5.100E + 07	1.663E − 04	1.451E − 03	5.455E + 00	−1.028E + 03
Output V_{o2}					
1	8.500E + 06	1.204E − 01	1.000E + 00	−9.530E + 01	0.000E + 00
2	1.700E + 07	1.697E − 03	1.409E − 02	1.488E + 02	3.394E + 02
3	2.550E + 07	2.029E − 03	1.685E − 02	1.142E + 02	4.001E + 02
4	3.400E + 07	1.532E − 04	1.273E − 03	3.413E + 01	4.153E + 02
5	4.250E + 07	4.201E − 05	3.489E − 04	2.167E + 01	4.982E + 02
6	5.100E + 07	3.499E − 05	2.906E − 04	4.685E + 01	6.187E + 02
Output V_{o3}					
1	8.500E + 06	1.056E − 01	1.000E + 00	−7.865E + 00	0.000E + 00
2	1.700E + 07	2.078E − 03	1.967E − 02	−1.247E + 02	−1.090E + 02
3	2.550E + 07	8.884E − 04	8.410E − 03	−1.328E + 02	−1.092E + 02
4	3.400E + 07	2.654E − 04	2.512E − 03	1.746E + 02	2.060E + 02
5	4.250E + 07	1.967E − 04	1.862E − 03	−1.793E + 02	−1.400E + 02
6	5.100E + 07	1.525E − 04	1.443E − 03	−1.748E + 02	−1.276E + 02
Output V_{o4}					
1	8.500E + 06	1.085E − 01	1.000E + 00	8.344E + 01	0.000E + 00
2	1.700E + 07	1.541E − 03	1.420E − 02	−1.535E + 01	−1.822E + 02
3	2.550E + 07	1.872E − 03	1.726E − 02	−7.073E + 01	−3.211E + 02
4	3.400E + 07	1.538E − 04	1.417E − 03	−1.445E + 02	−4.782E + 02
5	4.250E + 07	4.131E − 05	3.807E − 04	−1.620E + 02	−5.792E + 02
6	5.100E + 07	3.451E − 05	3.181E − 04	−1.372E + 02	−6.378E + 02

V_{o1}: DC component = 1.356817E − 03; THD = 1.703811E + 00 %
V_{o2}: DC component = −1.298111E − 03; THD = 2.201311E + 00 %
V_{o3}: DC component = −6.622693E − 04; THD = 2.170434E + 00 %
V_{o4}: DC component = 1.697496E − 03; THD = 2.240344E + 00 %

For the start-up of oscillation, the roots of the CE should be in the right-hand plane, which indicates that the coefficient of 's' term in Eq. (23) should be negative. Replacing $s = j\omega$ in Eq. (23), the frequency of oscillation (FO) and the condition of oscillation (CO) can be evaluated as:

$$\text{FO}: \quad \omega_0 = \sqrt{\frac{g_{m1}}{C_1 C_2 R}}, \tag{24a}$$

$$\text{CO}: \quad g_{m2} \geq \frac{1}{2}\left(\frac{1}{R} + g_{m1}\frac{C_2}{C_1}\right). \tag{24b}$$

From Eqs. (24a) and (24b), it is clear that the FO can be controlled by adjusting the value of the resistor R and/or by varying the control current I_{B1} of g_{m1}.

Assuming that the used external capacitors and the transconductance of both VDIBAs are equal, i.e. $C_1 = C_2$ and $g_{m1} = g_{m2}$, the relationship between four quadrature output voltages V_{o1}, V_{o2}, V_{o3}, and V_{o4} can be expressed as:

$$\frac{V_{o1}}{V_{o2}} = -j, \quad \frac{V_{o2}}{V_{o3}} = -j, \quad \frac{V_{o1}}{V_{o4}} = j, \tag{25}$$

ensuring the output voltages V_{o2}–V_{o1}, V_{o3}–V_{o2}, V_{o4}–V_{o3}, and V_{o1}–V_{o4} to be quadrature (in Fig. 21 the phase differences are $\phi = 90°$) and have equal amplitudes.

Assuming the non-ideal behavior of the active elements (β_i), the CE, FO, and the CO in Eqs. (23), (24a), and (24b) change to:

$$\text{CE}: \quad s^2 C_1 C_2 R + s[C_1 + \beta_1 C_2 g_{m1} R - \beta_2 C_1 g_{m2} R(\beta_1 + 1)] + \beta_1 g_{m1} = 0, \tag{26a}$$

$$\text{FO}: \quad \omega_0 = \sqrt{\frac{\beta_1 g_{m1}}{C_1 C_2 R}}, \tag{26b}$$

$$CO: \quad g_{m2} \geq \frac{1}{\beta_2(\beta_1 + 1)}\left(\frac{1}{R} + \beta_1 g_{m1}\frac{C_2}{C_1}\right). \tag{26c}$$

From Eqs. (26b) and (26c) it can be seen that the non-ideal behavior of the active elements affects both the frequency of oscillation and the condition of oscillation, however, CO can be satisfied by adjusting g_{m2} without affecting FO.

The proposed oscillator was designed with the following active parameters and the passive element values $I_{B1} = 100$ μA, $R = 1650$ Ω, and $C_1 = C_2 = 9.6$ pF, respectively, to obtain the sinusoidal output waveforms with the oscillation frequency of $f_0 = \omega_0/2\pi \cong 8.5$ MHz. In practice, to ensure the startup (build-up) of oscillations and subsequently to satisfy the CO in Eq. (24b) the value of I_{B2} is chosen as 131 μA. The waveforms of the quadrature voltages are shown in Fig. 22. In addition, Fig. 23 shows the frequency spectrum of the output waveforms and the value of total harmonic distortion (THD) at all outputs are less than 2.25 %. The results are summarised in Table 2.

7 Conclusions

This paper presents a new active element from the group of 'voltage differencing' devices, namely voltage differencing inverting buffered amplifier (VDIBA). The input part of the VDIBA is formed by the OTA, which is followed by the IVB with a gain of −1 that makes the introduced element attractive for resistorless and electronically controllable linear circuit design. As an application examples a new resistorless dual-output VM first-order all-pass filter, dual-output second-order all-pass filter, and four-phase quadrature oscillator circuits are proposed. SPICE simulation and experimental results confirm the feasibility of the proposed circuits.

8 Appendix

This section provides full nomenclature of the mentioned ABBs in Table 1 in alphabetical order.

C-(I)CDBA	Current-controlled (inverting) current differencing buffered amplifier
CCCDTA	Current controlled current differencing transconductance amplifier
CCCII+(−)	Plus-type (minus-type) second-generation current-controlled current conveyor
CC-VCIII−	Minus-type current-controlled third-generation voltage conveyor
DDCC	Differential difference current conveyor
DVCC+(−)	Plus-type (minus-type) differential voltage current conveyor
DV-VB	Differential-voltage voltage buffer
FD-OpAmp	Fully-differential operational amplifier
IUGA	Inverting unity gain amplifier
IVB	Inverting voltage buffer
MO-CCCCTA	Multiple-output current controlled current conveyor transconductance amplifier
OTA	Operational transconductance amplifier
UGDA	Unity gain differential amplifier
UVC	Universal voltage conveyor
VD-DIBA	Voltage differencing-differential input buffered amplifier
VDIBA	Voltage differencing inverting buffered amplifier

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References

1. Maheshwari, S. (2009). Analogue signal processing applications using a new circuit topology. *IET Circuits, Devices Systems, 3*(3), 106–115.
2. Minaei, S., & Yuce, E. (2010). Novel voltage-mode all-pass filter based on using DVCCs. *Circuits, Systems, and Signal Processing, 29*(3), 391–402.
3. Maheshwari, S. (2004). New voltage and current-mode APS using current controlled conveyor. *International Journal of Electronics, 91*(12), 735–743.
4. Minaei, S., & Cicekoglu, O. (2006). A resistorless realization of the first-order all-pass filter. *International Journal of Electronics, 93*(3), 177–183.
5. Kumar, P., Keskin, A. U., & Pal, K. (2007). Wide-band resistorless allpass sections with single element tuning. *International Journal of Electronics, 94*(6), 597–604.
6. Maheshwari, S. (2008). A canonical voltage-controlled VM-APS with a grounded capacitor. *Circuits Systems and Signal Processing, 27*(1), 123–132.
7. Metin, B., & Pal, K. (2010). New all-pass filter circuit compensating for C-CDBA non-idealities. *Journal of Circuits Systems and Computers, 19*(2), 381–391.
8. Bajer, J., & Biolek, D. (2010). Voltage-mode electronically tunable all-pass filter employing CCCII+, one capacitor and differential-input voltage buffer. In *Proceedings of the 2010 IEEE 26-th convention of electrical and electronics engineers in Israel*, Eilat, Israel, pp. 934–937.
9. Metin, B., Pal, K., & Cicekoglu, O. (2011). CMOS controlled inverting CDBA with a new all-pass filter application. *International Journal of Circuit Theory and Applications, 39*(4), 417–425.
10. Herencsar, N., Koton, J., Vrba, K., & Metin, B. (2011). Novel voltage conveyor with electronic tuning and its application to resistorless all-pass filter. In *Proceedings of the 2011 34th international conference on telecommunications and signal processing (TSP)*, Budapest, Hungary, pp. 265–268.
11. Biolkova, V., Kolka, Z., & Biolek, D. (2011). Dual-output all-pass filter employing fully-differential operational amplifier and current-controlled current conveyor. In *Proceedings of the 7th international conference on electrical and electronics engineering—ELECO 2011*, Bursa, Turkey, pp. 319–323.
12. Toker, A., & Ozoguz, S. (2003). Tunable allpass filter for low voltage operation. *Electronics Letters, 39*(2), 175–176.
13. Metin, B., Pal, K., & Cicekoglu, O. (2011). All-pass filters using DDCC- and MOSFET-based electronic resistor. *International Journal of Circuit Theory and Applications, 39*(8), 881–891.
14. Herencsar, N., Koton, J., Vrba, K., & Minaei, S. (2011). Electronically tunable MOSFET-C voltage-mode all-pass filter based on universal voltage conveyor. In *Proceedings of the international conference on computer and communication device—ICCCD 2011*, Bali Island, Indonesia, Vol. 1, pp. 53–56.
15. Herencsar, N., Koton, J., Jerabek, J., Vrba, K., & Cicekoglu, O. (2011). Voltage-mode all-pass filters using universal voltage conveyor and MOSFET-based electronic resistors. *Radioengineering, 20*(1), 10–18.
16. Minaei, S., & Yuce, E. (2012). High input impedance NMOS-based phase shifter with minimum number of passive elements. *Circuits, Systems, and Signal Processing, 31*(1), 51–60.
17. Biolek, D., & Biolkova, V. (2010). First-order voltage-mode all-pass filter employing one active element and one grounded capacitor. *Analog Integrated Circuits and Signal Processing, 65*(1), 123–129.
18. Khan, I. A., & Ahmed, M. T. (1986). Electronically tunable first-order OTA-capacitor filter sections. *International Journal of Electronics, 61*(2), 233–237.
19. Kumngern, M., Chanwutitum, J., & Dejhan, K. (2008). Electronically tunable voltage-mode all-pass filter using simple CMOS OTAs. In *Proceedings of the 2008 international symposium on communications and information technologies—ISCIT 2008*, Vientiane, Laos, pp. 1–5.
20. Tanaphatsiri, C., Jaikla, W., & Siripruchyanun, M. (2008). An electronically controllable voltage-mode first-order all-pass filter using only single CCCDTA. In *Proceedings of the 2008 international symposium on communications and information technologies—ISCIT 2008*, Vientiane, Laos, pp. 305–309.
21. Herencsar, N., Koton, J., & Vrba, K. (2009). A new electronically tunable voltage-mode active-C phase shifter using UVC and OTA. *IEICE Electronics Express, 6*(17), 1212–1218.
22. Pandey, N., Arora, P., Kapur, S., & Malhotra, S. (2011). First order voltage mode MO-CCCCTA based all pass filter. In *Proceedings of the 2011 international conference on communications and signal processing—ICCSP 2011*, Kerala, India, pp. 535–537.
23. Keskin, A. U., Pal, K., & Hancioglu, E. (2008). Resistorless first order all-pass filter with electronic tuning. *AEU—International Journal of Electronics and Communications, 62*(4), 304–306.
24. Fabre, A., Saaid, O., Wiest, F., & Boucheron, C. (1996). High frequency applications based on a new current controlled conveyor. *IEEE Transactions on Circuits Systems-I, 43*(2), 82–91.
25. Geiger, R. L., & Sanchez-Sinencio, E. (1985). Active filter design using operational transconductance amplifiers: a tutorial. *IEEE Circuits Devices Magazine, 1*, 20–32.
26. Biolek, D., Senani, R., Biolkova, V., & Kolka, Z. (2008). Active elements for analog signal processing: classification, review, and new proposals. *Radioengineering, 17*(4), 15–32.
27. OPA860—Wide bandwidth operational transconductance amplifier (OTA) and buffer, Texas Instruments, SBOS331C–June 2005–Revised August 2008, www.ti.com.
28. Maheshwari, S., Mohan, J., & Chauhan, D. S. (2011). Novel cascadable all-pass/notch filters using a single FDCCII and grounded capacitors. *Circuits, Systems, and Signal Processing, 30*(3), 643–654.
29. Herencsar, N., Koton, J., Minaei, S., Yuce, E., & Vrba, K. (2011). Novel resistorless dual-output VM all-pass filter employing VDIBA. In *Proceedings of the 7th international conference on electrical and electronics engineering—ELECO 2011*, Bursa, Turkey, pp. 72–74.

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