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A low power consumption CMOS differential-ring VCO for a wireless sensor

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Abstract This paper describes a new three-stage voltage controlled ring oscillator (VCO) based on 0.35 μm standard CMOS technology. The VCO was designed for a transmitter operating in the 863–870 MHz European band for wireless sensor applications. The transmitter is designed for binary frequency-shift keying (BFSK) modulation, communicating a maximum data rate of 20 kb/s. In addition to the VCO, the transmitter combines a BFSK modulator, an up conversion mixer, a power amplifier and an 863–870 MHz band pass filter. The modulator uses the frequency hopping spread spectrum and it is intended for short range wireless applications, such as wireless sensor networks. The oscillation frequency of the VCO is controlled by a voltage V_{CTRL}. Simulation results of the fully differential VCO with positive feedback show that the estimated power consumption, at desired oscillation frequency and under a supply voltage of 3.3 V, is only 7.48 mW. The proposed VCO exhibits a phase noise lower than −126 dBc/Hz at 10 MHz offset frequency.

Keywords Wireless sensor · CMOS technology · Direct conversion transmitter · Ring VCO · Differential structure · Positive feedback · Low power consumption

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1 Introduction

Nowadays wireless sensor networks (WSNs) constitute a promising research field. In fact, after great advancements in the development of intelligent sensors, powerful microprocessors and communication protocols, WSNs realize rapid integration in many applications. WSNs are composed by small nodes named sensors. These sensor nodes communicate in short distances and collaboratively work toward fulfilling the WSNs application specific objectives. When deployed in the environment, they communicate wirelessly to collect process and disseminate information about their physical or chemical environment to a point of interest. Sensors are used in critical applications such as telemedicine, precision agriculture, military surveillance, environmental monitoring, home automation and alarms.

With the increasing demand on security, reliability and autonomy for these WSNs applications, low power and low cost Wireless Sensor based on highly integrated circuits are needed. To design a fully integrated RF autonomous sensor for typical applications such as home automation and automatic meter reading, sensors should be able to operate for more than 5 years under battery energy supply. The 863–870 MHz band, which is available only in Europe, is a good field to test new ideas and concepts toward the development of a low power communication system for these low data-rate and short-range applications [1].

Products within these wireless applications already mentioned are generally extremely price sensitive and to reach network's objectives, they must meet some severe requirements. Since many systems are battery operated, there is a stringent demand on low power consumption to extend battery lifetime, a small physical size and a low unit cost are also required. Besides, since the transmission distance is very short, it is typically on the order of 50 m or less, we need a low data-rate and a Short range communication system. Cost-effective CMOS technology which enables development of true system-on-chips (SoCs) for wireless communication used in combination with highly integrated RF-IC implementations (the direct conversion architecture), the 863–870 MHz band, which was established by the electronic communications committee (ECC) and even the new global standard for wireless connectivity ZigBee are the key to achieving these requirements [1, 2].

This work deals with the design of a monolithic ring VCO for a sensor based wireless transmitter, which is presented with details in [2]. The VCO, which is an important component, can be used in several transmitters. The transmitter uses the direct conversion architecture for its simplicity, monolithic integration, as well as its low power consumption and low manufacturing cost [2, 3].

Section 2 presents the transmitter architecture. The circuit design of the proposed Ring VCO is presented in Sect. 3. Simulation results are given in Sect. 4 and discussion and design comparison with recently published VCOs are presented in Sect. 5. Finally, the conclusion is given in Sect. 6.

2 Transmitter architecture

The transmitter was designed for binary frequency-shift keying (BFSK) modulation with a data rate of 20 kb/s. Therefore, the peak signal energy in the modulated base band power spectrum of a BFSK signal represented in Fig. 1 concentrates in the frequency of 20 kHz. The transmission bandwidth of the BFSK signal was calculated to be 80 kHz. Therefore, the separation between adjacent channels has been chosen equal to 40 kHz. In fact, to fulfil FHSS requirement and ETSI regulations (which demand a minimum separation of 25 kHz between adjacent channels), the ISM band was divided into 58 channels and so each channel has a bandwidth of 120 kHz [2, 4].

Frequency hopped spread spectrum (FHSS) system was chosen for its low-power spectral density and high immunity to fading and interference [4].

Despite the direct conversion architecture has some well-known problems which prevented its widespread use; it has been well-recognized for its simplicity and potential for the use of single-chip implementation. Furthermore, it

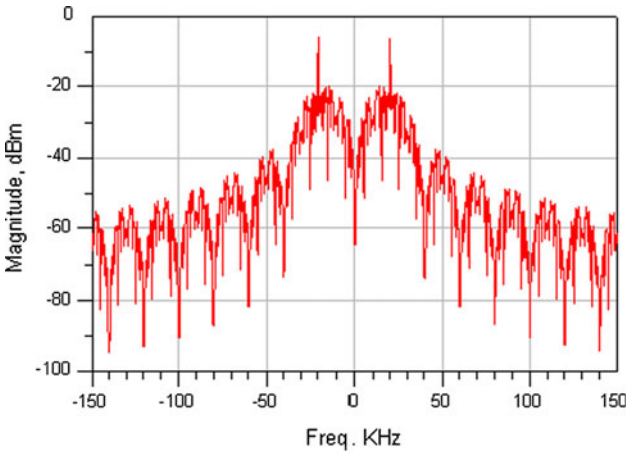

Fig. 1 Power spectrum of a BFSK signal (bit rate = 20 K bps)

requires only a minimum RF section and no image-reject filter [2–4].

The typical direct-conversion transmitter presented in Fig. 2 operates as follows: The digital FSK modulator modulates the data and synthesizes in a quadrature outputs a complex FHSS signals at base band. The modulator is based on direct-digital frequency synthesizer (DDFS) [4]. A fixed-frequency oscillator up converts these outputs to the 863–870 MHz band in a single-sideband mixer. With an oscillator at 866.5 MHz in the centre of the RF band, either the upper or the lower sideband is selected, the instantaneous carrier frequency will be placed anywhere in the band. So, the output frequency of the modulator needs only to span from 0 to 3.5 MHz to cover the ISM range of 866.5 ± 3.5 MHz and so the 7 MHz bandwidth ISM band [4]. After up conversion, a power amplifier (PA) drives the antenna with the modulated hopped carrier. An RF band pass filter (BPF) between the PA and the antenna suppresses out-of-band signals at the transmitter output.

Since the most demanding characteristics of an integrated transmitter are: linearity of the power amplifier, adjacent channel power ratio (ACPR) and transmitted power, the transmitter specifications were calculated and presented with details in paper [2]. Taking into account that the transmitter architecture is based on some standards and

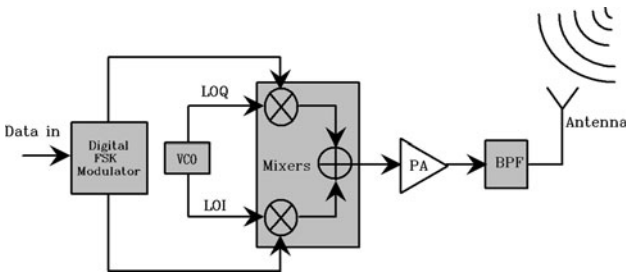

Fig. 2 Wireless sensor Transmitter architecture (direct conversion)

Table 1 Circuit blocks requirements of the transmitter

Components	VCO		Mixer		Power amplifier		BPF	
Parameters	F_{center} [kHz]	80	Conv gain	12.7 dB	Sparameters [dB]	$S_{21} = 10$	F_{center} [MHz]	866.42
			Sparameters [dB]	$S_{11} = -10$		$S_{11} = -10$		
				$S_{22} = -10$		$S_{22} = -10$	BW_{pass} [kHz]	100
				$S_{33} = -15$		$S_{12} = -25$		
	K_V [kHz]	20	NF	13 dB	NF	3 dB	BW_{stop} [kHz]	200
			Linearity [dBm]	IIP3 = 19	Linearity [dBm]	IIP3 = 7.4	A_{stop}	60 dB
				$P_{-1dB} = 9$		$P_{-1dB} = 0.5$	Insertion loss	4 dB

preliminary data like the BFSK modulation scheme, the hopping bandwidth of 7 MHz, number of channels, the data rate, and even the maximum range fixed by the use of Zigbee standard and is equal to 50 m, the specifications are −20 dBc for the ACPR and 0 dBm for the transmitted power.

Before starting the design of transistor-level blocks of the transmission system it is necessary to determine the specifications of each block in terms of performances. Therefore, each block in the transmitter was modeled and simulated using the advanced design system tool (ADS). The goal of this simulation is to determine the transmitter blocks parameters that meet the overall transmitter specifications using a filter, a VCO, a PA and an up conversion mixer from the ADS library models. Using the circuit envelope simulator in ADS a transmitter chain can be optimized for both output power and adjacent channel power ratio. Simulations were started (based on the state of the art) by assigning parameters values to transmitter blocks, then were adjusted to fulfil transmitter specifications already mentioned. Parameters for each block of the transmitter are optimised so they meet the low power and the low cost transceiver specifications. As a result, the obtained parameters of the transmitter's blocks are summarized in Table 1 [2, 4].

Lowering power is also achieved through the use of FHSS technique with a BFSK modulation approach [2]. This addresses for CMOS technology and allows a highly integrated single chip solution.

3 Circuit design

The designed oscillator must generate the center frequency of the 863–870 MHz ISM band [4]. The integrated oscillator must meet some important specifications such as low power consumption, low phase noise and small die size [2, 4]. According to the literature, there are two oscillator's types: harmonic and relaxation [5]. The advantage of harmonic oscillators is their excellent phase noise. But they can not always be fully integrated. Indeed, for this type of oscillators, we must have a technology that allows integration of the passive inductance on the silicon that can be not compatible with standard CMOS technology. In the case of an LC oscillator for frequencies below 1 GHz, silicon area required by the inductor is too high with a relatively low quality factor [6]. In fact, LC oscillators with excellent characteristics exist such as the VCO presented in [7]. Indeed, the external parallel resonator used in [7] increases the phase noise of the VCO, the cost and the complexity of the design by the use of an automatic amplitude control circuit. For relaxation oscillators the most used ones for integration are ring oscillators. Although ring oscillators present a relatively high phase noise, they are attractive since they usually have wider oscillation frequency range, smaller die size and lower power consumption. Therefore, ring oscillator topology is the most suitable for our application.

The designed fully differential Ring VCO uses a three cells structure connected as shown in Fig. 3. The use of three stages was chosen to increase the oscillation frequency (F_{osc}) and reduce power consumption at the same time. In fact, minimizing the number of stages reduces consumption and according to equations presented later in this section, it increases F_{osc}.

The basic structure of each cell of the Ring VCO is based on a differential pair with positive feedback. This is a new structure used for the first time for ring VCOs. This proposed architecture based on active CMOS transistors and a polysilicon resistor provides good performances especially in term of tuning range of oscillation, power consumption and phase noise as shown by the post-layout simulation results. The differential mode is used to reduce substrate noise. Two transistors controlled by the gate

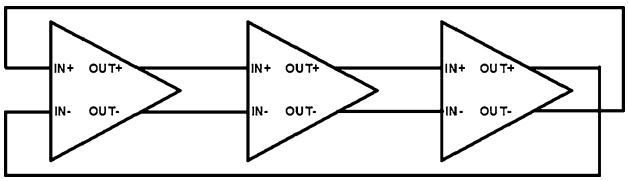

Fig. 3 Architecture of the three-stages Ring VCO

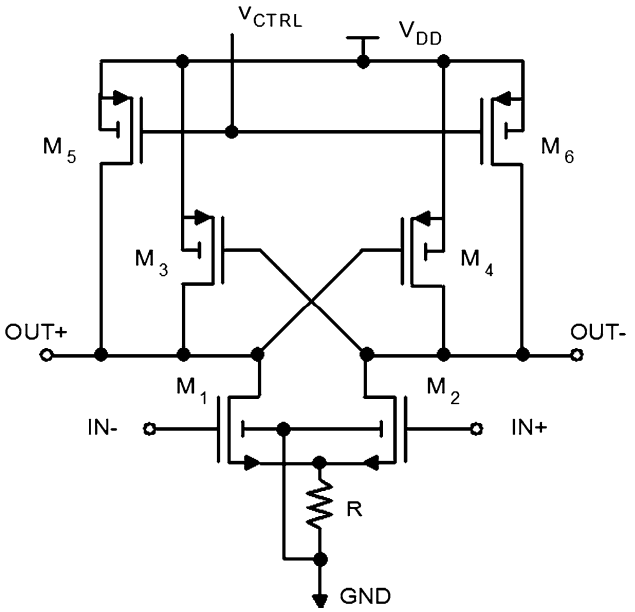

Fig. 4 Proposed delay cell implementation

voltage (V_{CTRL}) of two other cross-coupled transistors form this cell presented by Fig. 4. The voltage V_{CTRL} controls the output frequency of the structure. The polarization of the differential structure is provided by a polysilicon resistor. Positive feedback has been added to a fully differential CMOS amplifier to reduce the delay time and increase the speed of operation. Using negative feedback, improves the speed. However, for the same improvement in term of speed of operation, the negative feedback requires a much higher value of resistance than that used for the positive feedback. This is less favorable for integrated circuit technology [6].

Figure 4 illustrates the circuit schematic of the proposed delay cell. In this circuit, the NMOS transistors M_1 and M_2 form the input pair to increase the transconductance to capacitance ratio and achieve higher frequency of operation. The loads of the delay cell include controllable PMOS transistors (M_5 and M_6) by the gate voltage V_{CTRL} and the two cross-coupled PMOS transistors M_3 and M_4. These two transistors (M_3 and M_4) are used to provide positive feedback for oscillation. The use of the polarization resistance for the differential pair, avoids the use of current mirrors, and consequently additional transistors, which minimize the circuit area. This also enhances the phase noise performance. In fact, as detailed in [8], the current source transistor is responsible for injecting flicker noise and noise at the harmonic frequencies of the carrier frequency to the cross-coupled transistors, where these frequency components are up-converted and down-converted to the carrier frequency, respectively, and hence, degrades the phase noise performance.

Designing the three-stage ring VCO at central band frequency requires a compromise that must be obtained between frequency of oscillation, power consumption and noise performances. Therefore, theoretical analysis of the proposed cell is necessary to find the relationship between frequency of oscillation, control voltage and circuit's parameters.

To calculate the operating frequency of the oscillator, a half-circuit of the delay cell can be considered. In fact, the oscillation frequency of N stages ring oscillator is equal to $2NT_d^{-1}$, where T_d is the large signal delay of each stage [5, 6].

This delay is roughly proportional to τ which denotes the constant of time at each cell's output node of the oscillator.

$$\tau = R_{eq}C_L \tag{1}$$

with R_{eq} is the equivalent resistor at outputs OUT+ or OUT− and C_L denotes total capacitance seen at each cell's output node to ground. Thus, the oscillation frequency is given by:

$$F_{osc} = \frac{1}{2NR_{eq}C_L} \tag{2}$$

As the circuit shown in Fig. 4 is differential, to study the behavior of small signal circuit we can consider only the left half of the delay cell presented in Fig. 5 and so the effect of the other half-circuit can be neglected. Indeed, if we consider the input IN-, the transistor M2 is shorted and the node OUT- will be grounded and so transistors M4 and M6 are blocked.

In Fig. 5 g_{mi} and G_L are the transconductance of transistor Mi and the load conductance, respectively. Thus, according to half-simplified circuit of the delay cell, the equivalent output resistance is approximated to:

$$R_{eq} \approx r_{01}//r_{03}//r_{05} \tag{3}$$

Where r_{0J} is the drain-source resistance of transistor M_J. In saturate mode of operation [5], the resistance r_{05} can be approximated by:

$$r_{05} \approx \lambda I_{ds5} = \lambda K_{pp}\left(\frac{W}{L}\right)_5 (V_{CTRL} - (V_{DD} + V_T))^2 \tag{4}$$

Here λ, I_{ds5}, K_{pp}, V_T and W/L are respectively the channel length modulation factor, the drain current of transistor M_5,

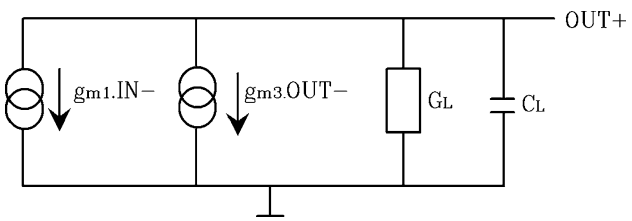

Fig. 5 Half-circuit of the proposed delay cell

the process transconductance parameter, the threshold voltage and the ratio of width by length of transistor M_5. K_{pp} is proportional to the product of the carrier mobility and the gate capacitance per unit area. According to Eqs. (2) and (4), the oscillation frequency can be varied by changing the value of r_{05} and r_{06}, which is controlled by V_{CTRL}. Indeed, when V_{CTRL} increases, the drain current of transistor M_5 (I_{ds5}) and r_{05} increase. Thus, F_{osc} decreases and equals to F_{min}. On the other side, if the control voltage decreases, the oscillation frequency increases and is equal to F_{max}. Thus, in this design, the output frequency can be simply tuned by controlling the channel conductance of PMOS transistors M_5 and M_6 via the control voltage. Moreover, the value of R can slightly vary F_{osc} but it widely affects both power consumption and phase noise of the VCO. That is why the circuit parameters are sensitive to the choice of the value of R. To ensure the oscillation in the wanted frequency band and keeping a good compromise between power consumption and phase noise, the value of R was chosen to be equal to 1.25 KΩ.

4 Simulation results

The process parameters for the transistors used in this work correspond to the AMS 0.35 µm Technology [9]. The design of the CMOS VCO starts by defining the design specifications in terms of the performance parameters of interest, such as low power consumption and low phase noise. As mentioned in [10], the reduction of transistor dimensions means that the speed of operation of the circuit is increased and so the operating frequency also increases. However, at the same time, the power consumption increases and new methods should be devised to reduce the dissipated power. Thus, it is necessary to achieve a compromise between the operating frequency and the power consumption.

Table 2 presents size parameters of the optimized delay cell ring VCO. These sizes were calculated using equations already presented and taking into account the optimization of power consumption and phase noise. The layout of the VCO, which is designed in Cadence virtuoso analog design environment, is shown in Fig. 6. The chip area of the proposed ring VCO without the pads is about 30 × 130 µm.

Table 2 Transistor sizes of delay cell

Components	Type	Size W/L (µm/µm)
M1–M2	NMOS	15/0.4
M3–M4	PMOS	5/0.4
M5–M6	PMOS	20/0.4
R	rpolyhc	5.85/5.85

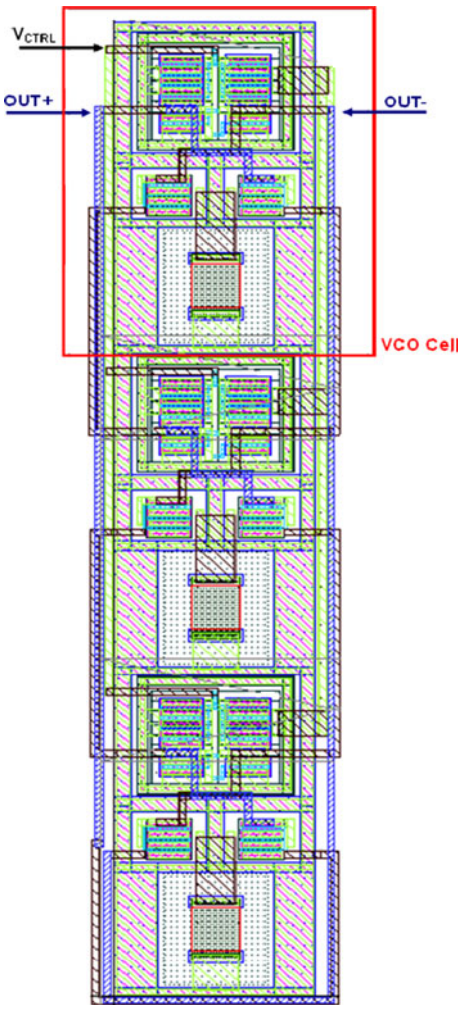

Fig. 6 VCO layout

To determine the tuning range and the linearity of the proposed VCO, a parametric analysis in which the oscillation frequency is simulated for several control voltages, is performed. This data is presented in Fig. 7 by the curve K_{VCO}.

As shown in this figure, the tuning range of the VCO Layout is 381 MHz–1.15 GHz when the control voltage is varied from 1.8 to 3.3 V. Considering 866.5 MHz as the central frequency, the simulated tuning range $\Delta f/\Delta f_0$ is of about 89 %. The oscillator has good linearity for a control voltage between 1.8 and 2.2 V and the VCO gain is around −783 MHz/V.

As the VCO is prepared for manufacturing, further simulation was done to ensure that even with process variations the circuit keeps his performances. Therefore, three cases were considered taking into account worst simulation conditions like variation of the temperature, the supply voltage and the MOS behaviour.

The first case (TM) presents the most typical one. It considers that all transistors have a typical model, supply

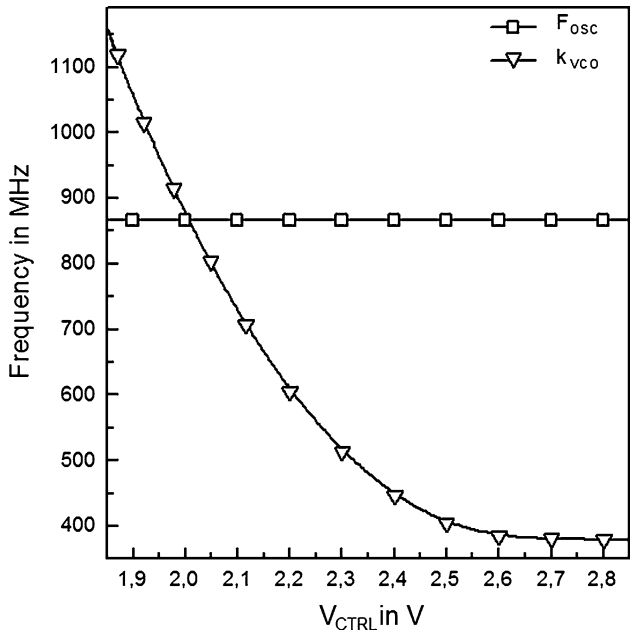

Fig. 7 VCO tuning characteristic for $F_{osc} = 866.521$ MHz

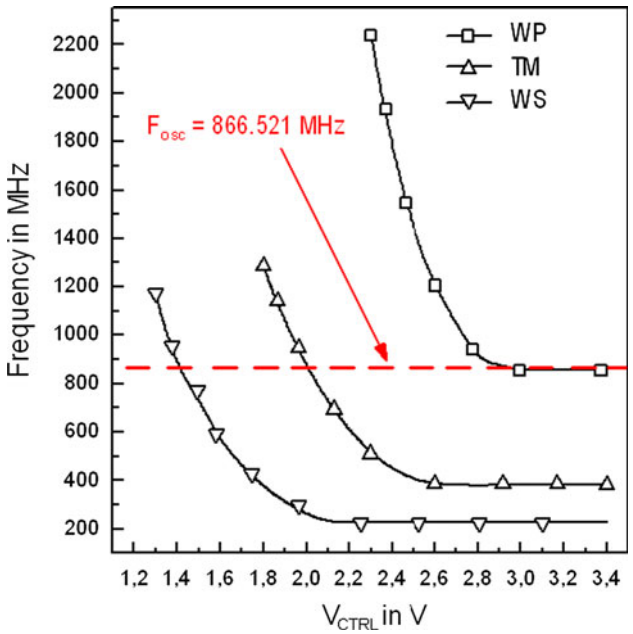

Fig. 8 VCO tuning range characteristic (Worst cases simulation)

voltage is equal to 3.3 V and the circuit is operating at a temperature of 27 °C.

The second one (WP) presents the worst power conditions where V_{DD} equals to 3.3 V + 10 %, the temperature is −60 °C and transistors are using the worst-case power condition model.

The third case (WS) resumes the worst speed one. In fact, transistors use the worst-case speed condition model, V_{DD} equals to 3.3 V −10 % and the temperature is about 60 °C.

Figure 8 shows the variation of the frequency of oscillation depending on the control voltage at these three cases presented previously. It is obvious to note that the ring VCO can always oscillate at required frequency which is $F_{osc} = 866.521$ MHz by a simple adjustment of the value of V_{CTRL}. It is important to note that the process variation effect on the poly-silicon resistor was considered. Although it is not presented in Fig. 8, it was verified that the system still works correctly at the desired frequency of oscillation even with process resistance variation.

The transient response of the VCO at a frequency of 866.521 MHz when the control voltage equals to 2 V is depicted in Fig. 9. It can be seen that the output signals VOUT+ and VOUT− of the designed VCO have large amplitude.

At this control voltage, the power consumption of the Ring VCO is only 7.48 mW. Hence, power dissipation varies with control voltage, it is equal to 4.44 mW at 3.3 V and the maximum power dissipation is 9.24 mW at operating frequency of 1.15 GHz under control voltage of 1.8 V.

To examine the noise performance of the proposed ring VCO, the phase noise is simulated with SpectreRF and

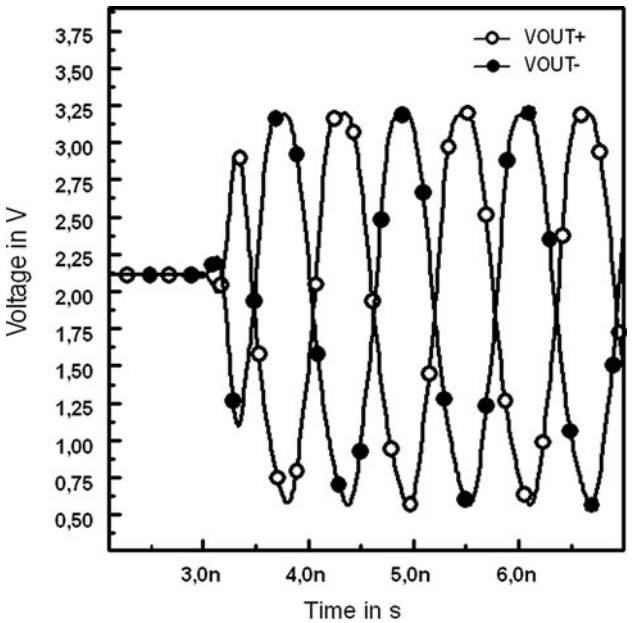

Fig. 9 Transient response of the VCO at 866.521 MHz

presented by Fig. 11. The VCO phase noise is represented as a ratio of power in 1 Hz bandwidth in one sideband to the power of the carrier and is specified in dBc/Hz at a frequency offset from the carrier. It is defined as [11]:

$$L(\Delta\omega) = 10log\left[\frac{2FKT}{P_{sig}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_1/f^3}{|\Delta\omega|}\right)\right] \quad (5)$$

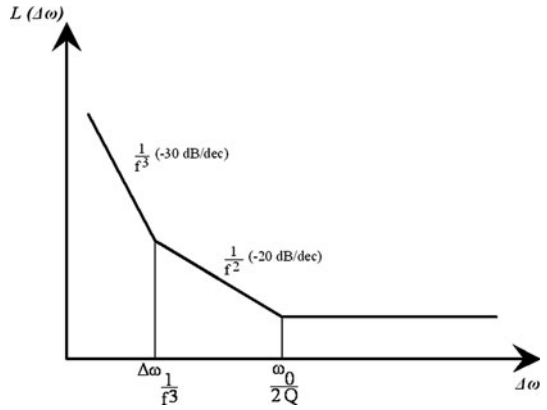

Fig. 10 Typical plot of the phase noise of an oscillator versus offset from carrier

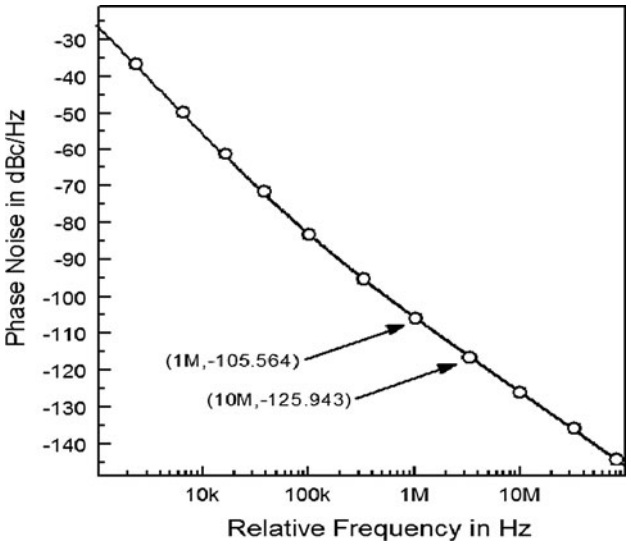

Fig. 11 Phase noise at central band frequency

where F is an empirical parameter (often called the "device excess noise number"), K is the Boltzmann's constant, T is the absolute temperature, P_{sig} is the average power dissipated in the resistive part of the circuit, ω_0 is the oscillation frequency, Q is the effective quality factor of the VCO, $\Delta\omega$ is the offset from the carrier and $\Delta\omega_{1/f}^3$ is the frequency of the corner between the $1/f^3$ and $1/f^2$ regions as shown in the sideband spectrum of Fig. 10, it is equal to the 1/f corner of device noise. It is important to note that the F factor is an empirical fitting parameter and therefore must be determined from measurements, diminishing the predictive power of the phase-noise equation [12]. Phase Noise in $1/f^3$ region is due to device 1/f noise. Phase Noise in $1/f^2$ region is due to device thermal noise.

As shown in Fig. 11, the single sideband phase noise at a frequency of 866.521 MHz has a value of about −106 dBc/Hz at an offset frequency of 1 MHz and a value of −126 dBc/Hz at an offset frequency of 10 MHz.

5 Discussion and design comparison

The performance of the proposed ring VCO designed is summarized in Table 3 along with the reported results of other recent published oscillators. Compared in various aspects to Ring oscillators using CMOS process and operating at similar frequencies, the proposed circuit provides good post-layout simulation results. In addition to a low phase noise value, a wide frequency tuning range and even a low power consumption, its area is small.

Compared to [13], which is designed under closest conditions to those of the VCO presented in this paper such as technology, number of stages and offset frequency, our ring VCO has −126 dBc/Hz of phase noise value which is 10 dBc/Hz lower and the power consumption is about six times smaller than [13]. In term of power consumption, the presented VCO has the lowest value although [14–17] operates at lower supply voltage. It is necessary to indicate that the value of power mentioned in the Table 3 is the power consumed by the oscillator alone without buffers.

Since the VCO was sent for fabrication, a microphotograph of the prototype, fabricated using a 0.35 μm CMOS process, is shown in Fig. 12. The chip area, including pads and without buffers, is about 725 × 324.4 μm. The chip area

Table 3 Performance summary and design comparison

Parameter	[13]	[14]	[15]	[16]	[17]	This work
Number of stages	3	2	2	4	2	3
Technology [μm]	0.35	0.18	0.09	0.18	0.18	0.35
Tuning range [GHz]	0.92–0.925	0.73–1.43	1.57–3.57	0.62–1.5	0.186–1.576	0.381–1.15
Central frequency [MHz]	–	900	–	1,350	850	866.521
Power [mW]	42.9	65.5	16.8	41	11.38	7.48
Phase noise [dBc/Hz]	−116	−106.1	−90	−126	−113.5	−126
Offset [MHz]	10	0.6	0.6	1	0.6	10
Design level	Tested	Tested	Simulated	Tested	Simulated	Simulated

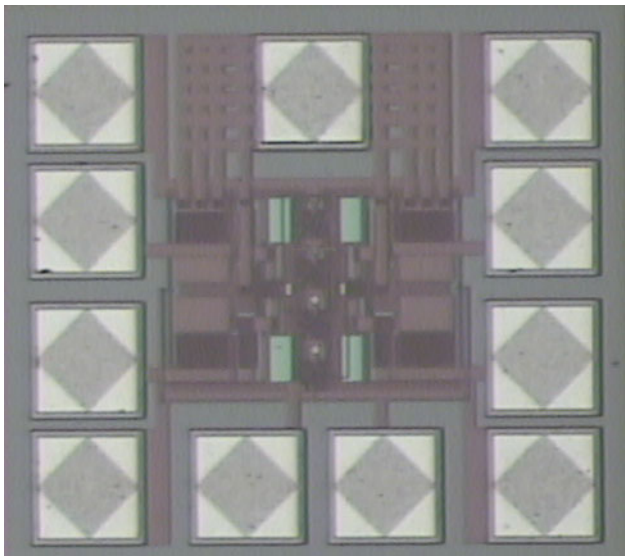

Fig. 12 Die microphotograph of the VCO's prototype

including pads and buffers will increase and exceed the layout area already mentioned. In fact, buffers were designed at the outputs of the VCO to magnify and regulate the output signal of front circuit, at the same time it provides large enough current and voltage to drive follow-up circuit. Even more important, it prevents frequency shift due to external loads Thus, buffers provide the 50Ω transmission line impedance matching, then eliminate the power loss of the signal reflection, and increase the efficiency of transmission.

The future work will be focused on realizing measurement of the circuit performances and compare them with those obtained from post-layout simulation. Thus, measurement results of the transmitter's die will be published in a further work.

6 Conclusion

A 863–870 MHz Band, three-stage CMOS ring oscillator with positive feedback and presenting wide frequency range with good linearity was detailed in this paper. The VCO is designed in 0.35 μm CMOS technology and operated on a 3.3 V supply voltage. At the oscillation frequency of 866.5 MHz, the power consumption of the circuit is only 7.48 mW and the phase noise at an offset frequency of 10 MHz is about −126 dBc/Hz. Post-Layout simulation results show that the proposed ring VCO has advantages of very low power dissipation, large amplitude and small area. In addition, it was shown that the circuit is able to keep its performances even in critical conditions (worst cases).

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