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Accuracy improvement of the output impedance model for capacitive down-converters

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Abstract Contemporary models fail to include the influence of the output buffer capacitor size on the performance of capacitive DC–DC converters. This letter examines the relevance of this dependency and shows how to adapt existing models in order to include it. The improved model is verified mathematically for down-converters, by means of Spice simulations and based on measurements of silicon integrated prototypes. Measurements demonstrate an accuracy improvement of up to 30 % compared with the conventional model.

Keywords Capacitive DC–DC converter · Output impedance model · Output capacitor · CMOS

1 Introduction

The design of capacitive DC–DC converters requires accurate modeling and analysis. The work in [1] laid the cornerstone of the output impedance model. The capacitive DC–DC converter can be modeled as an ideal voltage source with a non-zero output impedance. At rather low switching frequencies, if the system time constants are smaller than the switching period, the output impedance is inverse proportional to the switching frequency and to the total amount of charge transferring capacitance. The converter is operating in the slow switching limit (SSL). At high switching frequencies the system's time constants exceed the switching period and the parasitic resistances in the circuit dominate the output impedance, this region is called the fast switching limit (FSL).

The work in [1] became together with the work in [2, 3] the cornerstone of the state of the art design techniques. Last couple of years the fundamental work of these pioneers converged into the work in [4]. These models were conceived based on the assumption that capacitive DC–DC converters have an infinitely large output buffer capacitance.

Because of the raise of interest in monolithic converters the accurate modeling of capacitive DC–DC converters gains interest [5, 6]. Due to the high cost of chip area, the buffer capacitance size is decreasing and state of the art models fail to model the influence of this relative decrease on the output impedance of the converter.

Section 2 gives a short overview of the conventional model as it is developed in [4], Sect. 3 first gives a physical explanation for the inability of the conventional model to take the output capacitor size into account and next it introduces a mathematical approach for the problem. Finally this Section proposes a modified model. This model is applied on the series-parallel type of down-converters in Sect. 4 and verified against spice simulations in Sect. 5. Section 6 discusses the impact of output capacitor sizing on the output voltage ripple and the improved model is validated based on measurements in Sect. 7.

2 Conventional model

In [4] the output impedance in the SSL is determined to be:

$$R_{\mathrm{SSL,old}} = \frac{V_{\mathrm{out}}}{I_{\mathrm{out}}} = \frac{V_{\mathrm{out}}}{Q_{\mathrm{out}} f_{\mathrm{sw}}} = \Sigma_i \frac{Q_i}{Q_{\mathrm{out}}^2} \frac{\Delta v_i}{f_{\mathrm{sw}}} \quad (1)$$

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$$\Delta v_i = \frac{Q_i}{C_i} \tag{2}$$

$$R_{\mathrm{SSL,old}} = \Sigma_i \frac{a_{ci}^2}{C_{\mathrm{tot}} f_{\mathrm{sw}}} \tag{3}$$

In Eq. 1 f_{sw} represents the converters' switching frequency and Q_{out} Q_i respectively the total charge transferred to the load and the charge transferred by a single capacitor C_i in a topology with N charge transferring capacitors (also known as the flying capacitors). Δv_i is the change in voltage of the i-th flying capacitor. This change in voltage is induced by charge redistribution after connecting capacitor terminals that have different voltage potentials.

If the assumption is made that an infinitely large output buffer capacitor is present then the change in voltage Δv_i due to changing phases is only function of the capacitor size C_i and the charge transferred by the capacitor C_i. Thus Eq. 1 can be substituted by Eq. 2. This equation can be optimized and simplified towards Eq. 3. The latter is demonstrated in [4]. C_{tot} represents the total amount of flying capacitance and $a_{c\ i}$ is the charge transfer vector element corresponding to the i-th flying capacitor. In fact $a_{ci} = \frac{Q_i}{Q_{\mathrm{out}}}$.

3 Modified model

3.1 Physical approach

The conventional model is based upon the fact that an infinitely big output capacitor is present and therefore the output voltage is constant. In practice, the output capacitor is often in the same order of size as the flying capacitors. This gives raise to deviations in output impedance between the measurements and the conventional model: the conventional model gives an overestimate of the output impedance. Which corresponds with an underestimate of the potential converter performance. In order to explain these deviations between the conventional model and the measurements, this paragraph will go deeper into the physical phenomena that appear during the converter's operation. First in case of an infinite output capacitor, next in case of a finite output capacitor.

3.1.1 Infinite output capacitance

Two simultaneous phenomena take place during each switching-phase: charge redistribution and charge pumping. This is demonstrated for a single flying capacitor converter in Fig. 1

Charge redistribution: Charge is transferred from the flying capacitors to the output capacitor (Fig. 1a, c)). This

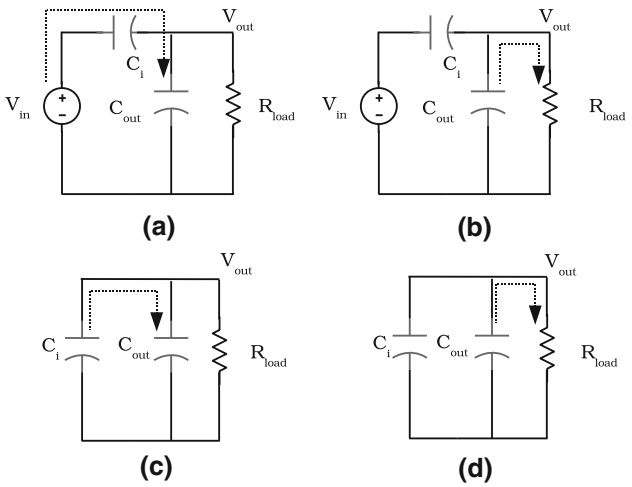

Fig. 1 **a** Charge redistribution phase1, **b** charge pumping phase1, **c** charge redistribution phase2 and **d** Charge pumping phase2

is induced by the potential difference of two nodes connected after the reconfiguration of the converter. The charge redistribution associated with this reconfiguration is lossy. By connecting two capacitors a part of the energy on the capacitors is dissipated in the circuit. This will appear as a non zero output impedance even if ideal switches and ideal capacitors are used. The charge redistribution takes place in an impulse-like fashion. This current impulse will be damped by the output capacitor and the charge is stored on the output capacitor. Since the output capacitor is infinitely big no variation in output voltage is observed.

Charge pumping: This phenomenon is associated with the transfer of charge from the converter to the load (Fig. 1b, d)). In fact this comes in the ideal case down to the charge transfer from the output capacitor to the load. Since the output capacitor is nothing but a charge reservoir, all the charge that is transferred from this reservoir was initially transferred from the flying capacitor to the output capacitor.

Charge redistribution will transfer charge from the flying capacitor to the output buffer capacitor C_{out}, charge pumping will transfer the charge from the buffer to the load. In case that an infinite output capacitor is used: all charge that is transferred to the load is transferred by a lossy mechanism. The latter gives raise to a nonzero output impedance.

3.1.2 Finite output capacitance

The charge redistribution phenomenon that appears when a finite output capacitor is present is identical as in case an infinite output capacitor is present (Fig. 2a, c)).

In this case charge pumping is different. Since the output buffer capacitor has a finite capacitance: the output voltage drops during each phase due to discharging this

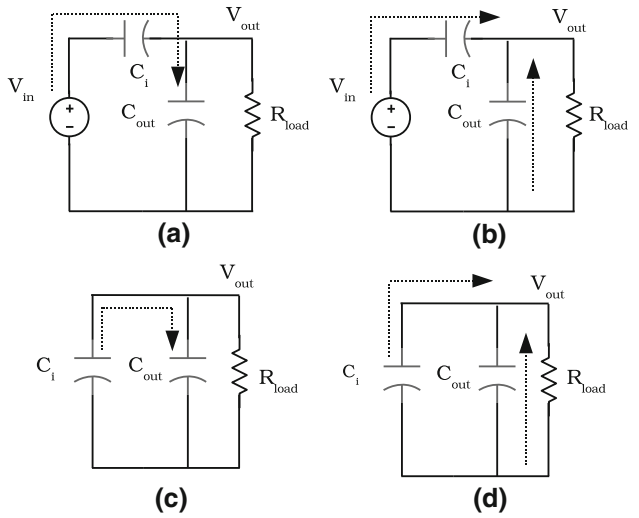

Fig. 2 **a** Charge redistribution phase1; **b** charge pumping phase1, **c** charge redistribution phase2 and **d** charge pumping phase2

output buffer capacitor. This change in output voltage induces a change in voltage over the flying capacitor and thus charge transfer from the flying capacitor to the load. Not only the output buffer capacitor will transfer charge to the load, as well will the flying capacitor (Fig. 2b, d)).

This charge transfer that originates from the flying capacitor corresponds with discharging capacitors by means of a resistive load. This charge transfer is lossless. This implies that in case a finite output capacitor is used, part of the charge delivered to the load is transferred by means of a lossy mechanism and part of the charge by means of a lossless mechanism. This explains the deviation of the conventional model from the observations in simulations and measurements. In the next paragraph this is quantified and put into an modified/improved output impedance model.

3.2 Mathematical approach

The output impedance is introduced by means of the change in voltage (Δv_i) on the flying capacitors after reconfiguration. According to the conventional model (Eq. 1) this Δv_i can be calculated based on the size of the capacitor and the amount of charge transferred to the load by the capacitor. But from the finite output capacitor point of view Δv_i is associated only with the lossy charge transfer thus is induced by the charge redistribution. In order to define the actual Δv_i one has to quantify the amount of charge that is transferred via the lossy mechanism. The latter corresponds with the charge that originates from the output capacitor C_{out} during the charge pumping. In the next paragraph the ratio between the charge involved in the lossy transfer and the total charge that is delivered to the load is determined.

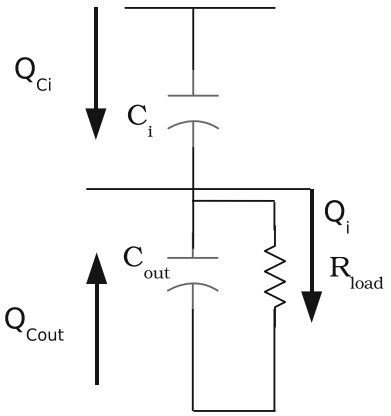

Fig. 3 A single flying capacitor voltage divider

In Fig. 3 a single flying capacitor capacitive DC–DC converter is depicted. During the charge pumping, charge is transferred from as well the flying capacitor Q_{C_i} as from the output capacitor Q_{Cout} to the load. The total amount of charge (Eq. 4) that is delivered to the load is Q_i. We are looking for the fraction of the charge that is transferred by means of the lossy mechanism thus: $\frac{Q_{\text{Cout}}}{Q_i}$

From Eq. 5 it is clear that the change in charge on the capacitors is only function of the size of the capacitors (C_{out} C_i) and the variation of voltage over the capacitors Δr_i. By calculating the ratio between the charge from C_{out} and the charge that is delivered to the load (Eq. 6), it is shown that this ratio is only function of the capacitor sizes (Eq. 7). The ripple Δr_i itself is a function of the other system parameters, such as the switching frequency and the load, but is cancelled out.

$$Q_i = Q_{\text{Cout}} + Q_{C_i} \tag{4}$$

$$Q_i = \Delta r_i \text{Cout} + \Delta r_i C_i \tag{5}$$

$$\frac{Q_{\text{Cout}}}{Q_i} = \frac{\Delta r_i \text{Cout}}{\Delta r_i \text{Cout} + \Delta r_i C_i} \tag{6}$$

$$\frac{Q_{\text{Cout}}}{Q_i} = \frac{\text{Cout}}{\text{Cout} + C_i} \tag{7}$$

Based upon 7 a new formula for Δv_i is proposed in Eq. 8. This change in voltage is function of the charge that is transferred by means of the lossy mechanism. So that a modified output impedance model is proposed in Eqs. 9–10.

$$\Delta v_i = \frac{Q_i}{C_i} \frac{C_{\text{out}}}{C_{\text{out}} + C_i} \tag{8}$$

$$R_{\text{SSL,new}} = \Sigma_i \left(\frac{Q_i}{Q_{\text{out}}} \right)^2 \frac{C_{\text{out}}}{C_{\text{out}} + C_i} \frac{1}{C_i f_{\text{sw}}} \tag{9}$$

$$R_{\text{SSL,new}} = \Sigma_i \frac{C_{\text{out}}}{C_{\text{out}} + C_i} \frac{a_{ci}^2}{C_i f_{\text{sw}}} \tag{10}$$

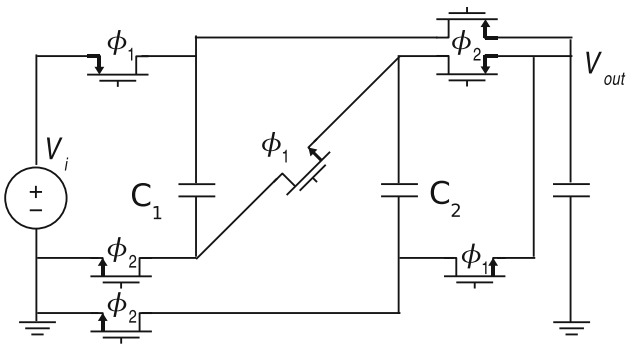

Fig. 4 Schematic representation of a capacitive series-parallel 1/3 converter topology

4 Cases

In this paragraph this improved output impedance model is applied on as well series-parallel topologies as on Makowski type topologies.

4.1 Series-parallel type

Series-parallel-type converters, convert voltages during two phases (ϕ_1 and ϕ_2). Fig. 4 shows a 1/3-topology of the series-parallel-type. In one phase the charge transferring capacitors (C_1, C_2) are put in series. In the other phase the capacitors are put in parallel. Based on the number of flying capacitors (N) and the configuration (in series between input and output and parallel with the output or vice versa) voltage conversion ratios $\frac{N}{N+1}$ or $\frac{1}{N}$ can be achieved. In general all of these capacitors are equivalent and thus for optimum charge transfer their sizes are equal.

The expression for R_{SSL} can be simplified if taken $C_i = \frac{C_{tot}}{N}$ in which N is the number of flying capacitors. This is true for capacitive DC–DC converters of the series-parallel type. Then R_{SSL} can be written as in Eq. 11

$$R_{SSL,new} = \frac{C_{out}}{C_{out} + \frac{C_{tot}}{N}} \Sigma_i \frac{a_{ci}^2}{C_{tot} f_{sw}} \tag{11}$$

$$R_{SSL,new} = \frac{C_{out}}{C_{out} + \frac{C_{tot}}{N}} R_{SSL,old} \tag{12}$$

Equation 12 shows that the influence of the output buffer capacitor decreases for high values of N. Thus the deviation between the actual performance and the conventional model is highest for $N = 1$ and thus a converter with a VCR of $\frac{1}{2}$.

4.2 Makowski type

In Fig. 5 the switch/capacitor configuration for a $\frac{4}{5}$ is shown. This topology is hard to classify but since its existence is predicted in [1], it is classified as such. It is proven in [4] that optimized charge transfer is achieved by sizing C_1, C_2 and C_3 respectively as $\frac{1}{4}$, $\frac{1}{4}$, $\frac{2}{4}$ of C_{tot}.

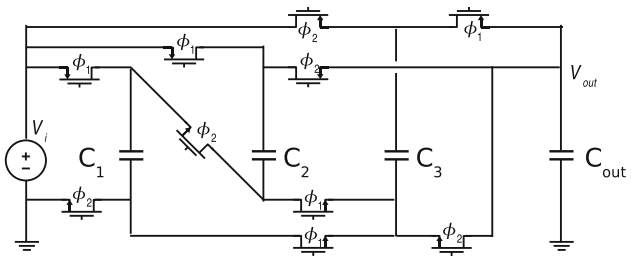

Fig. 5 Schematic representation of a capacitive 4/5 converter topology

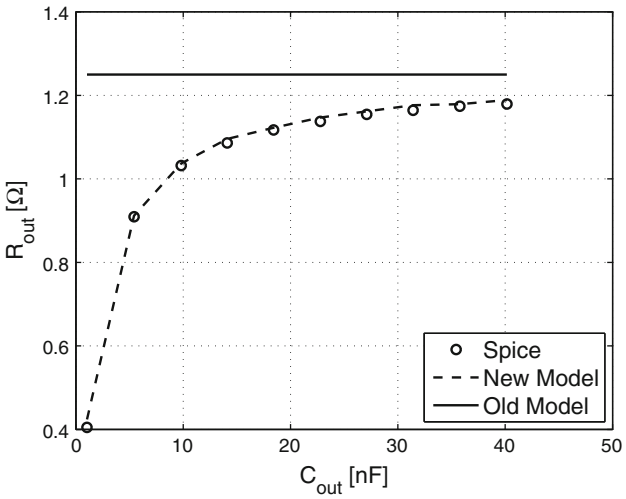

Fig. 6 Output impedance of a series parallel 1/2 capacitive DC–DC converter as a function of the output capacitor size

Thus calculation of the R_{SSL} gives Eq. 13.

$$R_{SSL,new} = 2\frac{\frac{1}{5}^2}{C_{1,2} f_{sw}} \frac{C_{out}}{C_{out} + C_{1,2}} + \frac{\frac{2}{5}^2}{C_3 f_{sw}} \frac{C_{out}}{C_{out} + C_3} \tag{13}$$

5 Verification

In this chapter the accuracy improvement of the model will be verified by means of Spice simulations. Two topologies, a $\frac{1}{2}$ series-parallel-type topology and a $\frac{4}{5}$ Makowski type topology are simulated for different ranges of capacitor size and freq ranges. These simulations were performed with ideal switches and capacitors so that the converter operates in the SSL.

5.1 Series-parallel

In Fig. 6 the output impedance of a series-parallel converter with ideal VCR $\frac{1}{2}$ is plotted in function of C_{out}.

The converter has one flying capacitor with a capacitance of 2nF and a switching frequency of 100 MHz. The C_{out} is swept from 1 to 40 nF. The continuous line represents the output impedance value as calculated by means of Makowski's Model and Seemans' optimization [4]: the old model. For small values of C_{out} one can observe a deviation between this model and Spice simulations of up to 200 %. The new Model—presented in this paper—will take the Output buffer size into account and fit the simulations perfectly.

5.2 Makowski

In Fig. 7 the output impedance of a Makowski converter with ideal VCR of $\frac{4}{5}$ is plotted in function of C_{out}. The converter has three flying capacitors, C_1 C_2 C_3, with respectively a capacitance of 0.25, 0.25 and 0.5 nF. The switching frequency is 10 MHz. The C_{out} is swept from 1 to 10 nF. The continuous line in Fig. 7 represents the output impedance value as calculated by means of Makowski's Model [1] and Seemans' optimization [4]: the old model. For small values of C_{out} one can observe a deviation between this model and Spice simulations. The new model fits the simulations perfectly.

6 Ripple

Although reducing the output capacitor size reduces the converter's output impedance, the output capacitor cannot be omitted at all. The size of the output capacitor has a significant impact on the output voltage ripple. If output capacitance is decreased, the output voltage ripple increases. In Eq. 14 an approximation of the peak-to-peak voltage of the ripple component at the converter output is given. κ_T is a topology dependent constant and introduces the additional damping of the ripple by means of the minimum amount of flying capacitance that is connected to the output node during either one of the converter phases. Thus damping is provided both by the output capacitor and the flying capacitors. For the 4/5-topology $\kappa_T = 0.25$ and for the 1/2-topology $\kappa_T = 1$.

$$V_{\text{ripple}} = \frac{I_{\text{load}}}{2f_{\text{sw}}(C_{\text{out}} + \kappa_T C_{\text{fly}})} \tag{14}$$

This approach only holds in the SSL, in the FSL the parasitic resistance of the switches and interconnect introduces additional damping to the SSL ripple [7].

7 Measurements

For sake of validation measurements are performed on two switched capacitor structures in 90 nm CMOS: a $\frac{2}{3}$-ratio

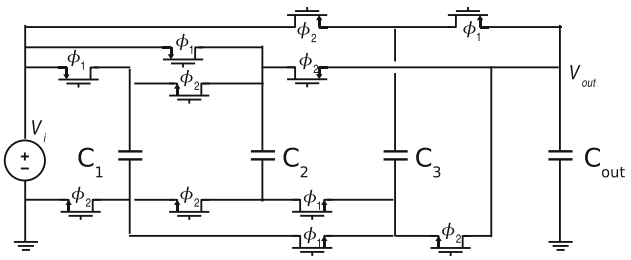

Fig. 8 Schematic representation of a capacitive 2/3 converter topology

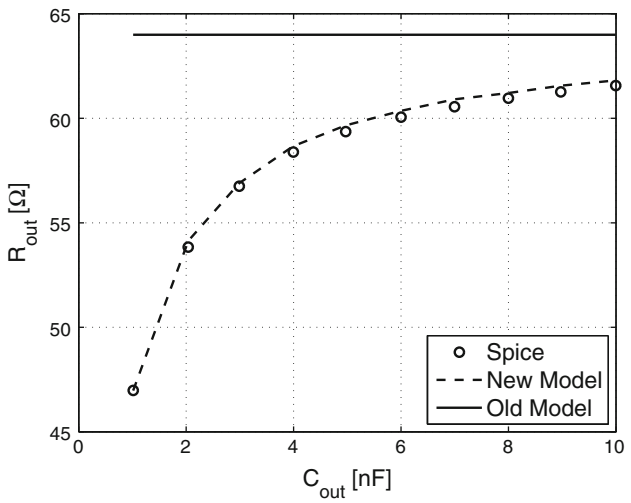

Fig. 7 Output impedance of a 4/5 capacitive DC–DC converter as a function of the output capacitor size

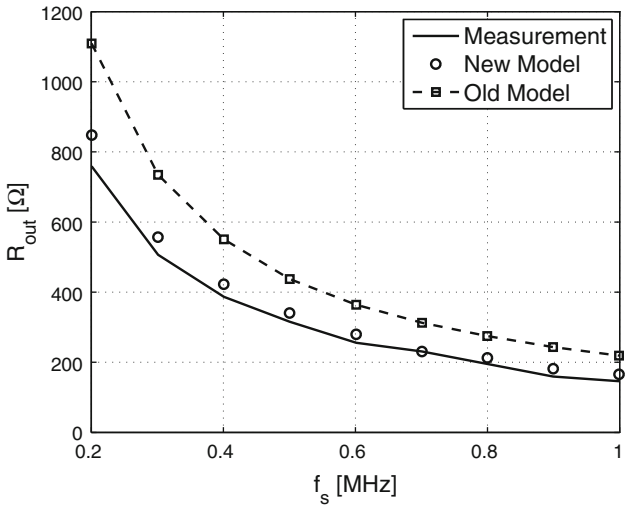

Fig. 9 Comparison of the output impedance models of a capacitive 2/3 DC–DC converter w.r.t the measurements

converter and a $\frac{4}{5}$-ratio converter. The output impedance is determined by means of accurate output voltage and output current measurements. High accuracy HP34401A multimeters are used for this purpose. The results are shown in Fig. 9 and in Fig. 10. They both have a total flying capacitance of 2 nF and an output buffer capacitance of 3.2 nF. The switching frequency was varied externally in order to retrieve the output impedance in function of the switching frequency. The 4/5-converter has a topology as presented in Sect. 5.2 and the 2/3-topology is shown in Fig. 8. A Photograph of the test-structures is shown in Fig. 11.

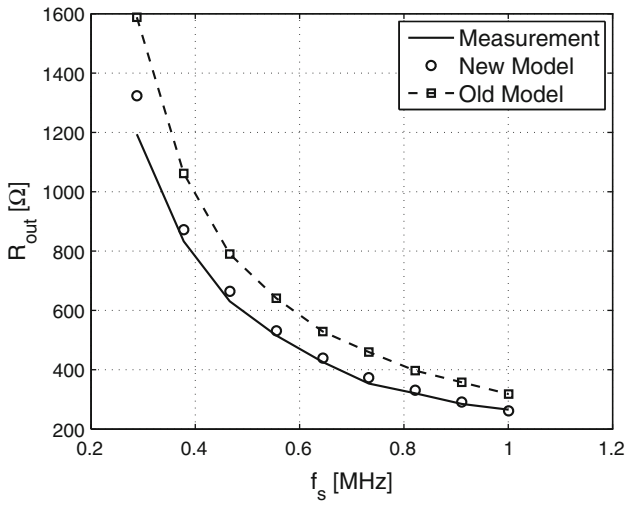

Fig. 10 Comparison of the output impedance models of a capacitive 4/5 DC–DC converter w.r.t the measurements

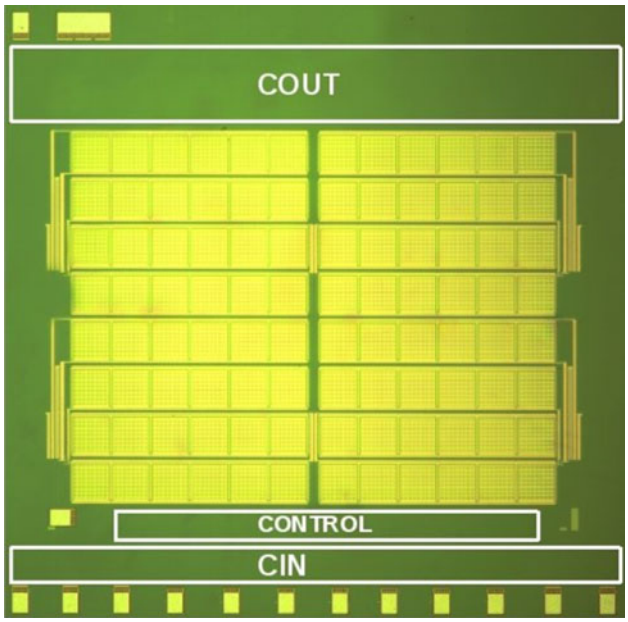

Fig. 11 Microphotograph of the test structures: both a 4/5 and 2/3 topology are implemented on a single integrated circuit, but measured separately

The model based on [4] is marked with the squares, the measurements with the solid line and the improved model by the round marks. Measurements show that in both cases the improved model shows a model accuracy improvement up to 30 %. These measurements validate the improvements made to the conventional model which is discussed in the previous sections.

8 Conclusion

In this paper an improved model for capacitive DC–DC converters is presented. In contrary to the state of the art models, this model takes the size of the output buffer capacitor into account. It was proven mathematically and by measurements that the size of the output buffer has a considerable influence on the output impedance of this type of converter. The model was verified by means of Spice simulations for two topologies and measurements of two test structures in 90 nm CMOS technology.

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