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MIXED SIGNAL LETTER

A termination scheme using intended asymmetric spatial filter response for averaging flash A/D converter

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Abstract Averaging network is adopted to reduce the front-end amplifier's offset in the flash analog-to-digital converter (ADC) commonly at the cost of the boundary threshold error. Such error worsens the integral-nonlinearity and introduces distortion. An averaging termination scheme using intended asymmetric spatial filter response is proposed to overcome this problem. It matches the impulse response window width, W_{IR}, to the active zero-crossing response window width, W_{ZX} at the boundary of network. Analysis and simulation show that by tuning the ratio between termination resistor R_T and averaging resistor R_1, the boundary error is reduced as close as to 1%. This method provides sufficient reliability since the resistance matching can be fabricated as high as 1% in modern CMOS technology. Its feasibility for the flash ADC has been validated by a 1GS/s 4-bit flash converter.

Keywords Asymmetric spatial filter · Averaging network · Offset · Flash ADC · Resistor

1 Introduction

High-speed low-to-medium resolution analog-to-digital converters (ADCs) are required in the communication receivers for Quadrature Amplitude Modulation (QAM), disk read channels and Ultra-Wideband (UWB) receivers [1]. The analog signal is sampled at Giga-Hertz and digitized to no more than 6 bits. At this relatively low resolution, the straight forward full-flash architecture seems best suited for the high speed data converter. However, flash ADCs in CMOS technology suffer greatly from random offsets in the comparators which can easily exceed the least significant bit (LSB) [2], defined as

$$3\sigma V_{\text{os,comp}} \leq \frac{1}{2}\text{LSB} = \frac{V_{\text{FS}}}{2^{N+1}} \quad (1)$$

where $\sigma V_{\text{os,comp}}$ is the mean square root value of the comparator offset, V_{FS} is the full-scale range of the converter and N is the resolution. Although the dynamic offset generated by the clocked latch can be reduced by the preamplifier, the spread in the threshold voltages of the preamplifier always limit the overall performance [3]. Such spread error scales down inversely as the square root of the input transistors' sizes [4] but at the expense of high parasitics which deteriorate available bandwidth. The key to realize good resolution at high speed ADC therefore lies in efficient methods to resolve such speed and resolution trade-off.

Offset averaging is one such method that can be applied to preamplifier array in flash ADCs [5]. Rational designed averaging network would improve the array offset performance by 3–4 times without enlarging preamplifiers area [6]. But any kind of averaging network generates boundary threshold offset due to the finite network configuration. More than 1bit linearity loss resulting from averaging edge stimulates various forms of averaging termination schemes to smooth out the random mismatch across the preamplifier array. Either dummy amplifiers with sufficient number to preserve an infinite character of array or special termination circuits to compensate edge offset are used in previous works [7–10]. But large number of dummies would waste

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the full scale range and consume too much power, on the other hand, special termination always requires delicate controlling of amplifier's transconductance which is not very efficient.

The proposed termination technique generates an intended asymmetric spatial filter response matching the impulse response window width, W_{IR}, to the active zero-crossing response window width, W_{ZX} at the boundary of network [11]. Such way is composed of less active dummies and passive components, at the same time the boundary error is reduced as close as to 1%. The principle of such termination scheme is explained in the subsequent sections followed by an experimental 1 GS/s 4bit flash ADC prototype.

2 Averaging and spatial filtering

Infinite offset averaging was presented in an array of preamplifiers of flash ADC, whose load resistors R_0 connect to nearest neighbors with lateral averaging resistors R_1 as shown in Fig. 1 [5]. The difference between analog input and reference voltage generates the signal dependent output current to the averaging resistor network. Figure 2(a) is used to simplify the analysis. Here the full differential circuit is replaced by the single end configuration and zero-crossing current source is simplified to an ideal current source. Each zero-crossing branch $I_s(n + i)$ contributes to a certain output current $I_{out}(n)$. It is obvious that such contribution depends on the distance away from the node n. For eg., $I_s(n)$ contributes larger than $I_s(n \pm 1, 2, 3\ldots)$. Considering an arbitrary node n, Kirchhoff's current law (KCL) requires that

$$I_s(n) = I_{out}(n) + (I_{out}(n) - I_{out}(n+1))\frac{R_0}{R_1} + (I_{out}(n) - I_{out}(n-1))\frac{R_0}{R_1} \quad (2)$$

The z and inverse z transform yields the spatial impulse response as follows [11],

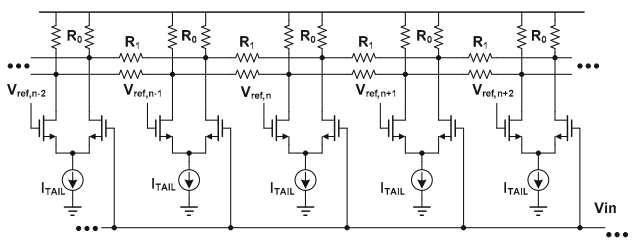

Fig. 1 Infinite resistor averaging network

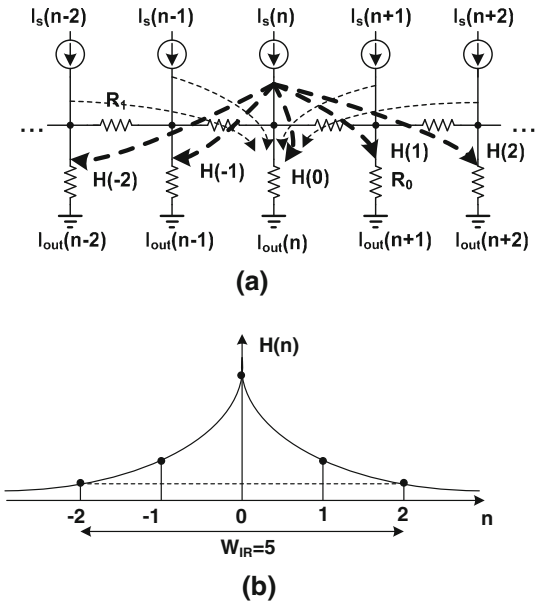

Fig. 2 The symmetric spatial filter response of the resistor averaging network. **a** Branch current distribution. **b** Spatial filter response

$$h(n) = b^{-|n|},\ b = e^{-|a\cosh(1+R_1/(2\times R_0))|}$$
$$H(n) = \frac{h(n)}{\sum_i h(i)} \quad (3)$$

Here $h(n)$ and $H(n)$ are relative current distribution to the main current $I_{out}(n)$ and normalized response to the overall input current as plotted in Fig. 2(b). The current distributions outside the impulse response window, W_{IR}, are all neglected. Until now the impulse response is only defined by the ratio of R_1/R_0. Although delicate analysis has proved that small R_1/R_0 improves the DNL/integral-nonlinearity (INL) better [3], a practical ratio about one is often chosen since preamplifiers gain shrinks with small R_1. Under such situation, the spatial filter has a decided characteristic with W_{IR} equal to 5. Actually $h(n)$ outside W_{IR} decreases seriously resulting in the value less than 5%.

Considering a true analog input varying randomly across the full scale range, the preamplifiers in the front-end array have different operation states dependent on the voltage headroom between their reference voltages and the analog inputs. All the zero-crossing cells are implemented by differential pairs, their static $V - I$ characteristic and zero-crossing response is shown in Fig. 3. Here zero-crossing window width, W_{ZX} is defined by

$$W_{ZX} \approx \frac{2\sqrt{2}V_{ov}}{LSB} + 1 \quad (4)$$

where V_{ov} is the overdrive voltage of input MOS transistors. The zero-crossing cells outside the W_{ZX} only generate the tail current to the averaging network. For an ADC,

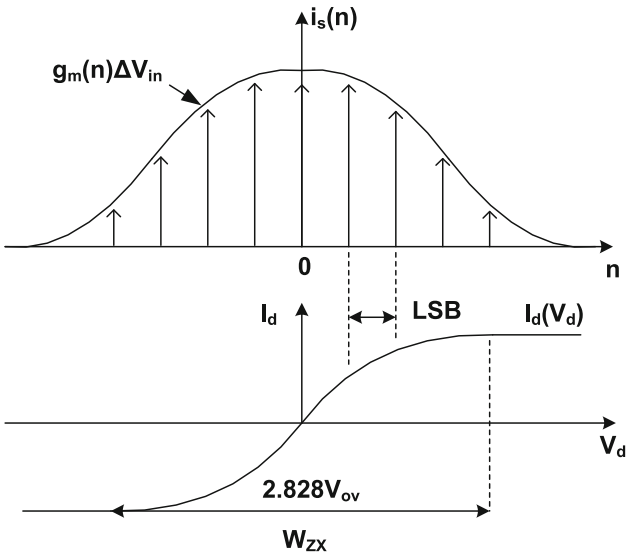

Fig. 3 Zero-crossing response

whose resolution is decided, the W_{ZX} is almost fixed because the overdrive voltage of MOS pair ranges from 150 to 300 mV in the typical applications due to both the speed and linearity requirements. Assuming the LSB is 25 mV, then the W_{ZX} width approximates 15 which is much larger than the typical W_{IR}.

3 Asymmetric spatial filter scheme for averaging termination

3.1 Averaging termination error analysis

The typical averaging network used in the flash ADC is the same as shown in Fig. 1 with finite number of preamplifiers. Such finiteness of the preamplifiers array poses unique problems at the boundaries when utilized in an averaging flash ADC. Usually the array reaches ends at the upper and lower limits of the full scale range. This will disrupt averaging at the last few amplifiers, because at the end nodes there is no longer equal zero-crossing current distribution into the resistor network from both left and right sides. To analyze the error at the averaging network edge, a 4-bit flash configuration is adopted and there are 15 preamplifiers at the front-end as shown in Fig. 4. There is no scheme to modify the edge error. Based on the analysis in Sect. 2, W_{IR} equal to 5 and W_{ZX} equal to 15 are assumed.

At the network edge, the effective W_{IR} only include 3 preamplifiers and W_{ZX} only comprise 8 preamplifiers. Both windows are not full as their own widths. Now let us focus on the current branch on the right end. Since W_{IR} is 5, preamplifier A1, A2, A3 contribute current to the right end branch as follows:

$$\begin{aligned} i_{out}(n) &= g_m(v_{in} - n\Delta)H(0) \\ &\quad + g_m(v_{in} - (n-1)\Delta)H(1) \\ &\quad + g_m(v_{in} - (n-2)\Delta)H(2) \\ &= g_m\Delta \times (H(0) + H(1) + H(2)) \\ &\quad \times \left(\frac{v_{in}}{\Delta} - n + \frac{H(1) + 2H(2)}{H(0) + H(1) + H(2)}\right) \end{aligned} \tag{5}$$

When output current becomes zero, the zero-crossing point is

$$v_{in} = n\Delta - \frac{H(1) + 2H(2)}{H(0) + H(1) + H(2)}\Delta \tag{6}$$

So the edge error (EDE) is

$$\text{EDE} = -\frac{H(1) + 2H(2)}{H(0) + H(1) + H(2)}\Delta \tag{7}$$

Here Δ is the symbol of LSB, $H(n)$ means absolute spatial filter response. This result shows that in the presence of the

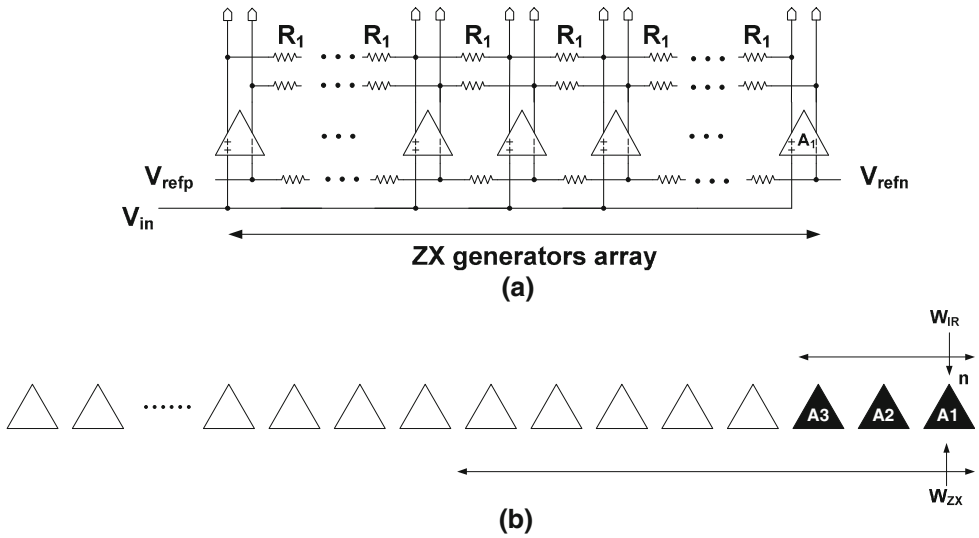

Fig. 4 4-bit flash ADC front-end averaging map without any termination. **a** Circuit configuration. **b** Simplified map

averaging resistors, those contributed positive currents to the edge node effectively pull the zero-crossing point toward the center of the array. Unless the positive current contributions are compensated by the negative ones from dummies or by distorting reference voltages, all the zero-crossings within the range of $W_{IR}/2$ at each edge are pulled, resulting a systematic INL. Some active averaging termination techniques are published. However they are always complicated due to delicate controlling of the input transconductance [1, 7–9].

3.2 Asymmetric spatial filter scheme

Until now all of the termination techniques try to compensate the edge error based on the decided spatial filter scheme as shown in Fig. 2(a), which is symmetric. The proposed way modifies such scheme to an asymmetric style matching the finite averaging network which is asymmetric also. The new averaging circuit is shown in Fig. 5 as follows.

There are three main differences from the original averaging network: 1) two dummies inserted, 2) two ends cross-connected, 3) termination resistor R_T used to tune the spatial filter characteristics. It is clear that the impulse response window W_{IR} is full again, meaning that new balance can be realized by including the two dummies D2 and D3, at the same time only D2 is added to the zero-crossing response window W_{ZX}. The amplifiers A1, A2, A3 and D2 work in the linear region while D3 operates in the saturation state. The modified current distribution in the node n can be calculated as

$$\begin{aligned} i_{out}(n) = {} & g_m(v_{in} - n\Delta)H(0) \\ & + g_m(v_{in} - (n-1)\Delta)H(-1) \\ & + g_m(v_{in} - (n-2)\Delta)H(-2) \\ & + g_m(v_{in} - (n+1)\Delta)H(+1) \\ & - I_{TAIL}H(2) \end{aligned} \tag{8}$$

Here the sequence $H(n)$ indicates the current contributions dependent on the symmetric spatial filter response and relative positions of the preamplifers. Using the same method as in the last section, the new EDE can be defined as

$$\mathrm{EDE} = -\frac{H(-1) - H(1) + 2H(-2) - \frac{H(2)V_{ov}}{\Delta}}{H(0) + H(1) + H(-1) + H(-2)}\Delta \tag{9}$$

The new form of the EDE provides the possibility to cancel itself in a proper combination of the spatial filter response $H(i)$. Considering the modern CMOS technology, the factor V_{ov}/Δ ranges from 5 to 10. Here the factor is assumed 5.5. Now the edge error is dependent only on the $H(i)$, which is tuned by the ratio of termination resistor R_T and R_1. In the

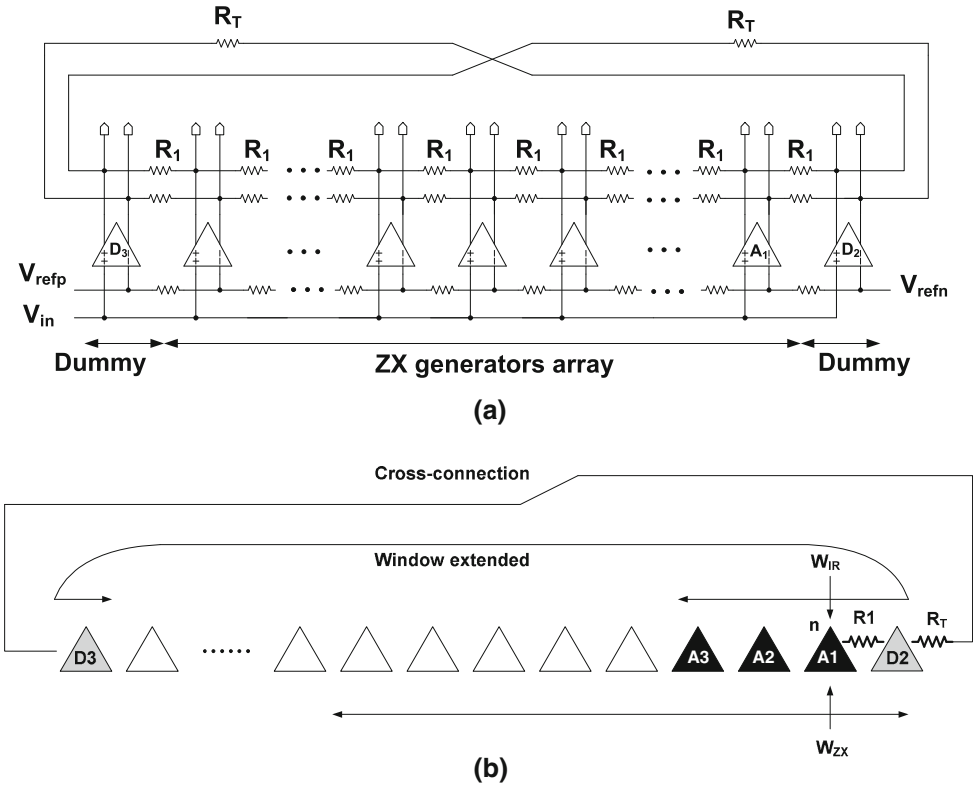

Fig. 5 4-bit flash ADC front-end averaging map with asymmetric spatial filter scheme which extending the width of W_{IR}. **a** Circuit configuration. **b** Simplified map

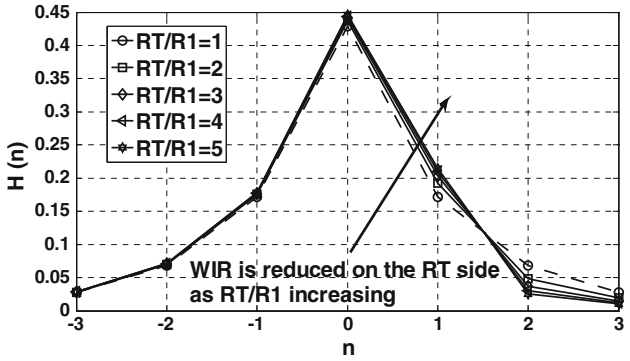

Fig. 6 Asymmetric spatial filter scheme with tuned R_T/R_1

Table 1 Asymmetric spatial filter response $H(i)$

R_T/R_1	$H(-2)$	$H(-1)$	$H(0)$	$H(1)$	$H(2)$
1	0.068	0.171	0.428	0.171	0.068
2	0.070	0.174	0.436	0.192	0.048
3	0.070	0.176	0.441	0.203	0.037
4	0.071	0.177	0.444	0.210	0.030
5	0.071	0.179	0.447	0.218	0.025

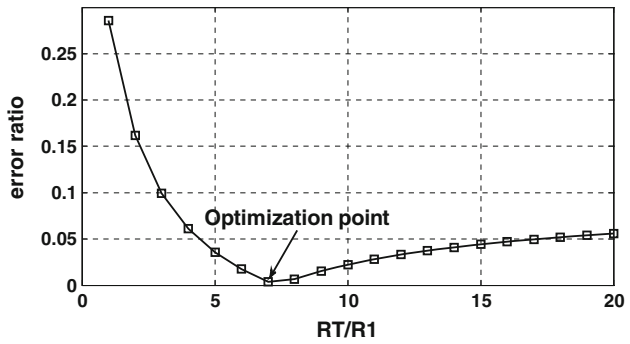

Fig. 7 Boundary resistance ratio tuning optimization

ideal averaging network, the equivalent resistances seen at each node from both left and right sides are the same. If a different R_T is inserted, this symmetric architecture is disrupted. Such effect can be plotted in Fig. 6. Using the same method in [3], the modified spatial filter response $H(i)$ is listed in Table 1. The spatial filter response is not anymore symmetric and $H(i)$ at the R_T side keeps reducing as the increasing R_T/R_1. It generates sufficient tuning space for adjusting the EDE as shown in Fig. 7. Simulation proves that a ratio of 7 corresponding to the error less than 1%. Moreover, the curve of Fig. 7 is quite flat around the optimum point which is good with respect to variation of R_T/R_1 due to the CMOS technology.

4 An experimental 1 GS/s 4-bit flash ADC using asymmetric spatial filter scheme

The proposed asymmetric spatial filter termination scheme is applied to a 1 GS/s 4-bit sub-sampling flash ADC to validate its performance, which is designed for UWB application with 400 mV full scale range. The experimental ADC is design in SMIC 0.13 μm CMOS technology with a 1.2 V power supply. A passive high pass filter operates for level shifting. A high speed Track and Hold Amplifier (THA) samples the input signal and its output goes through the averaging network to the comparators array. The circuit is designed with $R_1 = 600$ ohm, $R_0 = 660$ ohm, and $R_T = 4.8$ Kohm. The utilized P+ Poly SAB resistor has 3-sigma value at 0.5% level, which is high enough for 4-bit resolution in our UWB application. At the same time, if high matching behavior is required, the mirrored shuffle layout pattern can be utilized as mentioned in [12]. The layout of the ADC is shown in Fig. 8 and it occupies an active chip area of 0.6 mm^2. The ADC using and not using asymmetric filtering scheme is simulated both at the sub-sampling full swing input. Their output

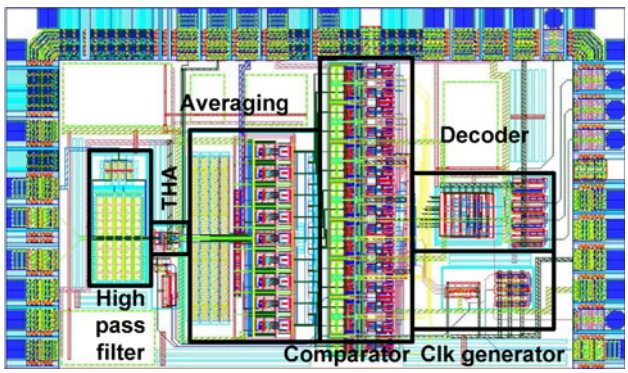

Fig. 8 The layout of the experimental ADC

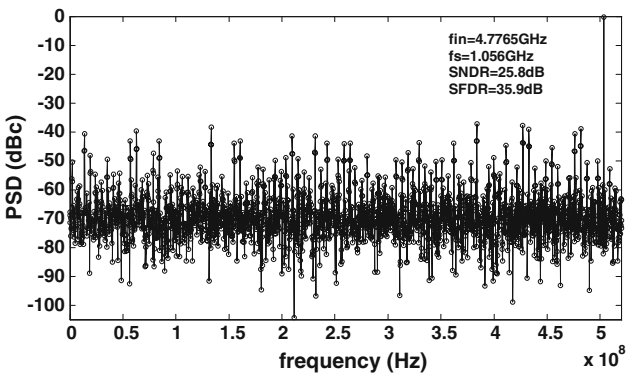

Fig. 9 The spectrum of the flash ADC using asymmetric spatial filter scheme

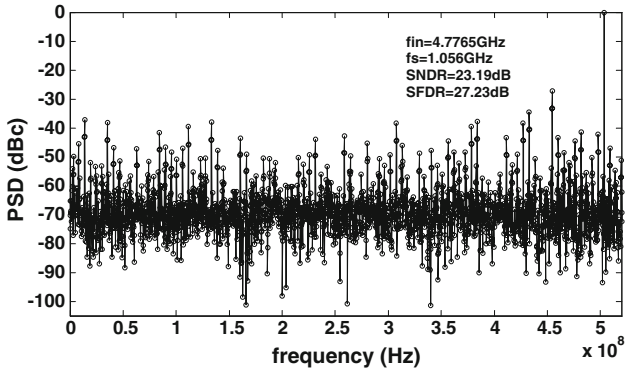

Fig. 10 The spectrum of the flash ADC using no special termination

Table 2 Summary of the experimental results

	This work	Xia [7]	Kai [8]
Input bandwidth (GHz)	4.8	0.413	0.8
CMOS technology	130 nm	180 nm	180 nm
Supply (V)	1.2	1.8	1.8
SNDR (dB)	25.8	34.8	32.2
FoM (pJ/step)	0.12	2.6	6

spectrum is depicted in Figs. 9 and 10 respectively. A 25.8 dB SNDR and 35.9 dB SFDR results in 4-bit ENOB at the first mode, at the same time 8.7 dB linearity loss happens without asymmetric termination. A short summary of the experimental results is listed in Table 2. It can be concluded that the proposed termination technique is a power efficient way to improve the low-to-medium resolution flash ADC.

5 Conclusion

A new averaging network termination scheme for flash ADC is presented that the edge error is relieved efficiently. This is implemented by adding less dummies than previous works and termination resistors in the cross-connection style, generating an asymmetric spatial filter response. The error source and improvement analysis is presented and a experimental 1 GS/s 4-bit flash ADC in 0.13 μm CMOS technology is designed to validate the scheme performance. The optimized error ratio is less than 1% while the ADC loses more than 1-bit linearity without the proposed scheme. Only two dummies are required which consumes much less power than the normal approaches.

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