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A Bandwidth Enhanced Transimpedance Amplifier with Improved Noise Performance

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Abstract A new TIA topology with enhanced bandwidth is presented in this paper. By adding an extra capacitive feedback loop to the resistive feedback TIA, bandwidth and sensitivity are increased without sacrificing the low power consumption. It is shown that this topology is superior to the self-compensated TIA when the photodiode is integrated on the same die as the TIA. An implementation is presented that boosts the bandwidth by a factor of 9 and reduces the noise by a factor of 4.2 for a photodiode capacitance of 106 pF, the parasitic capacitance of a POF-compliant 1 mm integrated photodiode in 130 nm CMOS.

Keywords Amplifiers · CMOS analog integrated circuits · Data communication · Optical communication · Optical receivers

1 Introduction

In optical receivers, the conversion from the optical to the electrical domain is realized by means of a photodiode. Photons with an energy higher than the bandgap create electron–hole pairs. By separating the electrons from the holes with an electrical field, a current is generated which is sensed by a transimpedance amplifier (TIA).

To obtain a high receiver sensitivity it is important to collect all light leaving the fiber. Therefore the diameter of the photodiode needs to be at least as large as the diameter of the fiber. Typical fiber diameters are between 8 and 10 μm for single-mode fiber and 50 μm for multi-mode fiber. The drawback of communication systems that make use of these types of fiber is the high cost. Nowadays there is a growing interest in low-cost optical communication systems for consumer applications. Plastic optical fibers (POFs) are preferred because the fiber, associated connectors and installation are all inexpensive. A typical core diameter for POF is 980 μm.

To decrease the cost to the minimum level, the whole receiver, including the photodiode, must be integrated on a single chip in CMOS. In [1] such a receiver is described for applications where a multimode fiber is used. The diameter of the integrated photodiode is 60 μm resulting in a parasitic photodiode capacitance of 1 pF at each side of the differential photodiode structure. This parasitic capacitance is determined by the area, the reverse voltage and the doping concentrations. It is a very important parameter because it determines the speed, sensitivity and power consumption of the complete receiver. Keeping it as low as possible is of the utmost importance.

For POF applications, the area of the photodiode needs to be a lot larger than in [1]. A receiver with a large-area integrated photodiode is presented in [2]. In a 0.6 μm BiCMOS process an optical receiver with a PIN photodiode, having a diameter of 500 μm, is integrated. A parasitic capacitance of only 2.2 pF for a reverse voltage of 2.5 V is obtained due to the availability of an intrinsic layer which increases the width of the depletion region. This value is almost as small as the parasitic photodiode capacitance in [1] where the area is a factor of 70 smaller. However, no intrinsic layer is available in standard CMOS technologies.

In [3, 4] a technique is presented to reduce the capacitive loading of the photodiode at the input of the TIA. The idea is to reduce the transient voltage across the photodiode. The charging and discharging current of the photodiode capacitance is reduced accordingly and therefore the bandwidth of the receiver is increased. This technique requires the ability

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to access both the cathode and the anode of the photodiode. For an integrated photodiode in standard CMOS, the best choice for the p-type material is the p-substrate [1, 5]. As the substrate is grounded, this technique is not applicable for receivers with an integrated photodiode.

In this paper a new TIA topology is presented that reduces the pernicious effect of the photodiode capacitance. In contrast with the technique presented in [3, 4], this new topology is compatible with integrated photodiodes. Moreover, the noise contribution of this new topology is lower, so a higher signal-to-noise ratio (SNR) can be obtained.

In Sect. 2 some issues about the integration of photodiodes in a CMOS process are discussed. In Sect. 3 the new TIA topology is compared to the one presented in [3, 4] in terms of noise, bandwidth and power consumption. An implementation of the new topology is presented in Sect. 4. The paper is concluded in Sect. 5.

2 Large-area integrated photodiodes

It is assumed from now on that an n-well to p-substrate photodiode takes care of the conversion of the incoming light power to an electrical current. In [1, 5] it is shown that this is the best choice in terms of responsivity and parasitic capacitance. The latter figure is the one of interest here as the proposed topology aims at reducing its detrimental effect.

The photodiode capacitance C_d can be calculated with the following formula:

$$C_d = C_{d,bp} \cdot A + C_{d,sw} \cdot P, \tag{1}$$

where $C_{d,bp}$ and $C_{d,sw}$ are the bottom plate capacitance per unit area and the sidewall capacitance per unit length respectively. A and P represent the area and perimeter of the photodiode. For a photodiode with a diameter of 1 mm to be compatible with POF, the area and perimeter are given by:

$$A = 785000\,\mu\text{m}^2$$
$$P = 3142\,\mu\text{m}.$$

$C_{d,bp}$ and $C_{d,sw}$ are both dependent on the reverse voltage over the junction. For the 130 nm CMOS technology which is used in this paper and for a reverse voltage of 0.6 V (half of the nominal supply voltage of the technology) the values are as follows:

$$C_{d,bp} = 0.131\,\text{fF}/\mu\text{m}^2$$
$$C_{d,sw} = 1.0474\,\text{fF}/\mu\text{m}^2.$$

With these numbers, the total photodiode capacitance C_d can be determined to be 106 pF, a value that is a factor of 50–100 larger than in previous publications which is due to the large-area photodiode and the fact that it is integrated in a standard CMOS technology.

3 Bandwidth Enhanced TIA topologies

With such a large parasitic capacitance at the input of the receiver it is a challenge to obtain a high bandwidth. Two circuit techniques are therefore discussed that alleviate the effect of this parasitic capacitance.

3.1 Self-compensated TIA

A first solution to circumvent the detrimental effects of a large photodiode capacitance is the self-compensated TIA [3, 4]. A block diagram of this topology is shown in Fig. 1(a). Two feedback loops can be distinguished. The first loop is composed of resistor R_f and an inverting amplifier with amplification A. Due to the inverting amplification over the resistor, the input resistance is a factor A lower than R_f. The second feedback loop exists only out of a non-inverting amplifier with amplification B. Its function is to make sure that the transient voltage across the photodiode is reduced. This reduced voltage swing results in a smaller effective input capacitance. The resistance and capacitance that determine the bandwidth of the system are both reduced by the first and second loop respectively and therefore the bandwidth of the system is increased.

The transfer function of this TIA is given by:

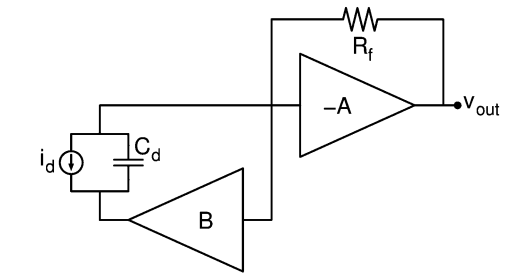
$$\left(\frac{v_{out}}{i_d}\right)_1 = \frac{AR_f - R_A}{1 + A + sC_d\big((1+A)R_B + (1-B)(R_A + R_f)\big)} \approx \frac{R_f}{1 + sC_d\left(R_B + R_f\left(\frac{1-B}{A}\right)\right)}. \tag{2}$$

R_A and R_B represent the output resistance of the amplifier with amplification $-A$ and B respectively. They are assumed to be much smaller than R_f. It is also assumed that A is large. The effect of the second feedback loop is clearly visible in (2). If B equals 1, which is supposed from now on, the bandwidth of the receiver is only determined by R_B and C_d:

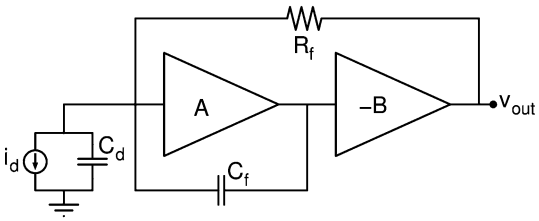
$$BW_1 = \frac{1}{2\pi R_B C_d}. \tag{3}$$

Consequently, to achieve a high bandwidth, a unity gain amplifier with a low output resistance R_B is needed.

Besides the transfer function from photocurrent to output voltage, also the noise behaviour of a TIA is important because the SNR determines the obtainable bit error ratio (BER). Three major noise contributors can be distinguished in Fig. 1(a): R_f and the two voltage amplifiers. Only thermal noise is considered. The output noise voltage spectral density of this topology is then given by:



(a) Self-compensated TIA.



(b) Capacitance relieved TIA.

Fig. 1 Bandwidth enhanced TIA topologies

$$\overline{dv_{n,out,1}^2} = \overline{dv_{n,R_f}^2} + \overline{dv_{n,A}^2} + \overline{dv_{n,B}^2}\left|\frac{sR_fC_d}{1+sR_BC_d}\right|^2, \tag{4}$$

where the same assumptions as before are made. In this formula, $\overline{dv_{n,R_f}^2}$ is the noise voltage spectral density of the feedback resistor whereas $\overline{dv_{n,A}^2}$ and $\overline{dv_{n,B}^2}$ are the input referred noise voltage spectral densities of the two voltage amplifiers. The three noise components in Eq. 4 are depicted in Fig. 2(a) where it is assumed that $\overline{dv_{n,B}^2} > \overline{dv_{n,A}^2}$ which is a typical situation for a unity gain buffer because no noise is suppressed by gain in a previous stage. To obtain the total output noise voltage, (4) is integrated from 0 Hz up till BW_1, the bandwidth of the self-compensated TIA. This results in the following formula:

$$\overline{v_{n,out,1}^2} = BW_1\left(\overline{dv_{n,R_f}^2} + \overline{dv_{n,A}^2} + \overline{dv_{n,B}^2}\frac{R_f^2}{R_B^2}\frac{4-\pi}{4}\right). \tag{5}$$

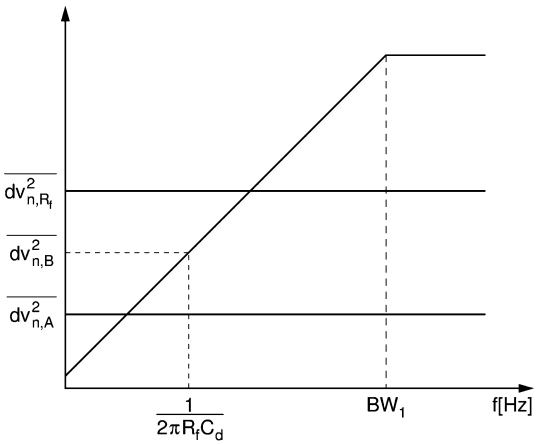
It can be concluded that it is especially amplifier B that determines the total noise voltage at the output.

3.2 Capacitance relieved TIA

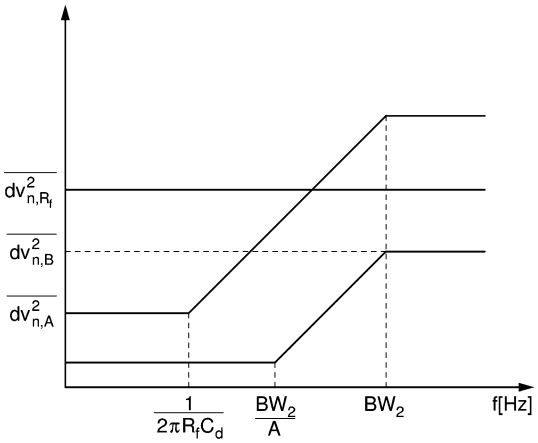
The schematic of Fig. 1(a) can not be adopted when the photodiode is integrated together with the circuit because the anode is then grounded. A new circuit that also enhances the bandwidth is therefore presented here. Its topology is depicted in Fig. 1(b). Again two feedback loops can be distinguished. The first loop is now composed of two amplifiers and resistor R_f. To make the voltage amplification over R_f inverting, one of the amplifiers is inverting while the other one is non-inverting. The objective of the inverting amplification is again to reduce the input resistance, by a factor AB now however. The second feedback loop is nested in the first one and consists of capacitor C_f and a non-inverting amplifier with amplification A. The function of this loop is to provide a negative capacitance at the input of the TIA. This negative capacitance appears in parallel with the photodiode capacitance. The result is that the effective input capacitance is decreased so that the bandwidth of the TIA is increased accordingly. The transfer function of the topology in Fig. 1(b) is given by (6). Again, it is assumed that R_A and R_B are negligible compared to R_f and that A is large. When B equals 1 and if it is assumed that the two poles in (6) are far from each other, the bandwidth of this TIA is given by:

$$\begin{aligned}\left(\frac{v_{out}}{i_d}\right)_2 &= \frac{ABR_f - R_B + sC_f(BR_AR_f - R_AR_B)}{1+AB+s\big(C_d(R_f+R_B)+C_f((1-A)(R_f+R_B)+(1+B)R_A)\big)+s^2C_dC_f(R_fR_A+R_AR_B)}\\ &\approx \frac{R_f\left(1+s\frac{C_f}{A}R_A\right)}{1+s\left(\frac{R_fC_d}{AB}-\frac{R_fC_f}{B}\right)+s^2\frac{R_fR_AC_dC_f}{AB}}.\end{aligned} \tag{6}$$

$$\begin{aligned}LG &= -AB\frac{1-\frac{s(R_f+R_B)C_f}{B}}{1+s\big(C_d(R_f+R_B)+C_f(R_f+(1+B)R_A+R_B)\big)+s^2C_dC_f(R_fR_A+R_AR_B)}\\ &\approx -AB\frac{1-\frac{sR_fC_f}{B}}{1+sR_fC_d+s^2R_fR_AC_dC_f}.\end{aligned} \tag{7}$$



(a) Self-compensated TIA.



(b) Capacitance relieved TIA.

Fig. 2 Noise voltage spectral densities at the output of the self-compensated TIA and the capacitance relieved TIA

$$BW_2 = \frac{1}{2\pi R_f \left(\frac{C_d}{A} - C_f\right)}. \tag{8}$$

It seems that BW_2 becomes infinite by choosing C_f a factor A smaller than C_d. However, in this case the two poles are not far from each other and the bandwidth is actually not given any more by (8). The zero in (6) is at a very high frequency if R_A is small and A is large. It is therefore neglected from here on.

For frequencies below BW_2 where the second pole and the zero can be neglected, the output noise voltage spectral density of this topology is given by:

$$\overline{dv^2_{n,out,2}} = \overline{dv^2_{n,R_f}} + \overline{dv^2_{n,A}}\left|\frac{1 + sR_fC_d}{1 + \frac{s}{2\pi BW_2}}\right|^2 + \frac{\overline{dv^2_{n,B}}}{A^2}\left|\frac{1 + \frac{sA}{2\pi BW_2}}{1 + \frac{s}{2\pi BW_2}}\right|^2. \tag{9}$$

The three noise components are depicted in Fig. 2(b). It is assumed that R_f and both amplifiers are identical to those in the other topology to make a fair comparison. Therefore, also $\overline{dv^2_{n,R_f}}$, $\overline{dv^2_{n,A}}$ and $\overline{dv^2_{n,B}}$ are just as high as can be seen in Fig. 2. Equation 9 is integrated from 0 Hz up till BW_2, the bandwidth of the capacitance relieved TIA, to obtain the total output noise voltage. This results in the following formula:

$$\overline{v^2_{n,out,2}} = BW_2\left(\overline{dv^2_{n,R_f}} + \overline{dv^2_{n,A}}\frac{R_f^2}{R_B^2}\frac{4-\pi}{4} + \overline{dv^2_{n,B}}\frac{4-\pi}{4}\right). \tag{10}$$

For the presented topology it is especially amplifier A that determines the total noise voltage at the output.

Like for every feedback system, stability should be verified for the capacitance relieved TIA. Only a single loop gain needs to be considered because the two feedback loops are nested and can therefore be cut in one time. This is shown in Fig. 3. The loop gain LG is then determined by (7). Again it is assumed that R_A and R_B are significantly smaller than R_f. C_f is also supposed to have a significantly lower capacitance than C_d which will be confirmed later as a necessary condition to guarantee a stable operation. It can be noticed in (7) that the loop gain has two poles and a positive zero. The second pole can however be ignored as it is located at a very high frequency. The system can therefore become unstable as a positive zero shifts the phase with $-90°$ just as a pole would do. However, the magnitude rises again with 20 dB/decade just as a negative zero does. The possibility therefore exists that the gain is larger than 1 when the phase has shifted with $-180°$ so that the system becomes unstable. In order to prevent this, the following condition needs to be fulfilled:

$$A\frac{C_f}{C_d} < 1 \iff C_f < \frac{C_d}{A}. \tag{11}$$

This means that eventually, the magnitude of LG drops below 1 so that there is no gain any more at the frequencies where the phase has shifted with $-180°$ (Fig. 4) .

3.3 Comparison

It is assumed from now on that C_d, R_f, and both amplifiers are the same for both topologies. From Eqs. 3 and 2 it follows

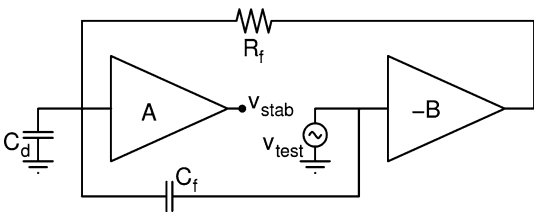
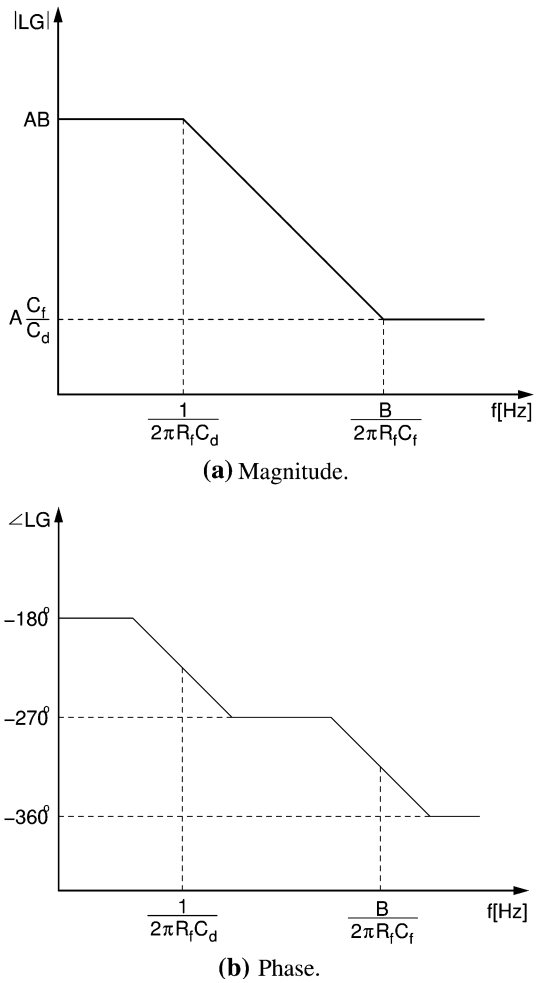


Fig. 3 Test setup to analyze the loop gain of the capacitance relieved TIA



(a) Magnitude.

(b) Phase.

Fig. 4 Loop gain of the capacitance relieved TIA

that both topologies have the same transimpedance gain. To make a fair comparison, BW_1 and BW_2 are made equal. This is possible due to the extra degree of freedom in the capacitance relieved TIA. C_f is then determined as follows:

$$C_f = C_d\left(\frac{1}{A} - \frac{R_B}{R_f}\right). \tag{12}$$

From Eqs. 6 and 10 it is clear that the new topology has a lower integrated noise voltage at the output. The SNR is thus higher which results in a lower BER. By fixing C_f at the value calculated in (12), the stability condition (11) is always fulfilled.

4 Implementation of a capacitance relieved TIA

By means of illustration, a circuit implementation in 130 nm CMOS of the capacitance relieved TIA is presented here. The schematic can be seen in Fig. 5. The two feedback loops can easily be distinguished. Amplification A is provided by a cascade of two inverting common-source stages. Amplification B on the contrary is provided by a third common-source stage. B is consequently larger than 1. For the presented topology this is not a problem, whereas for the self-compensated TIA B should always be smaller than or equal to 1 to prevent the circuit from oscillating.

The gain of an amplifier stage in Fig. 5 equals 16.5 dB. This means that A and B equal 44.67 and 6.68 on a linear scale respectively. The photodiode capacitance C_d is 106 pF to model an integrated photodiode with a diameter of 1 mm. R_f is fixed at 100 kΩ.

Because B is larger than 1, Eq. 8 does not hold any more. The bandwidth, which can be deduced from (6) is now given by:

$$BW_{TIA} = \frac{1}{2\pi R_f\left(\frac{C_d}{AB} - \frac{C_d}{B}\right)}. \tag{13}$$

When no capacitor C_f is added to the circuit, the bandwidth is not higher than 4.5 MHz. This can be seen in Fig. 6. If C_f equals 2.08 pF, the bandwidth increases to 40.4 MHz. Without any supplementary power consumption, the bandwidth is increased by a factor of 9. This case is also shown in Fig. 6. To reach a bandwidth of 40.4 MHz without capacitor C_f, the value of R_f should be decreased to 11.5 kΩ, decreasing the gain from input to output by almost a factor of 9. Again, this case is shown in Fig. 6. Everything is summarized in Table 1.

While the gain A and B determine the bandwidth, the noise of the receiver is determined by the current through the three amplifying stages and the value of R_f. Transistor M_1, M_2 and M_3 have a length of 120 nm, the minimal length of the technology, and a width of 250 µm. R_1, R_2 and R_3 have a value of 240 Ω. To obtain an optimal trade-off between power consumption, speed and noise, the overdrive voltage of all transistors is designed at 50 mV [1]. This results in a total power consumption of 11.94 mW if the supply voltage equals 1.2 V. To enable a fair comparison between all three presented cases, the integrated output noise is divided by R_f to obtain the equivalent

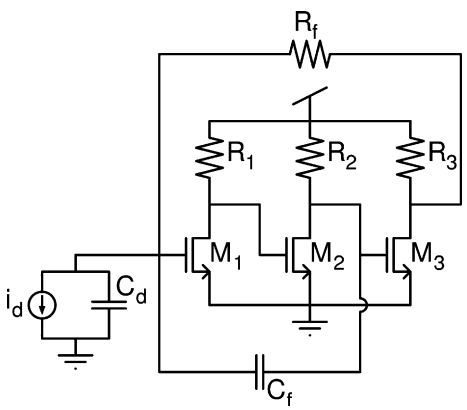


Fig. 5 Schematic of the capacitance relieved TIA

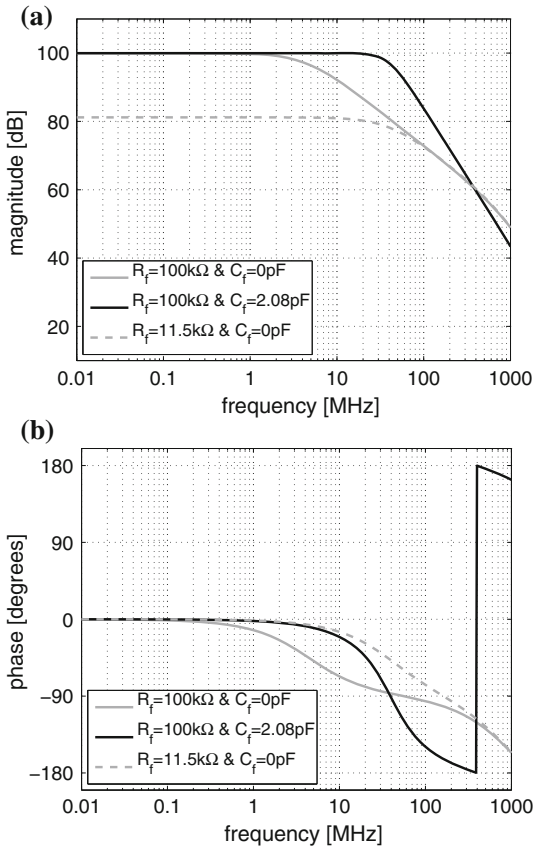


Fig. 6 Transfer characteristic of the capacitance relieved TIA for different values of R_f and C_f

Table 1 Overview of the presented design examples

R_f (kΩ)	C_f (pF)	BW_{TIA} (MHz)	RMS input noise (nA)
100	0	4.5	44.4
100	2.08	40.4	90.3
100	0	40.4	378.3

integrated input noise. These values are also listed in Table 1. The addition of C_f with a value of 2.08 pF results in an increase of the noise level from 44.4 to 90.3 nA. For a bandwidth increase by a factor of 9, the noise level only increases by a factor of 2. The equivalent integrated input noise when R_f is only 11.5 kΩ and no C_f is used adds up to 378.3 nA. For an equal bandwidth, the sensitivity of the receiver with a capacitor C_f of 2.08 pF is 4.2 times higher than when that bandwidth is obtained by reducing the value of the feedback resistor R_f.

5 Conclusion

A new TIA topology is presented that relieves the effect of a large photodiode capacitance on the receiver bandwidth. This is accomplished by adding a capacitive feedback loop to the resistive feedback TIA. An implementation in 130 nm CMOS is presented, having a transimpedance of 100 kΩ and a bandwidth of 40.4 MHz for a photodiode capacitance of 106 pF. The integrated equivalent input noise is not higher than 90.3 nA which is 4.2 times lower than that of a normal feedback TIA. The power consumption is only 11.94 mW.

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Michiel Steyaert received the master's degree in Electrical-Mechanical Engineering and the Ph.D. degree in Electronics from the Katholieke Universiteit Leuven (K.U. Leuven), Heverlee, Belgium in 1983 and 1987, respectively. From 1983 to 1986 he obtained an IWNOL fellowship (Belgian National Foundation for Industrial Research) which allowed him to work as a Research Assistant at the Laboratory ESAT at K.U.Leuven. In 1987 he was responsible for several industrial projects in the field of analog micro power circuits at the Laboratory ESAT as an IWONL Project Researcher. In 1988 he

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