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High efficiency, high switching speed, AlGaAs/GaAs P-HEMT DC–DC converter for integrated power amplifier modules

Han Peng · Vipindas Pala · Peter Wright · T. Paul Chow · Mona Mostafa Hella

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Abstract This paper presents a high efficiency, high switching frequency DC–DC buck converter in AlGaAs/GaAs technology, targeting integrated power amplifier modules for wireless communications. The switch mode, inductor load DC–DC converter adopts an interleaved structure with negatively coupled inductors. Analysis of the effect of negative coupling on the steady state and transient response of the converter is given. The coupling factor is selected to achieve a maximum power efficiency under a given duty cycle with a minimum penalty on the current ripple performance. The DC–DC converter is implemented in 0.5 μm GaAs p-HEMT process and occupies 2×2.1 mm^2 without the output network. An 8.7 nH filter inductor is implemented in 65 μm thick top copper metal layer, and flip chip bonded to the DC–DC converter board. The integrated inductor achieves a quality factor of 26 at 150 MHz. The proposed converter converts 4.5 V input to 3.3 V output for 1 A load current under 150 MHz switching frequency with a measured power efficiency of 84%, which is one of the highest efficiencies reported to date for similar current/voltage ratings.

Keywords Gallium Arsenide Technology · p-HEMT · Interleaved structure · Coupled inductors · DC–DC converters · Supply modulators

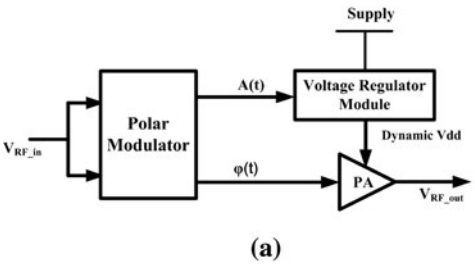
H. Peng (✉) · V. Pala · T. P. Chow · M. M. Hella
ECSE Department, Rensselaer Polytechnic Institute,
110 8th Street, Troy, NY 12180, USA
e-mail: pengh2@rpi.edu

P. Wright
Triquint Semiconductor Inc., Hillsboro, OR 97124, USA

1 Introduction

In wireless communication systems, the efficiency of the radio frequency power amplifiers (RF PA) dominates the power consumption of the radio transceiver. In addition, to improve spectral efficiency of communication standards, non-constant envelope modulations with high peak to average signal variations are being adopted. This translates to strict requirements on the power amplifier linearity to avoid signal distortion. Such highly linear amplifiers are inefficient, particularly at "backed-off" power conditions, where the power amplifier typically operates for most of its operating time. Polar modulation is an effective technique to alleviate the linearity-efficiency tradeoff [1–3]. As shown in Fig. 1a, the baseband signal is converted to envelope signal $A(t)$ and phase signal $\varphi(t)$. Since the phase signal has a constant amplitude, high efficiency switching power amplifier classes such as Class E and F can be utilized. The envelope varying information is restored by modulating the supply voltage of the PA through the output of an envelope modulator. Possible supply modulators include linear low-dropout (LDO) [4–6], switched-capacitor converters [7–9], switched-mode dc–dc converters [10–12], and hybrid- solutions [13, 14]. Among previously mentioned approaches, switch-mode DC–DC converters can provide the highest efficiency with acceptable bandwidth.

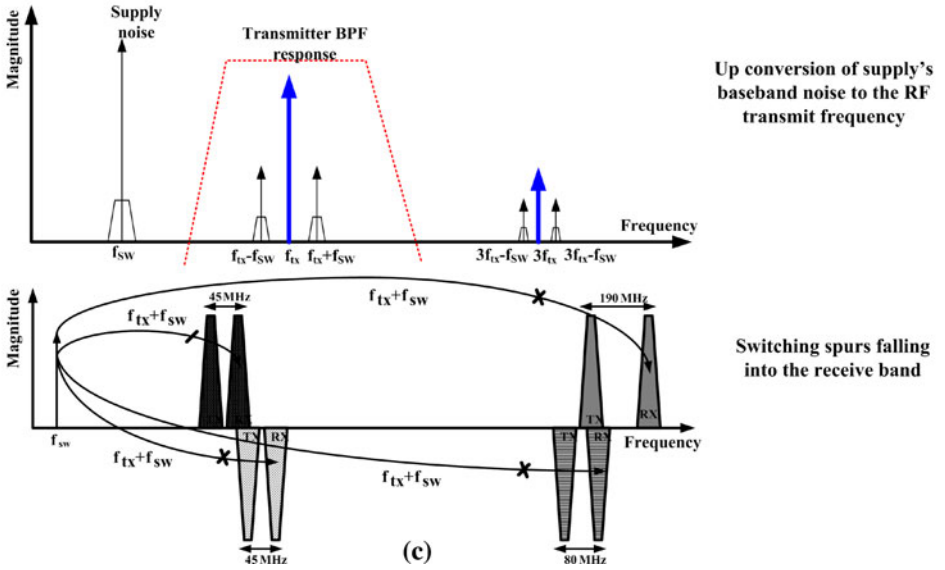
Traditional switch-mode DC–DC converters usually require inductors up 100 μH, and capacitors in hundreds of micro-Farads [15]. With the continuous trend in integrating various components of the communication system on the same die or the same package, increasing the switching frequency to the hundreds of MHz range will reduce inductors' and capacitors' sizes to the nano-Heneries and pico-Farads, where they can be implemented on-chip. Such



(a)

	Ftx (MHz)	Frx (MHz)	duplexer separation (MHz)
Band 1	1920 - 1980	2110 - 2170	**190**
Band 2	1950 - 1910	1930 - 1990	**80**
Band 5	824 - 849	869 - 894	**45**
Band 8	880-915	925 - 960	**45**

(b)



(c)

Fig. 1 Motivation for high switching speed DC–DC converters for power amplifier modules, **a** block diagram of polar modulator, **b** an example of duplexer separation for four WCDMA bands, **c** effect of switching frequency selection on the transmitter's and receiver's performance

integration level will simplify packaging, reduce the power loss from the interconnection of different dies and external components. In addition, the quality factor Q of on-chip inductors increases with frequency up to $\sim$1GHz, such that the higher switching frequency, the higher Q, and the less high frequency harmonic losses due to inductors' ac resistances.

Other factors also contribute to the selection of the appropriate switching frequency. For a given communication standard and its associated frequency band and channel separation, the switching frequency should be selected to avoid any switching spurs falling into the adjacent receiver band or switching noise lowering the PA adjacent channel power rejection (ACPR) in the transmitter (Fig. 1(b,c)). For example, in WCDMA standards, the duplexer separations of the four WCDMA bands are 190 MHz for band 1, 80 MHz for band 2 and 45 MHz for band 5 and 8 as shown in Fig. 1b. The up-converted supply baseband noise should not fall onto any of these frequencies. For other communication standards such as WiMAX and LTE, given that the control loop crossover frequency is around 1/10 $\sim$ 1/5 of the switching frequency, to achieve a control loop bandwidth up to 20 MHz for envelope modulation of high peak-to-average waveforms, the switching frequency of the DC–DC converter has to be higher than 100 MHz. Thus higher switching speed DC–DC converters can have major advantages in terms of both smaller passive devices and wider control bandwidth. However, due to frequency dependent loss components of the DC–DC converter such as the gate driver loss and the switching transistor loss, there is an optimum switching frequency beyond which the efficiency of the converter drops. This optimum switching frequency is a function of the used integration technology and the input/output voltage and current ratings.

Significant research efforts have been directed towards silicon integrated switching DC–DC converters [15–21], however either the switching frequency or the voltage/current ratings have been below those required for integrated power amplifier and transmitter modules. In this paper we propose the use of GaAs technology as the integration platform for high switching speed, high efficiency switching supply modulators. Given that GaAs has been and is expected to continue as the dominant process technology for power amplifier implementations for cellular standards, it is natural to integrate the supply modulator with the PA in the same technology. The paper is organized as follows; Section 2 presents the steady state and transient response of interleaved DC–DC converter topology and examines the effect of coupling of filter

inductors in the special case of two-stage interleaved architecture. Section 3 discusses the structure and properties of GaAs p-HEMT devices and their intrinsic advantages for power switches employed in DC–DC converters. Section 4 provides detailed circuit implementation, including output switches and gate driver circuit design, inductor design, closed loop control, and the power consumption analysis for different power loss components. Measurement results for the output stage and load network, and simulation results for the closed loop control are reported in Section 5. Finally, conclusions are drawn in Section 6.

2 Interleaved topology with negative coupled inductors

Multi-phase interleaved DC–DC converters have become widely adopted to reduce current ripple and improve efficiency [15–20]. Compared to a single buck converter, the multi-phase interleaved structure has more active components as well as more inductors which can increase the converter module size. Coupling the inductors has recently been proposed to improve the steady state and transient responses of the converter by reducing the current ripple and the stabilization time [22]. While the analysis given in [22] has proceeded by developing an equivalent inductance under different coupling conditions for the steady and transient conditions separately, we will extend this analysis by quantifying the optimum coupling factor for ripple cancellation under different duty ratios, and use space state analysis to derive an expression for the converter's open loop transfer function to study the bandwidth enhancement effect of coupled inductors.

2.1 Steady state analysis

Figure 2 shows the core of a two-stage interleaved structure with coupled inductors. Let us assume that the two branches have equal inductances L, the mutual inductance between the two phases is M, while $k = M/L$ is the coupling factor. The current and voltage waveforms at the input and output of the DC–DC converter for each phase, assuming ideal switching stages, are shown in Fig. 3. As can be seen from the figure, the circuit has four different states depending on the ON/OFF condition of switches SW1 and SW2. To find the current ripple in each converter phase, let us derive the relationship between the currents i_1, i_2 and the voltages at the input and output of the DC–DC converter during each state.

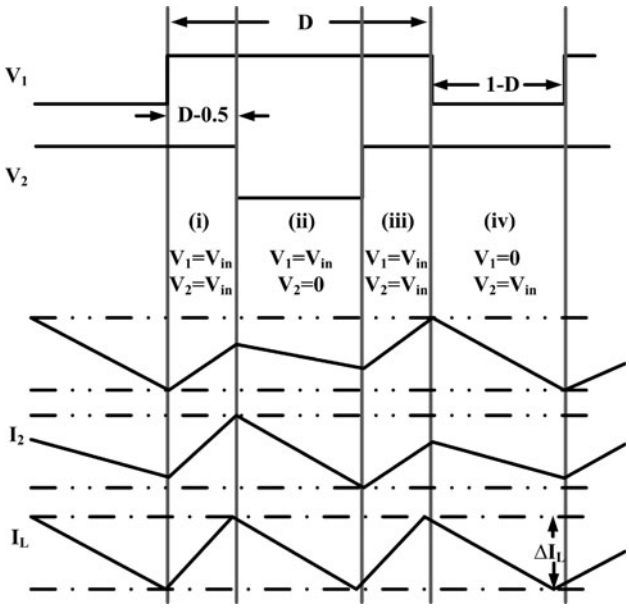


Fig. 3 Voltage and current waveforms at the terminals of the coupled inductors for $D \geq 0.5$

State I: $0 \leq t < (D - 1/2)T$

$$L_1 \cdot \frac{di_1}{dt} + M \cdot \frac{di_2}{dt} = V_{\text{in}} - V_{\text{out}} = V_{\text{in}}(1 - D) \quad (1)$$

$$L_2 \cdot \frac{di_2}{dt} + M \cdot \frac{di_1}{dt} = V_{\text{in}} - V_{\text{out}} = V_{\text{in}}(1 - D) \quad (2)$$

The two phases are symmetrical, such that current ripple of each phase should be identical. We can get current ripple in the first phase as Δi_1 by substituting (2) into (1):

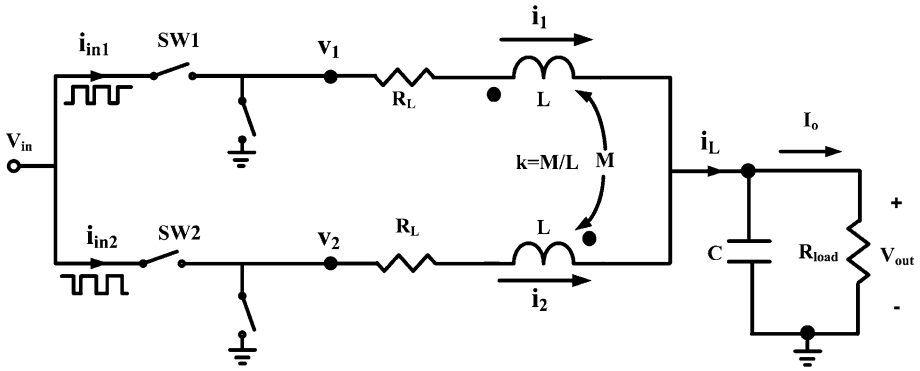


Fig. 2 Ideal two-phase interleaved topology with negative coupling between filter inductances

$$\Delta i_1 = \frac{V_{\text{in}}(1-D)(1-k)}{L(1-k^2)} \cdot (D-\frac{1}{2})T \tag{3}$$

State II: $(D - 1/2)T \le t < T/2$

$$\begin{aligned} L_1 \cdot \frac{di_1}{dt} + M \cdot \frac{di_2}{dt} &= V_{\text{in}}(1-D) \\ L_2 \cdot \frac{di_2}{dt} + M \cdot \frac{di_1}{dt} &= -V_{\text{out}} = -DV_{\text{in}} \\ \Delta i_1 &= \frac{V_{\text{in}}(1-D)(1+\frac{kD}{1-D})}{L(1-k^2)} \cdot (1-D)T \end{aligned} \tag{4}$$

State III: $T/2 \le t < DT$

$$\begin{aligned} L_1 \cdot \frac{di_1}{dt} + M \cdot \frac{di_2}{dt} &= V_{\text{in}}(1-D) \\ L_2 \cdot \frac{di_2}{dt} + M \cdot \frac{di_1}{dt} &= V_{\text{in}}(1-D) \end{aligned} \tag{5}$$

As State III is identical to state I, we can write Δi_1 during State III as:

$$\Delta i_1 = \frac{V_{\text{in}}(1-D)(1-k)}{L(1-k^2)} \cdot \left(D-\frac{1}{2}\right)T \tag{6}$$

State IV: $DT \le t < T$

$$\begin{aligned} L_1 \cdot \frac{di_1}{dt} + M \cdot \frac{di_2}{dt} &= -DV_{\text{in}} \\ L_2 \cdot \frac{di_2}{dt} + M \cdot \frac{di_1}{dt} &= V_{\text{in}}(1-D) \\ |\Delta i_1| &= \frac{V_{\text{in}}(1-D)(\frac{D}{1-D}+k)}{L(1-k^2)} \cdot (1-D)T \end{aligned} \tag{7}$$

By inspecting (3), (4), (6), and (7) and as can be seen in Fig. 3, it is clear that the largest ripple occurs at state IV. Thus, (7) can be used to represent the current ripple for $D \ge 0.5$. The same analysis can be repeated for $D < 0.5$ such that the current ripple can be derived as:

$$|\Delta i_1| = \frac{V_{\text{in}}D(\frac{1-D}{D}+k)}{L(1-k^2)} \cdot DT \quad \text{for } D<0.5 \tag{8}$$

To show the effect of coupling on the current ripple in each phase, let us define the ripple reduction factor ξ as the ratio between the coupled to uncoupled current ripples, such that:

$$\xi = \begin{cases} \dfrac{1+k(\dfrac{1}{1-D}-1)}{1-k^2} & \text{if } D<0.5 \\ \dfrac{1+k(\dfrac{1}{D}-1)}{1-k^2} & \text{if } D \ge 0.5 \end{cases} \tag{9}$$

Figure 4 shows the ripple reduction factor ξ versus the duty cycle for different coupling factors. As can be seen from the figure, within the duty cycle range of 0.3–0.7, the current ripple is reduced in the coupled case compared to uncoupled case. It is also clear that there is an optimum coupling factor for maximum ripple cancellation at each duty cycle, which can be derived as:

$$k_{\text{opt}} = \begin{cases} \frac{1-D}{D}\left(\sqrt{1-\left(\frac{D}{1-D}\right)^2}-1\right) & \text{if } D<0.5 \\ \frac{D}{1-D}\left(\sqrt{1-\left(\frac{1-D}{D}\right)^2}-1\right) & \text{if } D \ge 0.5 \end{cases} \tag{10}$$

Figure 5 shows the lowest achievable current ripple in each phase for different duty cycles, where the maximum reduction of 50% in current ripple occurs at $D = 0.5$ for $k = -1$. This improvement drops to 13% within 20% variation in duty cycle. The sensitivity of ripple reduction to the coupling factor is shown in Fig. 6. For duty cycles other than 0.5, as the absolute value of the coupling factor increases beyond 0.4, the current ripple increases dramatically.

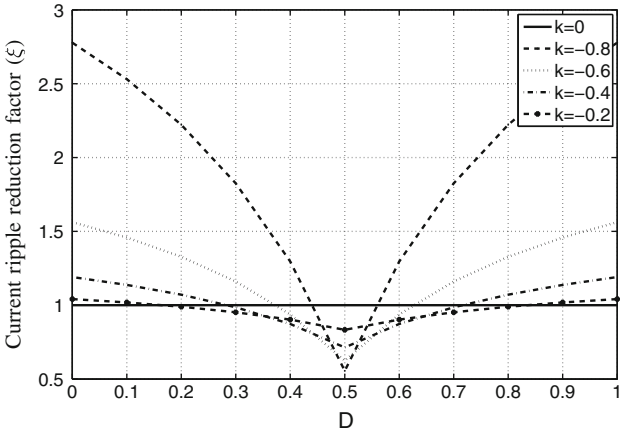


Fig. 4 Current Ripple reduction as a function of duty cycle for different coupling factor

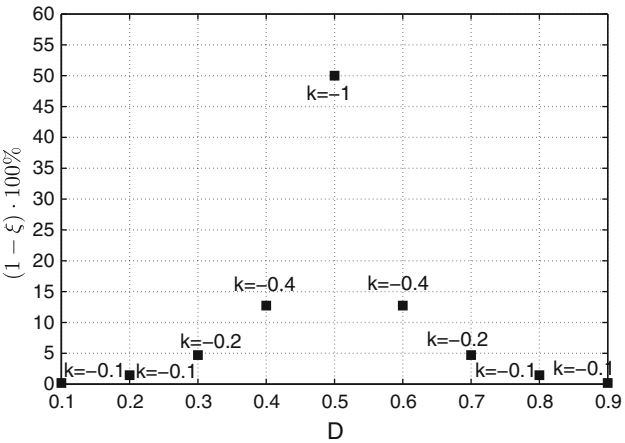


Fig. 5 Ripple reduction percentage for two phase interleaved converter as function of duty factor with optimum k listed

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{dv_{\text{out}}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-LR_L}{L^2-M^2} & \frac{MR_L}{L^2-M^2} & \frac{-1}{L+M} \\ \frac{MR_L}{L^2-M^2} & \frac{-LR_L}{L^2-M^2} & \frac{-1}{L+M} \\ \frac{1}{C} & \frac{1}{C} & \frac{-1}{CR_{\text{load}}} \end{bmatrix} \times \begin{bmatrix} i_1(t) \\ i_2(t) \\ v_{\text{out}}(t) \end{bmatrix} + \begin{bmatrix} \frac{D}{L+M} \\ \frac{D}{L+M} \\ 0 \end{bmatrix} \times V_{\text{in}} + \begin{bmatrix} \frac{V_{\text{in}}}{L+M} \\ \frac{V_{\text{in}}}{L+M} \\ 0 \end{bmatrix} \times d(t) \tag{11}$$

$$\begin{bmatrix} i_{\text{in1}}(t) \\ i_{\text{in2}}(t) \end{bmatrix} = \begin{bmatrix} D & 0 \\ 0 & D \end{bmatrix} \times \begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix} + \begin{bmatrix} \frac{I_o}{2} & 0 \\ 0 & \frac{I_o}{2} \end{bmatrix} \times d(t) \tag{12}$$

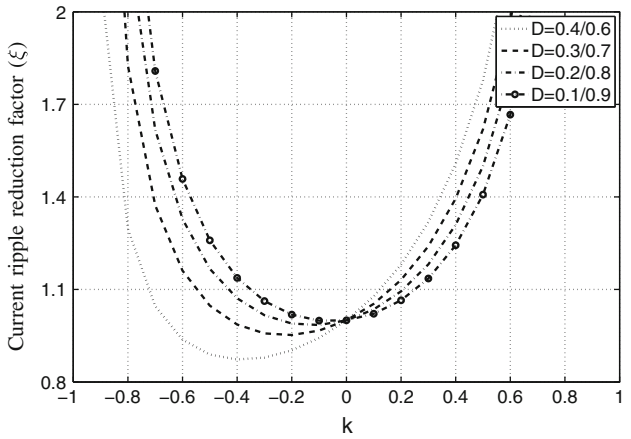


Fig. 6 Sensitivity of current ripple reduction to the variation in coupling factor for different duty ratios

2.2 System stability and transient response

To study the effect of coupling on the transient response of the DC–DC converter, let us define $d(s)$ as the small signal function of the duty ratio D. The open loop transfer function $v_o(s)/d(s)$ can be derived following the space state analysis described in [23]. The average space state equation is given in (11) and (12), where i_{in1} and i_{in2} are the input currents to the two phase converter and R_L is the dc resistance of the inductor, which is approximated as $8 \times L$ mΩ/nH. The transfer function of $v_o(s)/d(s)$ is derived as in (13) and plotted in Fig. 7 for different coupling factors. The figure compares the bandwidth and phase margin between non-coupled ($k = 0$), positively coupled ($k = 0.4$) and negatively coupled ($k = -0.4$) two phase interleaved dc–dc converters. The input voltage is selected as 4.5 V, L = 8 nH, $R_{\text{load}} = 3.3$ ohm, and the load capacitor $C = 20$ nF. As can be seen from the figure, for negative coupling factor of 0.4, the converter bandwidth increases by 29.2% compared to the non-coupled two

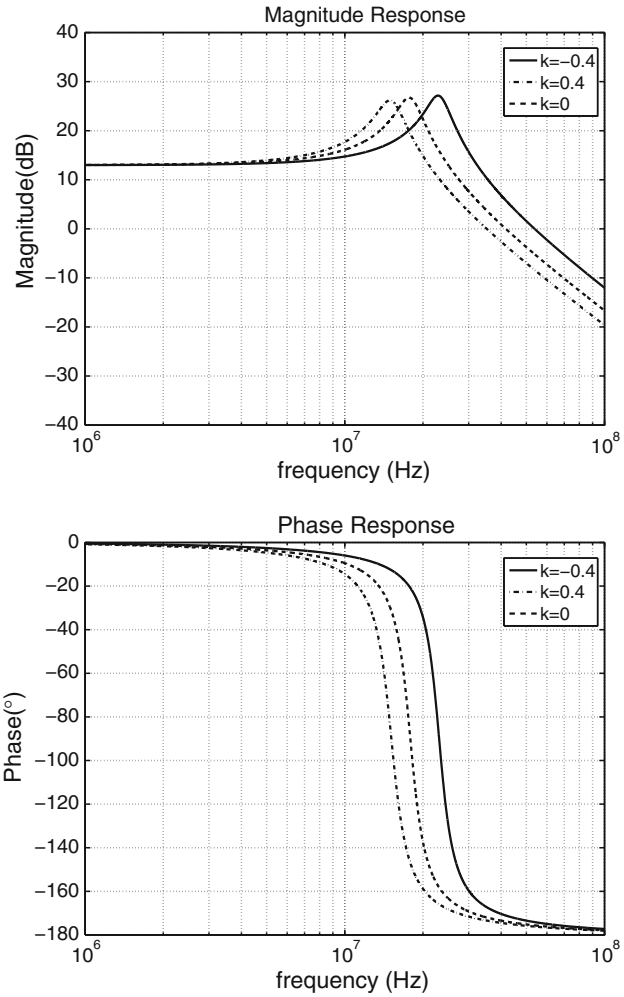


Fig. 7 Open loop transfer function versus coupling factor

phase converter, and 52.7% compared to positively coupled converter with the same coupling factor. Figure 8 shows the improvement in bandwidth as function of the coupling factor, where a strong indirect (negative) coupling translates to wider bandwidth.

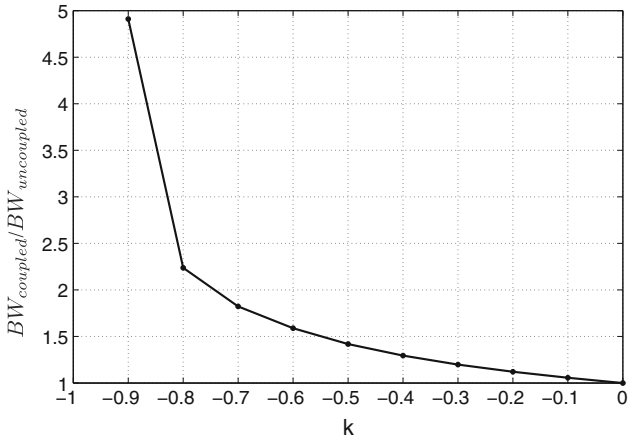


Fig. 8 Bandwidth improvement versus coupling factor

$$\frac{v_{\text{out}}(s)}{d(s)} = \frac{\frac{2V_{\text{in}}}{C(L+M)}\left(s + \frac{R_L}{L-M}\right)}{s^3 + K1 \cdot s^2 + K2 \cdot s + K3}$$
$$K1 = \frac{1}{R_{\text{load}}C} + \frac{2LR_L}{L^2 - M^2}$$
$$K2 = \frac{2LR_L}{R_{\text{load}}C(L^2 - M^2)} + \frac{R_L^2}{L^2 - M^2} + \frac{2}{C(L+M)} \quad (13)$$
$$K3 = \frac{R_L^2}{R_{\text{load}}C(L^2 - M^2)} + \frac{2R_L}{C(L^2 - M^2)}$$

The DC–DC converter's transient behavior can also be explained using the equivalent inductor as follows. The transient response is measured by the time it takes the converter to stabilize when the input voltage or the duty cycle changes. The stabilization time is a function of the output filter network formed of the inductance and capacitance as well as their parasitic resistances. For faster transient response, the value of inductor should be small enough to allow a fast slew rate and prevent excessive voltage changes on the capacitor. The equivalent inductor for transient response is given by $L_{\text{eq\_trans}} = L(1-k)$ [22], which implies that higher coupling coefficients result in reduced rise and fall times. Hence, from the discussion above, negative coupling can be beneficial for both the steady state and transient responses, by reducing the current ripple and increasing the bandwidth of the DC–DC converter system. However, the improvement in the current ripple is very sensitive to duty cycle and at each duty cycle, there is an optimum coupling factor. Since bandwidth improvement is less for smaller k, the selection of coupling factor should mostly be based on the duty cycle of the system. In this design, the coupling factor is selected at -0.3 for optimum performance at the desired duty ratio of 0.7. For practical limitations, the coupling factor has to be fixed, however, the selected coupling factor of -0.3, can still achieve current ripple reduction over duty ratios from 0.25 to 0.75 as shown in Fig. 4.

3 Technology considerations

This section addresses the technology aspect of high switching speed power converters. A few of the desirable characteristics of the power transistor technology for high frequency switching regulators are the following. A low ON resistance (R_{ON}) is necessary to minimize conduction losses as the transistor conducts. A low gate charge (Q_G) is necessary to minimize power losses in the driver circuits, as well as to reduce the switching time, thereby reducing $V_{\text{DS}} \times I_D$ loss during the switching transition. In addition, the transistor has to have a high breakdown voltage since parasitic drain inductances can cause voltage spikes higher than the rail voltage, that would appear at the drain terminal during sharp current transitions. P-HEMTs have a higher channel electron mobility and a lower gate capacitance and therefore a lower $R_{\text{ON}} \times Q_G$ product compared to silicon NMOSFETs in the same voltage range making them suitable candidates for high frequency power switching applications [24].

The transistor chosen for the switching device is an enhancement mode pseudomorphic HEMT device fabricated on GaAs substrate. The structure and the epilayers of

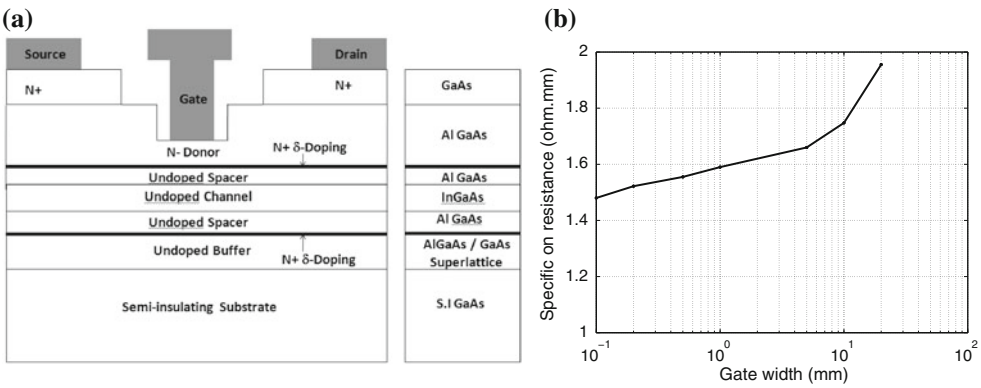


Fig. 9 GaAs p-HEMT device: **a** structure and epilayers, **b** ON resistance characterization [24]

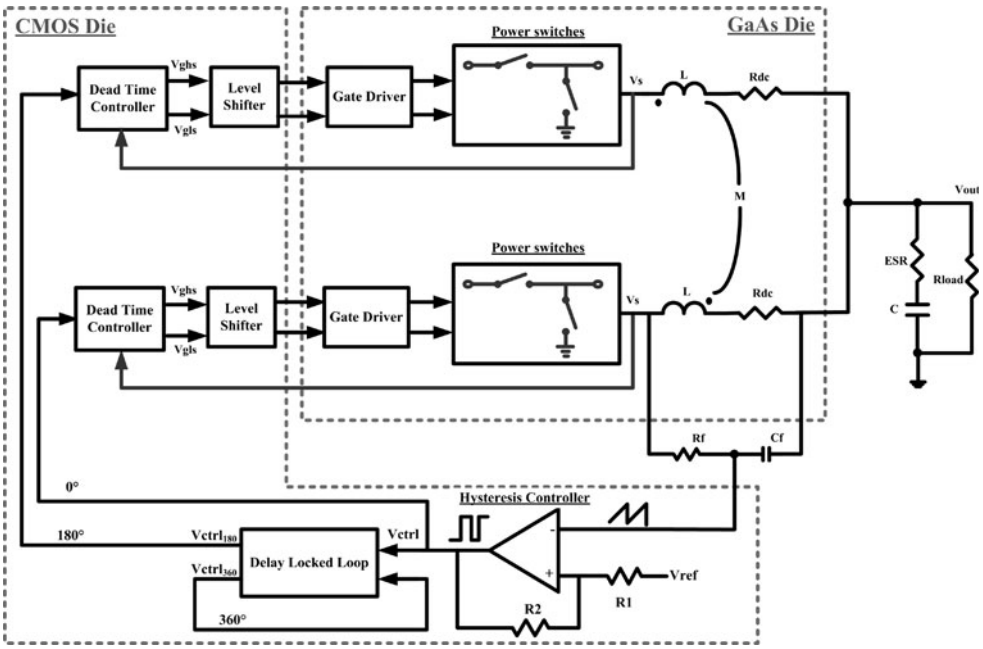


Fig. 10 Two phase hysteretic controlled buck converter block diagram

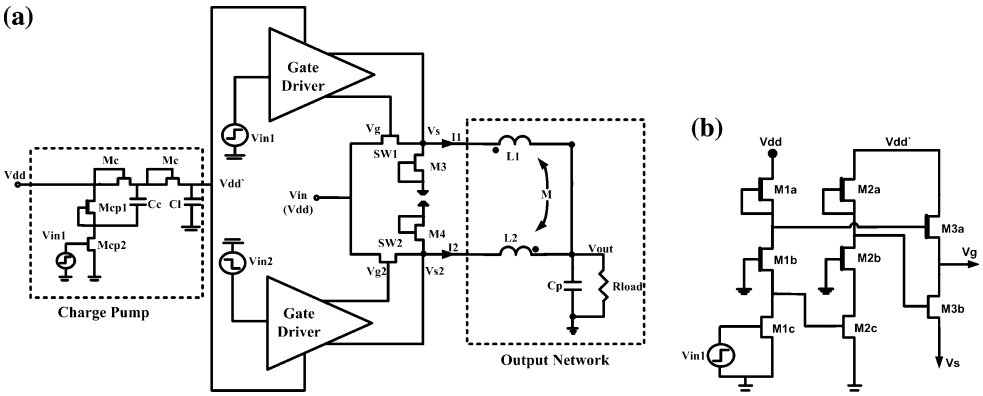


Fig. 11 Schematic of DC–DC converter, **a** power stage, and **b** gate driver stage

the device technology are shown in Fig. 9a. The transistor has a floating substrate and therefore the source terminal of the N-type transistor can be raised above the ground potential without causing body depletion in a high side switch. The threshold voltage of the device is 0.36 V. The breakdown voltage of the transistor is 11 V at 300 K and the drain to source leakage current is of the order of ~ 1 μA/mm. The ON resistance of E-p-HEMT is shown in Fig. 9b. For a 10-mm E-p-HEMT device, the on resistance is 1.75 ohm.

4 Circuit implementation

To show the capabilities of GaAs power devices in a high frequency power switching environment and demonstrate the effect of negatively coupled inductors in interleaving architectures, a prototype using 0.5 μm GaAs p-HEMT process is designed and fabricated. The two stage interleaved DC–DC converter is designed for 4.5–3.3 V, 1 A load current conversion with 150 MHz switching frequency. The coupled inductors are implemented on a separate GaAs die with 65 μm thick top copper layer. Given the lack of complementary devices in the used GaAs p-HEMT process, the closed loop power control circuitry that includes a hysteresis comparator, delay-locked loop and adaptive dead-time controller, is designed in 0.25 μm BiCMOS technology using 3.3 V thick oxide transistors. The block diagram of the two-chip solution, closed loop interleaved DC–DC converter system is shown in Fig. 10, while the schematics of the output and driver stages are shown in Fig. 11.

4.1 GaAs two phase interleaved DC–DC converter with coupled inductors

The output stage of the switch mode DC–DC converter, is implemented as conventional buck converter with reversed diodes M_3 and M_4 as low side switches and SW1 and SW2 as high side switches. Two loss mechanisms are encountered in the switching stage; (1) the switching losses during the transition between on and off states, which increase

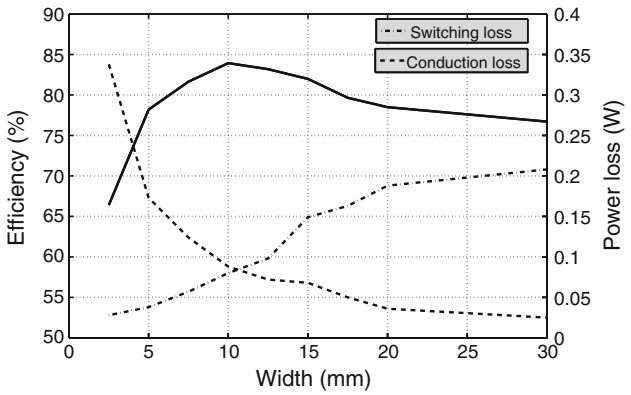


Fig. 12 Variation of MOSFET switching and conduction losses and the corresponding output stage efficiency as a function of device width

with increasing the transistors' sizes, and (2) conduction losses due to the finite on-resistance of the switching devices which decreases with increasing the transistors' sizes. Figure 12 shows the variation in both losses as a function of the switching transistor width for 4.5–3.3 V conversion ratio. The optimum device widths are obtained by equating the conduction and switching losses of the switches to minimize their total power loss.

It is important to consider the gate driver losses when sizing the switching transistors. This is mainly due to the fact that the switching losses increase as the gate driver stage fails to provide enough driving power. For a 1 A output current and 4.5/3.3 V voltage conversion ratio, the widths of SW1 and SW2 are chosen as 10 mm from Fig. 12. They are implemented as 20 unit transistors in parallel, each with 500 μm width. This is mainly to satisfy a given aspect ratio for the converter die. The reverse connected diodes are realized by connecting the gate and source of the HEMT devices together. Transistors M3 and M4 have to provide a path for the current when SW1 and SW2 are off. In this design, they are sized at the same width of SW1 and SW2.

Due to the lack of complementary transistors in the used GaAs p-HEMT process, the supply voltage for the gate driver has to be higher than the supply voltage of the output stage of the converter in order to drive the high side switches. The minimum value for the gate driver supply is $V_{dd} + V_p$, where V_p is the pinch off voltage of the enhancement mode p-HEMT. A single stage Dickson charge pump is adopted to generate $V_{dd} + V_p$ as the supply voltage of gate driver circuit as shown in Fig. 11a.

The gate driver stage, shown in Fig. 11b, is a two-stage active inverter with the second stage referenced to the source of the high side switches. This inverter stage is designed as pseudo-complementary switches with high side depletion mode HEMT and low side enhancement mode HEMT. The gate driver generates complementary control signals for M_{3a} and M_{3b}. Since the depletion mode HEMT has a negative pinch off voltage, the supply voltage for the first driver stage can be lowered to V_{dd} to reduce the power consumption. The second and third stages have a supply of $V_{dd} + V_p$, so that the output of second driver stage can swing between 0 and $V_{dd} + V_p$, and turn on switch SW1.

The sizing of the gate driver stages is a tradeoff between the gate driver loss and its capability to drive the high side switches, which affects the switching loss of SW1 and SW2. The larger sizes of M_{3a} and M_{3b} provide better driving capability while decreasing the rise and fall times, which will accordingly reduce the switching loss of the main transistors. However, larger sizes of M_{3a} and M_{3b} will also increase the power consumption in the gate driver. The width of enhancement mode p-HEMT M_{3b} is chosen as 1/10 of the high side switch SW1. M_{3a} is sized as 1/3 of M_{3b}. The first two stages are equally sized. Transistors M_{1c} and M_{2c} are selected as 1/4 of M_{3b} as well as M_{1b} and M_{2b}, since they are pull down transistors. Considering the same turn on and turn off time, pull up transistors M_{1a} and M_{2a} are sized as 1/10 of M_{1c} and M_{2c}.

4.2 Coupled inductors design

While operating at high switching frequency facilitates the monolithic integration of inductors, satisfying the requirements for low dc resistance and high current handling capability makes the inductor design quite challenging. Since the total current delivered to the load passes through the filter inductors, the size of the inductors must be properly selected to achieve an optimal balance between the required inductance value for a given current ripple and their respective series resistance that affects the converter efficiency. Thus, the inductance value can be determined based on either the required current ripple or to minimize the losses in the inductance. To find the minimum acceptable inductor value for a give current ripple, the maximum current ripple is defined at the boundary of Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) [25], such that

$$|\Delta i_1| = I_o \tag{14}$$

where I_o is the current in the load resistance. Using (7) and (14), the inductor required for minimum current ripple can be defined as:

$$L_{\min} = \frac{V_{\text{in}}(1-D)(\frac{D}{1-D}+k)(1-D)}{(1-k^2)f_{\text{sw}}I_o} \tag{15}$$

Thus, for $V_{\text{in}} = 4.5$ V, $I_o = 1$ A, $f_{\text{sw}} = 150$ MHz, and $D = 0.65$, the optimum coupling factor is -0.3 according to (10), which corresponds to a minimum inductor value of 6.28 nH.

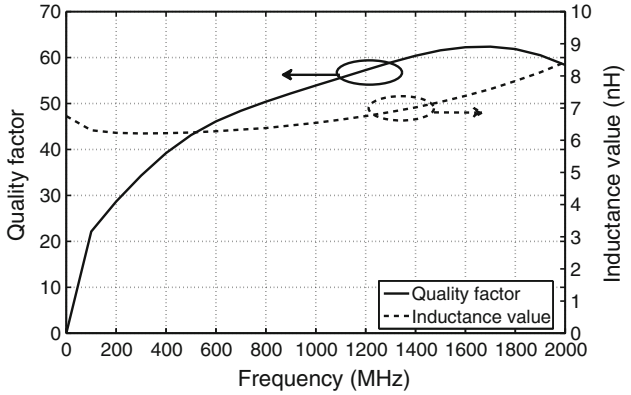


Fig. 13 Coupled inductor characterization results from electromagnetic simulations using MOMENTUM

Alternatively, the inductor value can be found from the inductor power loss, which can be written as (16) by adding the average current to the current ripple, and using R_{ind} as the resistance of the inductor, where $R_{\text{ind}} = R_L + \frac{2\pi f_{\text{sw}} L}{Q}$. From the axiom that $a^2 + b^2 \geq 2ab$, the inductor value for a minimum inductor loss P_{indloss} can be given by

$$P_{\text{indloss}} = \left(\frac{I_o^2}{2} + \frac{2}{3}\left(\frac{V_{\text{in}}(D + (1-D)k)}{2L(1-k^2)}(1-D)T\right)^2\right)R_{\text{ind}} \geq \frac{V_{\text{in}} I_o (1-D)^2 (\frac{D}{1-D} + k)}{\sqrt{3}(1-k^2) f_{\text{sw}} L} \cdot R_{\text{ind}} \tag{16}$$

$$L_{\text{min}} = \frac{V_{\text{in}}(1-D)^2(\frac{D}{1-D} + k)}{\sqrt{3}(1-k^2) f_{\text{sw}} I_o} \tag{17}$$

For the given circuit specification, $L_{\text{min}} = 3.63$ nH according to (17). However, to make sure the converter operating at CCM, the inductance value of 6.28 nH is selected.

The coupled inductors are designed in 65 μm copper layer with interleaved square topology. The spacing between windings are determined based on the selected coupling factor of −0.3. ASITIC [26] is used to estimate the number of turns and metal width for the desired inductance and resistance values. Electromagnetic EM simulations using MOMENTUM are performed to verify the inductance value and characterize the variation of Q versus frequency. Figure 13 shows the EM simulation results of inductance and quality factor. For $L = 6.3$ nH, a quality factor of 25 at 150 MHz and a dc resistance = 55 mΩ are simulated, while assuming flip chip packaging. The EM simulated coupling factor between two inductors is −0.34, which is close to the desired value from circuit and system level simulations. The power loss of the designed inductor is only 2.4% of the total power loss in the converter. In [15], a 2 nH spiral inductor in 130 nm CMOS technology contributed 11.5% of the total power loss at a switching speed of 170 MHz. Similarly, in [18], an 11 nH inductor in 0.18 μm RF BiCMOS process with an extra 10 μm thick copper layer provided 75% power loss contribution in single phase buck converter.

4.3 Closed loop based on hysteretic controller

Given the high switching speed of the converter, a hysteresis controller with delay-locked loop circuit for two phase converter operation is adopted for this prototype due to its simplicity and fast transient response. Hysteretic controller is a self oscillation circuit that regulates the output voltage by keeping it within a hysteresis window set by a reference voltage regulator and comparator. The switching frequency of hysteresis controller is given by [27]:

$$f_s = \frac{D(1-D)}{\tau_{RC}(V_H/V_s) + \tau_D} \tag{18}$$

where D is the duty ratio, τ_{RC} equals to $R_F C_F$, and τ_D is the propagation delay. R_F and C_F are selected to ensure that the hysteresis controller operates at 150 MHz under peak power. It also implies that the maximum switching frequency occurs at $D = 0.5$.

The schematic of the voltage differential comparator is shown in Fig. 14. Current mirrors are used to bias the differential input stage and the output stage. Two-stage inverters are used at the output to provide enough driving capability for the following stage. The bandwidth of designed comparator is 250 MHz to respond to the signal at the desired switching frequency. The delay from input to output is about 0.2 ns. The power loss for the hysteresis comparator is 2.34 mW, only 0.035% of the output power of DC–DC converter.

For two phase DC–DC converter system, the control signals for the two phases should be exactly 180° out of phase. A self-biased delay-locked loop [28, 29] is adopted to produce exactly the required phase delay which consists of phase detector, charge pump, low pass filter, bias generator and voltage controlled delay cell as shown in Fig. 15. The phase detector, which consists of two set and reset D flip-flops and a NAND gate, is shown in Fig. 16 determines the phase lead or lag between the feedback signal and the reference clock. The output of phase detector is fed into a charge pump to generate the control voltage V_{cp}. Since any small offset in charge pump circuit will affect the output control voltage for VCDL, a differential zero-offset charge pump with symmetric-load is used as shown in Fig. 17.

For a robust design with low jitter, self biasing is adopted. The bias generator, shown in Fig. 18, generates the control voltage for voltage controlled delay line based

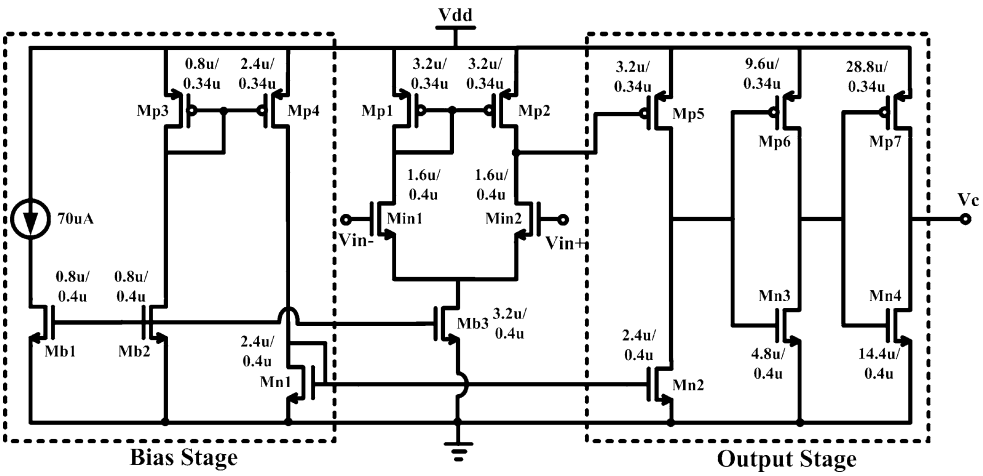


Fig. 14 Schematic of hysteresis comparator

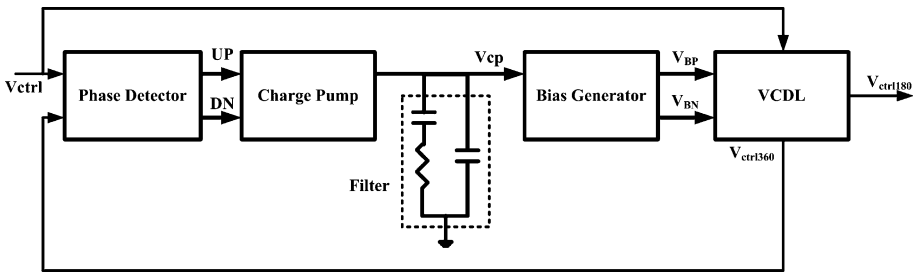


Fig. 15 Block diagram of Delay-locked-loop

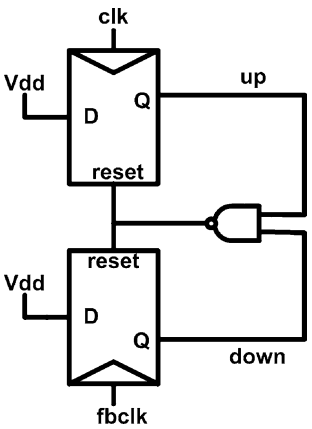


Fig. 16 Phase detector block diagram

upon V_{cp}. The advantage of using bias generator is to avoid any disturbances and noises affecting V_{cp}. The voltage controlled delay line is composed of a series of delay cells which produce the required phase delays as shown in Fig. 19. The whole system will be locked once the feedback clock $V_{ctrl360}$ is aligned with the reference V_{ctrl}. The 180° delay signal $V_{ctrl180}$ is used to drive the other phase. A specific delay is obtained by adjusting the ON-resistance of M_{n1} and the load current.

To increase the converter efficiency at light load, synchronous buck converter topology with adaptive deadtime control is used rather than the asynchronous structure shown in Fig. 11. The adaptive deadtime controller senses the source of the high side switch V_s, and compares it with the pulse width modulated PWM control signal V_{ctrl}, as shown in Fig. 11. The details of the deadtime controller is given in Fig. 20. As V_{ctrl} changes from HI to LO, V_{ghs} will turn LO immediately. When V_s reaches zero, V_{gls} goes from LO to HI, turning on the low side switch. Similarly, for V_{ctrl} = HI, the low side switch is turned off as V_{gls} = LO, which will automatically turn on the high side switch.

The efficiency comparisons among conventional buck converter, synchronous buck converter with fixed deadtime and synchronous buck converter with adaptive deadtime controller is given in Fig. 21. The efficiency variation using conventional gate driver is about 45% from peak output power of 3.3 W to low output power of 0.5 W and 15% for synchronous rectifier topology. The adaptive deadtime controller achieves almost the same efficiency as fixed dead-time controller at high output power, and is about 2% higher at low output power.

A level shifter circuit is inserted between the GaAs and CMOS dies as shown in Fig. 10. The output of the CMOS circuits in the used technology swings from 0 to 3.3 V, while the GaAs gate driver input requires gate-source voltage lower than 0.85 V [24]. If the voltage supplied to the gate of the GaAs P-HEMT goes beyond

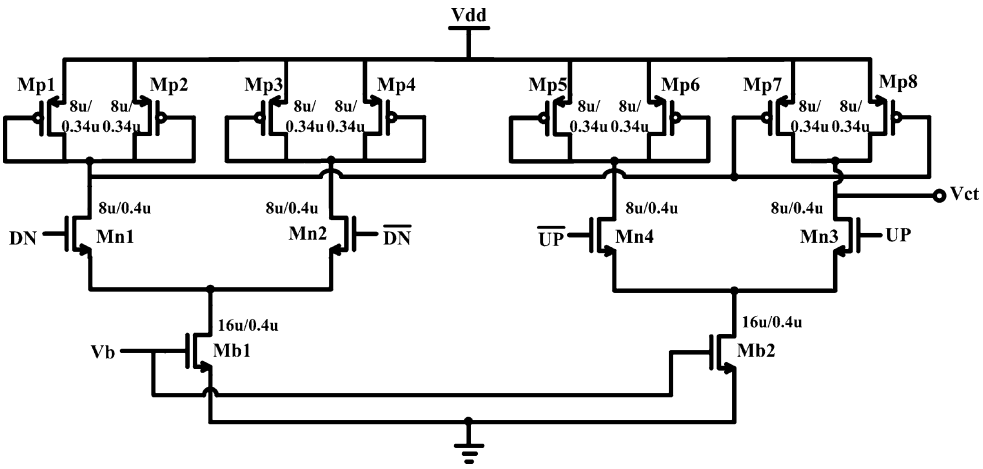


Fig. 17 Schematic of zero-offset charge pump [29]

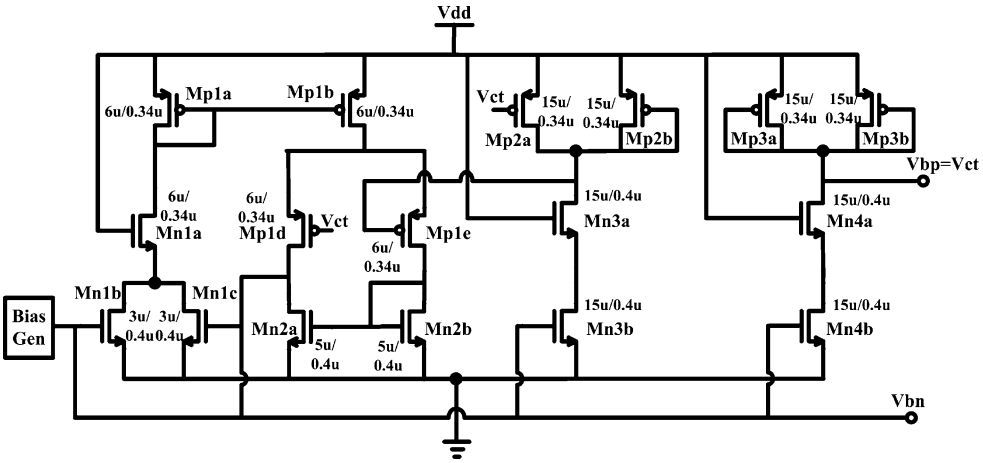


Fig. 18 Bias generator circuit in DLL [29]

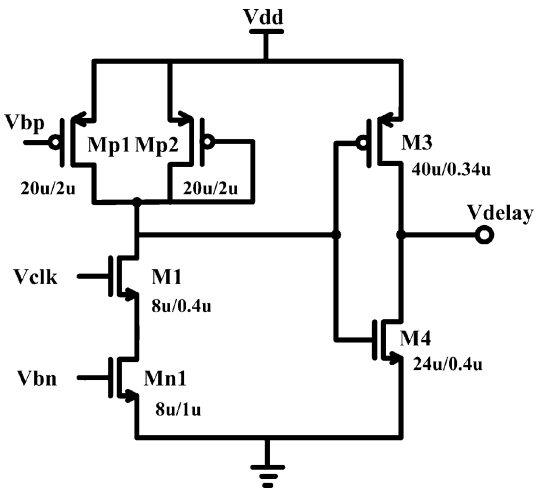


Fig. 19 Schematic of voltage controlled delay cell

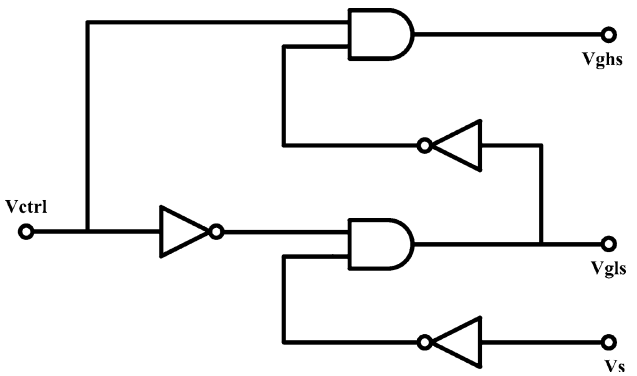


Fig. 20 Block diagram of adaptive deadtime controller

0.85V, the gate Schottky diode will be heavily forward biased and will draw large current from the supply, increasing the overall power consumption. The design of the level shifter to shift down the signal level at the interface between the two dies follows the design procedure proposed in [30].

4.4 Power loss analysis

The major power loss components in a DC–DC converter can be divided as; (1) series resistance losses from the

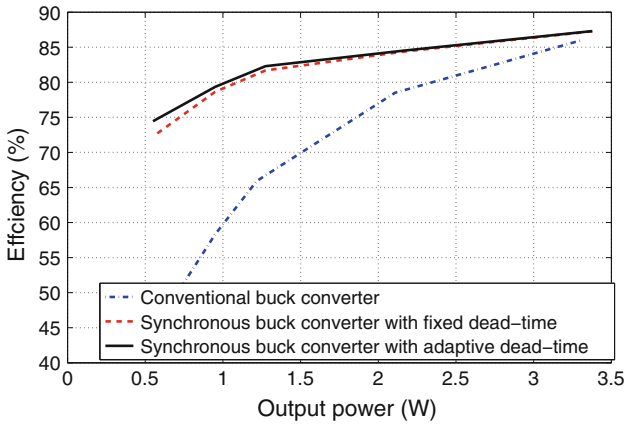


Fig. 21 Simulated power efficiency of single phase synchronous buck converter with fixed dead-time and conventional buck converter at 4.5 V input and 150 MHz switching frequency

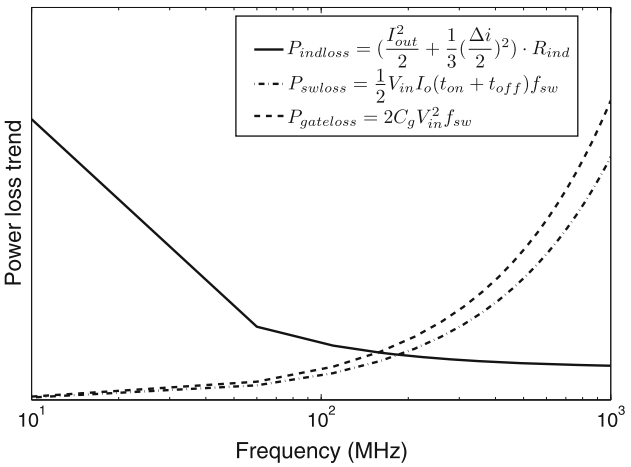


Fig. 22 Power loss trend with increasing switching frequency

inductors P_{indloss}, (2) the conduction loss of the high side switches P_{onloss}, (3) the switching losses of SW1 and SW2 P_{swloss}, which depend on the turn-on and off time periods and the switching frequency, (4) the conduction loss of the diode connected transistors M3 and M4 during $(1 - D)T$ period $P_{\text{diodeloss}}$, and (5) the gate driver loss P_{gateloss} which depends on the parasitic gate capacitances as well as the switching frequency.

Operating at high switching frequency reduces the inductor size, and its equivalent DC resistance. However, this comes at the expense of increasing the switching losses and gate driver losses. Figure 22 shows the drop of inductance loss over switching frequency, the trends of switching loss and gate driver loss. Conduction losses of both high side switches and diode do not change with frequency.

The distribution of power losses for the DC–DC converter, shown in Fig. 23, is based on simulations results. The conduction loss is almost the same as the switching

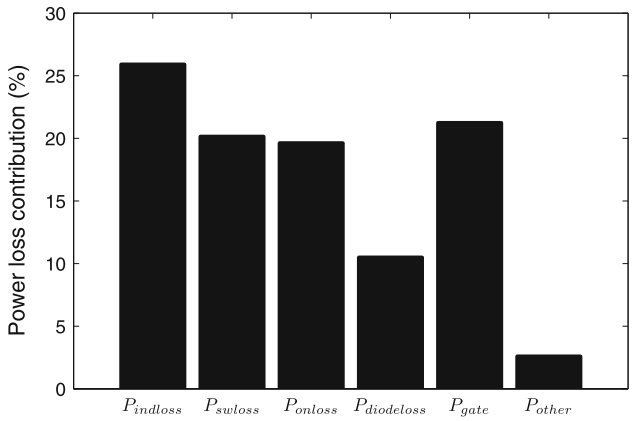


Fig. 23 Power loss contribution of various elements in the two phase interleaved converter with negative coupled inductors at 4.5/3.3 V, 1 A output and 150 MHz switching frequency

loss which contribute about 20% of the overall power losses. Since the duty cycle is 0.65, the diode loss is only half of the conduction loss. At 150 MHz, inductor loss is still the dominant loss component, while the overall power efficiency is 84.5%.

The lack of complementary devices in the used technology contributed to the increase in gate driver losses. For the duty cycle of 0.65, the diode loss is almost 10% of the overall losses. The contribution of the diode loss is expected to increase for lower power level. Using synchronous rectifiers with dead-time control circuit will maintain the efficiency over a wide output power range. The contribution of the closed loop control circuitry to the overall power consumption is less than 1%, given the digital nature of the circuits involved and the use of CMOS technology.

5 Characterization results of hysteretic controlled DC–DC converter

The complete DC–DC converter system is composed of the power converter stages with coupled inductors implemented in GaAs 0.5 μm p-HEMT technology and hysteresis controller with delay locked loop and adaptive dead-time controller designed in 0.25 μm BiCMOS technology. Section 5.1. A presents the measurement results of the two phase interleaved GaAs converter, while the closed loop simulation results are given in Section 5.2.

5.1 Two phase interleaved DC–DC converter performance

The circuit shown in Fig. 11 is designed for 150 MHz switching frequency with 8.77 nH coupled inductors and

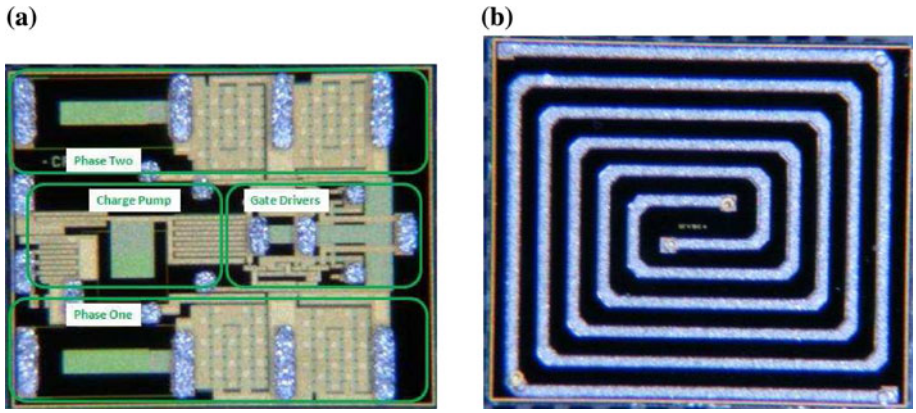


Fig. 24 **a** DC–DC converter and **b** coupled inductors die photos

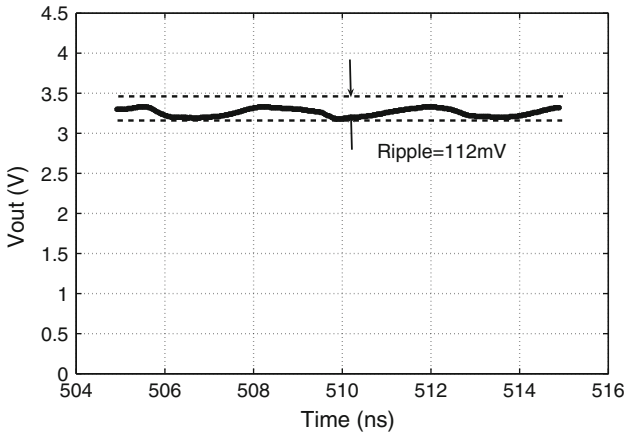


Fig. 25 Output voltage transient response

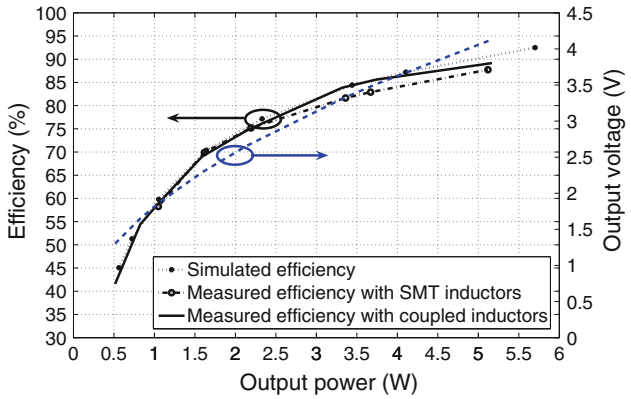


Fig. 27 Efficiency comparisons for different output power at 150 MHz, 4.5 V input and 1 A load current

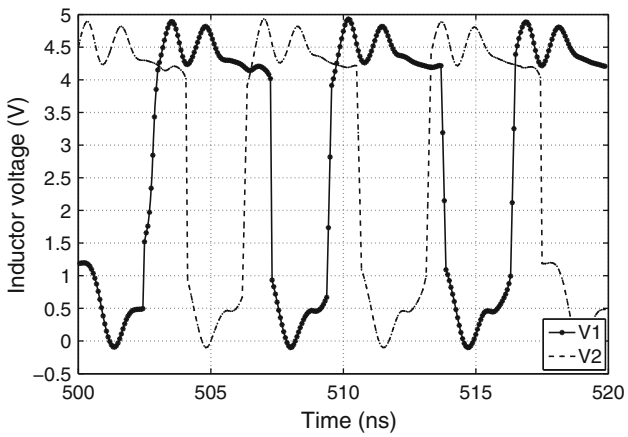


Fig. 26 Two-phase operation of DC–DC converter

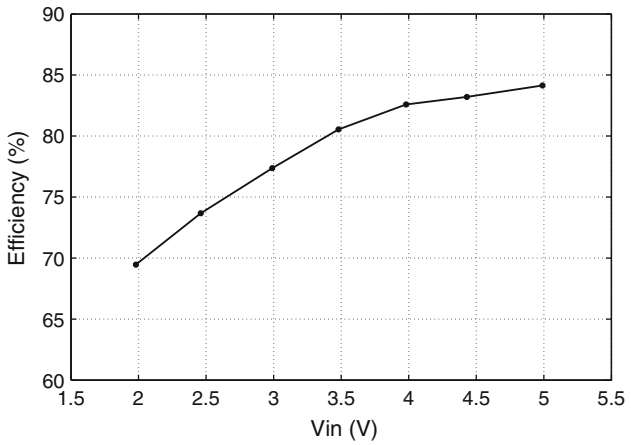


Fig. 28 Efficiency versus input voltage for 150 MHz, 3.3 V/1 A output

20 nF load capacitor. The circuit converts 4.5 V input to 3.3 V output with 1 A output current. The die micrograph is shown in Fig. 24. The area of the converter is 2×2.1 mm^2 and 2.3×2.7 mm^2 for the coupled inductors. Both dies use C4 bump for flip chip packaging, which eliminate the parasitic inductances and resistances introduced by bondwires. The circuit test board is a four-layer PC board with copper plus OSP. An input decoupling capacitor of 22 µF is mounted close to the input supply voltage to avoid any oscillations.

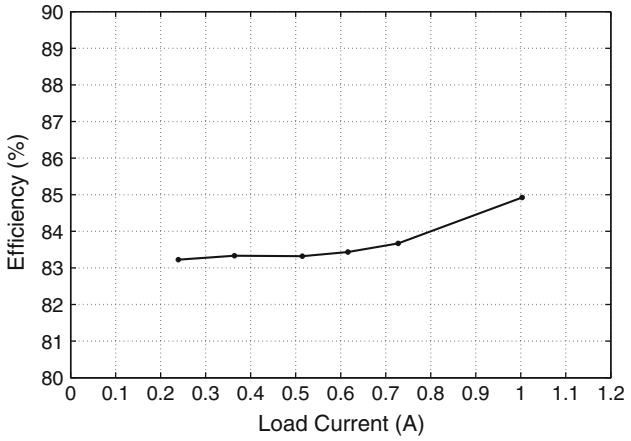


Fig. 29 Efficiency versus load current at 150 MHz, 4.5 V/3.3 V conversion

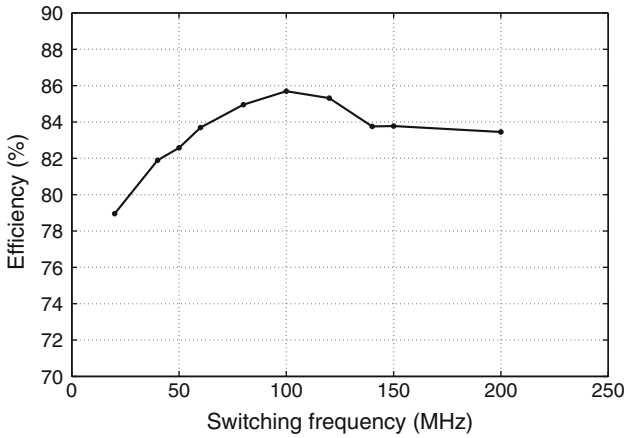


Fig. 30 Efficiency versus switching frequency at 4.5/3.3 V conversion and 1 A load current

The two stage interleaved DC–DC converter is tested using an external pulse input provided by Agilent B1110A generator with the output measured using HP Infinium 1.5 GHz Oscilloscope. Figure 25 shows the signal at the output node with a measured output ripple of 116 mV. This is slightly higher than the simulated output ripple of 72 mA due to the deviation in the coupling factor of the implemented inductors from the optimum value, for maximum ripple cancellation. The implemented inductors have a effective coupling factor of 0.46 compared the optimum value of 0.3 from the analysis in Section 2. This is mainly due to the fact that the coupled inductors are flip mounted on the four layer PCB, which increases the distance between copper layer and ground. Figure 26 gives the two-phase operation waveform with the internal access at the input of coupled inductors, showing a 180° phase delay between two phases.

The efficiency using integrated coupled inductors as well as external uncoupled surface-mount inductance are compared to simulation results in Fig. 27. The measured

Table 1 Measured performance summary

Technology	0.5 μm GaAs p-HEMT
Circuit area	4.22 mm^2
Inductor area	5.94 mm^2
Inductance value	8.77 nH
Coupling factor	0.46
Q at 150 MHz	26
Input voltage	4.5 V
Output voltage	3.3 V
Output current	1 A
Switching frequency	150 MHz
Peak efficiency	84%
Voltage ripple	116 mV

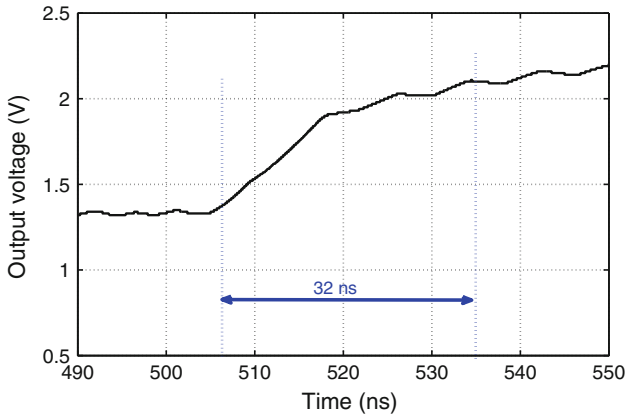


Fig. 31 Output response to changes in reference at 500 ns

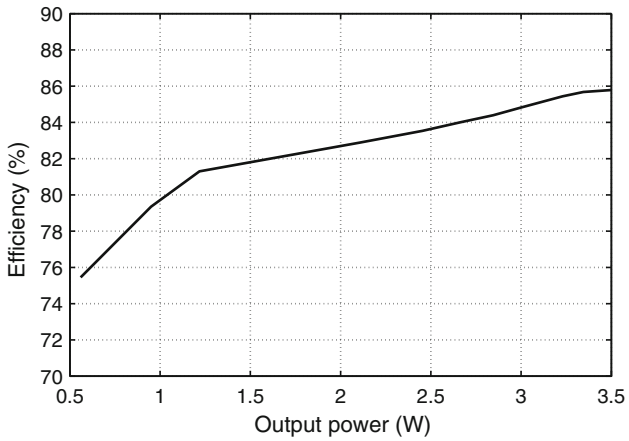


Fig. 32 Closed loop efficiency versus output power

efficiency using integrated coupled inductors at the target conversion ratio of 4.5/3.3 V is 83.8%. As the duty ratio changes from 0.2 to 0.8, the efficiency drops about 30%.

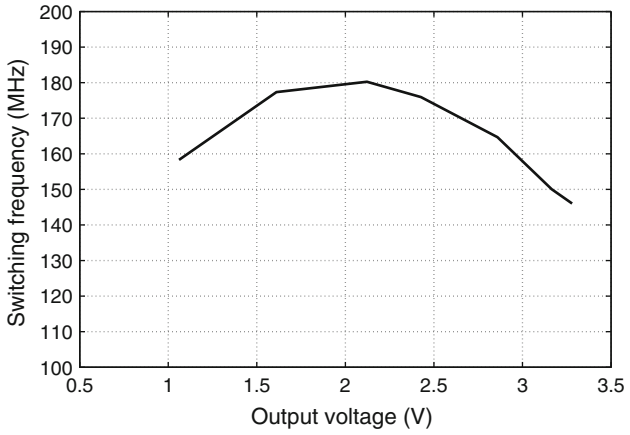


Fig. 33 Switching frequency at different output voltage

For the measurements using external uncoupled inductors, 7.5 nH 0603 SMT inductors by Coilcraft [31] with a quality factor of 28 at 150 MHz and dc resistance of 0.059 ohm, are used. The simulation results are based on circuit models provided by the manufacturer and the extracted lumped element parameters from EM simulations of the coupled inductors. The measurement result using non-coupled SMT inductor is about 1.5% less efficient than coupled inductors at the target conversion ratio.

The output efficiency at different input voltages is plotted in Fig. 28 at a constant load and duty ratio. Figure 29 shows the efficiency at different load resistors with constant input of 4.5 V and a duty ratio of 0.65. The relation between efficiency and switching frequency is shown in Fig. 30. The measurement results show that the optimum point is at around 120 MHz which is about 20% offset from the designed frequency. Table 1 summarizes the measurement results of the proposed two phase interleaved dc–dc converter with negative coupled inductors in 0.5 μm GaAs p-HEMT technology.

5.2 Closed loop system performance

The closed loop power control, shown in Fig. 10, is designed in 0.25 μm BiCMOS technology, using 3.3 V thick oxide transistors. The input is 4.5 V for power stage and 3.3 V for CMOS stage, with peak output current of 1 A. The output load capacitor is 20 nF and the load resistor is 3.3 ohm. The inductor ripple sensing network, R_F and C_F are selected as 4 Kohm and 5 pF for switching frequency equals to 150 MHz at peak output power.

Transient response performance is simulated for a step change in reference voltage at 500 ns. The rise time of the step function is 5 ns. It takes the output 32 ns to stabilize as depicted in Fig. 31. The closed loop efficiency at different outputs is shown in Fig. 32. The peak efficiency at 3.3 W is 85.68%, and control loop power consumption is 71 mW, which is less than 1% of the overall power. Compared to the asynchronous buck converter topology characterized in the previous section, which showed 30% efficiency variation as the power changes from 1 to 3.3 W, the simulation results of the closed loop control uses a synchronous converter topology which improves the overall efficiency variation to about 11%.

Hysteresis controller has the inherent problem of switching frequency variation with duty ratio. Figure 33 provides the switching frequency at different output voltage. At 3.3 W, the switching frequency is 150 MHz. It reaches the peak frequency of 180 MHz at $V_{out} = 2.2$ V, which is about $D = 0.5$, where the frequency variation is 20%. To maintain a constant switching frequency, another frequency control block should be inserted after the hysteresis comparator to compare and adjust the signal frequency of the output of the hysteresis comparator based on an external clock signal.

The comparison between this work and prior art within the same switching frequency range and/or with integrated filters, is given in Table 2. As can be seen, the majority of

Table 2 A sample of the state-of-the-art, high switching speed, integrated DC–DC converters in silicon and GaAs technologies

Ref.	Technology	No. of phases	V_{in}/V_{out}(V/V)	I_{out} (A)	f_{sw} (MHz)	L (nH)	Eff. (%)
[15]	0.13 μm CMOS	2	1.2/0.9	0.19	170	2 on die	77.9
[16]	90 nm CMOS	4	1.2/0.9	0.3	233	6.8 SMT	82.5
[18]	0.18 μm BICMOS	2	2.8/1.8	0.2	45	11 on die	64
[12]	Discrete	1	16/12	0.833	100	100 SMT	72
[19]	0.18 μm BiCMOS	2	1.8/0.9	0.5	200	2.14 on die	64
[20]	0.13 μm CMOS	1	1.2/0.8	0.12	180	8.22 SMT	80
[21]	0.18 μm CMOS	1	3.6/1.8	0.15	140	18 bondwire	65
This work	0.5 μm GaAs p-HEMT	2	4.5/3.3	1	150	8.77 on die	85.68

DC–DC converters in CMOS technology do not satisfy the high output power requirements of communication standards such as GSM/EDGE and WCDMA. Also, the efficiency of the majority of CMOS prototypes with integrated filters is well below 80%. Hysteresis controller provides a fast transient response for high speed DC–DC converters. Measurement results of the output switching stage and gate driver as well as simulation results of the closed loop hysteretic controller show an expected peak efficiency of 85.68% at 150 MHz.

6 Conclusion

A high efficiency, high frequency two stage interleaved DC–DC converter with negative coupling has been demonstrated in 0.5 μm, p-HEMT GaAs technology. GaAs technology provides a faster switch with lower on-resistance and smaller parasitic capacitors compared to CMOS technology. The inductors are fabricated in 65 μm thick copper layer and achieve Q of 26 at 150 MHz when flip mounted. The interleaved open-loop converter achieves a measured peak efficiency of 84% at 150 MHz with 4.5/3.3 V output and 1 A load current. Hysteresis control of the DC–DC converter provides fast output regulation for high frequency switching. The control loop is designed in 0.25 μm BiCMOS technology using 3.3 V thick oxide transistors. The complete closed loop converter achieves a simulated peak efficiency of 85.68% at 150 MHz with efficiency variation of only 11% from 1 to 3.3 W. The proposed architecture and AlGaAs/GaAs technology are suitable for high frequency, high efficiency DC–DC converters for integration with GaAs power amplifier modules.

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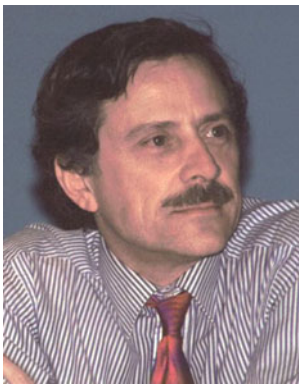
References

1. Kitchen, J. N., Deligoz, I., Kiaei, S., & Bakkaloglu, B. (2007). Polar SiGe class E and F amplifiers using switch-mode supply modulation. *IEEE Transactions on Microwave Theory and Techniques, 55*(5), 845–856.
2. Qin, J., Guo, R., Park, J., & Huang, A. (2009). A low noise. High efficiency two stage envelope modulators structure for EDGE polar modulation. In *Proceedings of IEEE international symposium on circuits and systems*, pp. 1089–1092, Taipei.
3. Hanington, G., Chen, P.-F., Asbeck, P., & Larson, L. (1999). High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications. *IEEE Transactions on Microwave Theory and Techniques, 47*(8), 1471–1476.
4. Wong, J. (1990). A low noise low dropout regulator for portable equipment. In *Proceedings of Power conversion and intelligent motion*, pp. 38–43, May 1990.
5. Gupta, V., & Rincon-Mora, G. (2007). A 5 mA 0.6 μm CMOS Miller-compensated LDO regulator with −27 dB worst-case power-supply rejection using 60 pF of on-chip capacitance. In *Proceedings of IEEE international solid-state circuits conference*, pp. 520–521, February 2007.
6. Lam, Y.-H., & Ki, W.-H. (2008). A 0.9 V 0.35 μm adaptively biased CMOS LDO regulator with fast transient response. In *Proceedings of IEEE international solid-state circuits conference*, pp. 442–626, February 2008.
7. Al-Kuran, S., Scheinberg, N., & Saders, J. V. (2000). GaAs switched capacitor DC-to-DC converter. *IEEE Journal of Solid-State Circuits, 35*(8), 1121–1127.
8. Favrat, P., Deval, P., & Declercq, M. (1998). A high-efficiency CMOS voltage doubler. *IEEE Journal of Solid-State Circuits, 33*(3), 410–416.
9. Ma, D., Su, L., & Somasundaram, M. (2010). Integrated interleaving SC power converters with analog and digital control schemes for energy-efficient microsystems. In *Proceedings of Analog integrated circuits and signal*, pp. 361–372, March 2010.
10. Severns, R., & Bloom, G. (1985). *Modern DC–DC switch mode power converter circuits*. Van Nostrand Reinhold.
11. Ajram, S., & Salmer, G. (2001). Ultrahigh frequency DC-to-DC converters using GaAs power switches. *IEEE Transactions on Power Electronics, 16*(5), 594–602.
12. Rivas, J. M., Jackson, D., Leitermann, O., Sagneri, A. D., Han, Y., & Perreault, D. J. (2006). Design considerations for very high frequency dc–dc converters. In *Proceedings of IEEE power electronics specialists conference (PESC '06)*, pp. 1–11, June 2006.
13. Kwak, T.-W., Lee, M.-C., & Cho, G.-H. (2007). A 2W CMOS hybrid switching amplitude modulator for EDGE polar transmitters. *IEEE Journal of Solid-State Circuits, 42*(12), 2666–2676.
14. Chu, W.-Y., Bakkaloglu, B., & Kiaei, S. (2008). A 10 MHz-bandwidth 2 mV-ripple PA-supply regulator for CDMA transmitters. In *Proceedings of IEEE international solid-state circuits conference*, pp. 448–626, February 2008.
15. Wibben, J., & Harjani, R. (2008). A high-efficiency DC–DC converter using 2 nH integrated inductors. *IEEE Journal of Solid-State Circuits, 43*, 844–854.
16. Hazucha, P., Schrom, G., Hahn, J., Bloechel, B., Hack, P., Dermer, G., Narendra, S., Gardner, D., Karnik, T., De, V., & Borkar, S. (2005). A 233-MHz 80%-87% efficient four-phase DC–DC converter utilizing air-core inductors on package. *IEEE Journal of Solid-State Circuits, 40*, 838–845.
17. Schrom, G., Hazucha, P., Hahn, J., Gardner, D., Bloechel, B. A., Dermer, G., Narendra, S., Karnik, T., & De, V. (2004). A 480-MHz, multi-phase interleaved buck DC–DC converter with hysteretic control. In *Proceedings of IEEE power electronics specialists conference (PESC '04)*, pp. 4702–4707, June 2004.
18. Abedinpour, S., Bakkaloglu, B., & Kiaei, S. (2007). A multistage interleaved synchronous buck converter with integrated output filter in 0.18 μm SiGe process. *IEEE Transactions on Power Electronics, 22*(6), 2164–2175.
19. Sun, J., Lu, J., Giuliano, D., Chow, T., & Gutmann, R. (2007). 3D power delivery for microprocessors and high-performance ASICs. In *Proceedings of IEEE applied power electronics conference (APEC '07)*, pp. 127–133, February 2007.
20. Li, P., Bhatia, D., Xue, L., & Bashirullah, R. (2008). A 90–240 MHz hysteretic controlled DC–DC buck converter with digital PLL frequency locking. In *Proceedings of Custom integrated circuits conference*, pp. 21–24, September 2008.
21. Wen, M., & Steyaert, M. (2008). A fully-integrated 0.18 μm CMOS DC–DC step-down converter, using a bondwire spiral inductor. In *Proceedings of Custom integrated circuits conference*, pp. 17–20, September 2008.
22. Wong, P.-L., Xu, P., Yang, P., & Lee, F. (2001). Performance improvements of interleaving VRMs with coupling inductors. *IEEE Transactions on Power Electronics, 16*(5), 499–507.
23. Abu-Qahouq, J., Batarseh, M., Huang, L., & Batarseh, I. (2007). Analysis and small signal modeling of a non-uniform multiphase

buck converter. In *Proceedings of IEEE power electronics specialists conference (PESC '07)*, pp. 961–967, June 2007.
24. Pala, V., Varadarajan, K., & Chow, T. (2009) GaAs pseudomorphic HEMTs for low voltage high frequency DC–DC converters. In *Proceedings of international symposium on Power semiconductor devices and IC's*, pp. 120–123, June 2009.
25. Erickson, R. W., & Maksimovic, D. (2001). *Fundamentals of power electronics* (2nd ed.). New York: Springer.
26. ASITIC, http://rfic.eecs.berkeley.edu/niknejad/asitic.html.
27. Li, P., Xue, L., Hazucha, P., Karnik, T., & Bashirullah, R. (2009). A delay-locked loop synchronization scheme for high-frequency multiphase hysteretic dc–dc converters. *IEEE Journal of Solid-State Circuits, 44*(11), 3131–3145.
28. Maneatis, J., & Horowitz, M. (1993). Precise delay generation using coupled oscillators. *IEEE Journal of Solid-State Circuits, 28*(12), 1273–1282.
29. Maneatis, J. (1996). Low-jitter process-independent dll and pll based on self-biased techniques. *IEEE Journal of Solid-State Circuits, 3*(11), 1723–1732.
30. Hass, K. J., & Cox, D. F. (2000) Level shifting interfaces for low voltage logic. In *9th NASA symposium on VLSI design*, pp. 3.1.1–3.1.7.
31. Coilcraft, available at http://www.coilcraft.com.

Han Peng received the B.S. degrees in Electrical Engineering from Southeast University, Nanjing, P.R. China, in 2006. She is currently a Ph.D. candidate in the Electrical, Computer and Systems Engineering Department, Rensselaer Polytechnic Institute, Troy, NY. She was a research assistant in the Institute of RF&-OE-ICs., at Southeast University, Nanjing, P.R. China, from 2006 to 2007. During summer of 2009, she was with TriQuint Semiconductor Inc., Hillsboro, OR, developing high frequency, fully integrated DC–DC converter systems. She is currently intern at National Semiconductor Inc's research laboratory. Her research interests are in the area of fully integrated power management circuit design.

Vipindas Pala received his Bachelors and Masters degree in Electrical Engineering from Indian Institute of Technology, Chennai, India in 2007 and is currently working towards his Ph.D. Degree in Rensselaer Polytechnic Institute, Troy, NY, USA. His research interests include power device design, compound semiconductor device physics and high speed circuit design.



Peter Wright has been with TriQuint Semiconductor in Hillsboro, Oregon since 2000. Before that he was with Thomson-Microsonics in Sophia-Antipolis, France. He has worked widely in Europe and the United States. He holds undergraduate degrees from Cambridge University, UK, and an S.M. and Ph.D. from MIT, Boston, MA. For many years he was involved with the development of surface acoustic wave devices and acoustic signal processing. He pioneered many of the architectures and analysis techniques for SAW single-phase unidirectional transducers and resonators. While at Schlumberger, he developed a fast algorithm for processing wellbore evaluation logs to image cement integrity on the outside of the casing. At TriQuint Semiconductor, he has focused on the development of advanced RF front-end modules for cellular handsets.

T. Paul Chow was a member of the technical staff at GE-CRD from 1977 to 1989. Since 1989, he has been with RPI, where he is now professor of the Electrical, Computer and Systems Engineering Department. He has been working in the power semiconductor device area since 1982. His present research activities include novel device concepts, processing and circuit models for high-voltage silicon, GaAs and wide bandgap (particularly SiC and GaN) semiconductor power devices. He has published over 100 papers in scientific journals, has contributed seven chapters in technical textbooks, and has filed over fifteen patents. He is a fellow of the IEEE and a member of the Electrochemical Society.

Mona Mostafa Hella received the B.Sc. and Masters degrees with Honors from Ain-Shams University, Cairo, Egypt, in 1993, and 1996, and the Ph.D. degree, in 2001, from The Ohio-State University, Columbus, Ohio, all in Electrical Engineering. From 1993 to 1997, she was a teaching and research assistant at Ain Shams University. From 1997 to 2001 she was a research assistant at the Ohio-state University. She was with the Helsinki University of Technology (HUT), Espoo, Finland as a visiting scholar in the summer of 1998, and with the analog group at Intel cooperation, Chandler, AZ in summer 1999. She was a senior designer at Spirea AB,

Stockholm, Sweden working on CMOS power amplifiers (2000–2001). From 2001 to 2003, she was a senior designer at RFMD Inc, Billerica, MA working on Optical communication systems, as well as silicon-based wireless systems. She joined the Electrical, Computer and Systems Engineering department at Rensselaer Polytechnic Institute as an Assistant Professor in 2004. Her research interests include the areas of mixed-signal and RFIC design for wireless and wire-line applications.