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Digitally programmable high-order current-mode universal filters

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Abstract New high-order current-mode (CM) filter topologies capable of providing all functions simultaneously are presented. The proposed filters are based on digitally controlled current amplifiers and unity gain voltage buffers. The gains of the current amplifiers are digitally programmed to adjust the filters' transfer function coefficients. It is shown that the proposed approach results in more efficient realizations compared with its counterparts based on other CM active elements. Using BSIM3 0.18 μm CMOS models, simulation results of a fourth-order universal filter are provided.

Keywords CMOS mixed analog/digital systems · Current-mode circuits · Active filters · High order filter

1 Introduction

The general transfer function of an *n*th-order filter response is given by:

$$T(s) = \frac{N(s)}{D(s)} = \frac{a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0}{s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + b_0}, \qquad (1)$$

where a_0 through a_n are real numbers, and b_0 through b_{n-1} are positive real numbers. An *n*th-order universal filter (UF) can realize not only (1) but also any other function with various numerator polynomials. This is typically achieved by designing a filter providing basic responses, namely $a_i s^i / D(s)$ for $i = 0$ to n, simultaneously. Then, other functions including (1) are obtained by properly adding and/or subtracting these basic responses. In other word, the *n*th-order UF is a general purpose filter that can be flexibly used to realize any *n*th order function and hence serve wide range of applications. In integrated circuit (IC) applications, changing the circuit hardware is not possible. Therefore, for a given UF to be compatible with IC implementation, it has to satisfy the following two conditions. First, it must be reconfigurable without changing the hardware to promote the realization of different types of functions. Second, it must exhibit programmable parameters to adjust the filter frequency response. It is mandatory in IC applications, to compensate for components, process and temperature variations.

One approach to realize high-order multi-output UFs is via cascading second-order sections. Advantages of this approach are ease of design and that tuning can be done separately for each section. However, this approach may lead to less efficient design solutions when multi-functions filters are required. For instance, consider a second-order UF1 with lowpass (LP), bandpass (BP), and highpass (HP) outputs; and it is required to develop their fourth-order responses. This can be achieved using the cascading topology shown in Fig. 1. When the LP output of UF1 is applied as an input to UF2, then the output will be fourth-order BP, fourth-order LP and one output wherein N(s) is proportional to s^1. Note that there is no need to cascade the BP output of UF1. Whereas, when the HP output of the UF1 is use as input to UF3, then N(s) of the three outputs will be proportional to s^4, s^3 and s^2. This means that a fourth-order HP and fourth-order BP filters are obtained. Hence, it is clear that three 2nd-order sections are required to generate fourth-order LP, BP, and HP filters. Also, the same three sections can be used to realize any other fourth-order function as all terms of s^0 to s^4 are available at the outputs of UF2 and UF3. However, it can be seen that as the required filter order is increased, this approach will be

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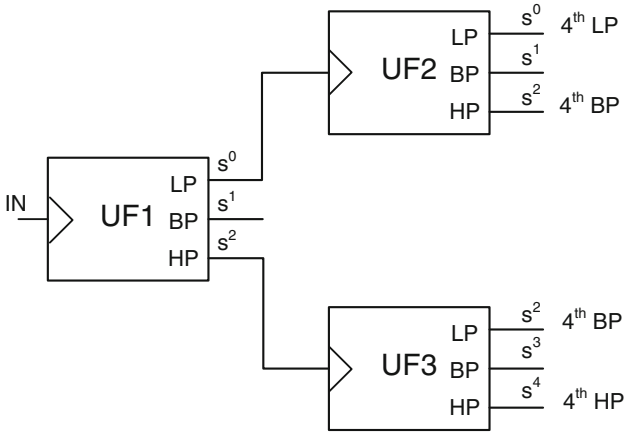

Fig. 1 Cascading of second-order UF sections to develop fourth-order UF

more inefficient. For example, to realize sixth-order UF, total of six 2nd-order sections will be needed.

Several high-order transfer function realizations based on current-mode building blocks (CMBBs), transconductance amplifiers (gm), operation transconductance amplifiers (OTAs) were suggested [1–21]. These filters can be classified, based on the type of the input and output signals, as voltage-mode (VM) [1–10, 19, 21] and CM [11–20]. However, all of the filters from [1–16] can realize one function at a time. Thus, changing the filter type would require modifying the hardware of the circuit topology. Therefore, they are unsuitable for monolithic implementation. The second disadvantage that hinders the use of most of these filters in IC applications is the absence of programmability feature.

On the other hand, the CM filters suggested in [17–20] can realize any filter function without changing the circuit topology. In fact, they provide various basic responses (i.e. $a_i s^i/D(s)$ for $i = 0$ to n) simultaneously. Hence, any other function can be obtained by proper addition and/or subtraction of the basic responses. Also, they offer programmability feature to tune the filters' parameters electronically. The filters in [17, 18] are single input topologies, whereas the filters in [19, 20] use multiple inputs. Therefore, they require extra circuitry to generate copies of the input signal. The filter in [17] uses relatively large number of active elements namely $3n + 2$ electronically tunable current conveyors (ECCIIs). A ECCII consists of CCII and a current amplifiers employed between the X and Z terminals of CCII to provide current gain. But, the operation of ECCII circuits is valid only for small signals processing. The filters proposed in [18, 19] have the disadvantage of requiring impractical number of outputs from one of the OTAs. The feedforward network necessitates the use of an OTA with as many outputs as the filter-order. Also, the filter in [20], based on current-controlled current conveyor (CCCII), suffers from the same disadvantage. For *n*th-order filter, a CCCII with 'n' outputs is required. In addition, the filter is electronically tunable by controlling r_x, but the resistance at X terminal is non-linear for large signals and is also dependent on temperature. The linearity of the filter is therefore expected to be poor. The VM based filter proposed in [21] uses field programmable analog array to realize high order functions. Although the filter can realize the filter transfer functions by interconnecting proper gm cells in the array, this technique results in large number of active elements.

This work uses signal flow graph approach to realize (1) and adapts suitable active elements namely digitally controlled current amplifiers (DCCAs) and voltage buffers (VBs) for its realization. Section 2 presents the proposed approach and Sect. 3 describes the proposed filters. Comparison with recent works is given in Sect. 4 and non-ideal analysis is provided in Sect. 5. Simulation results are given in Sect. 6.

2 Proposed approach

Filter designs based on CMBBs has the potential to provide higher bandwidth and better linearity than their counterparts based on op-amps and gm (OTAs), respectively. A

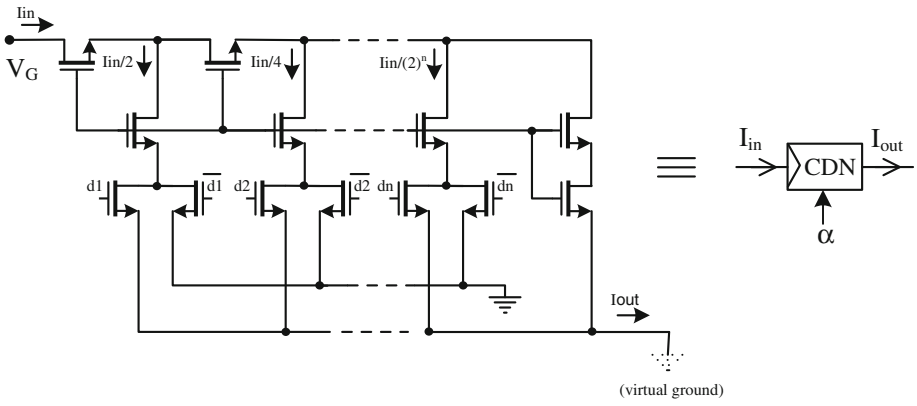

Fig. 2 CMOS realization of CDN [25] and its symbol

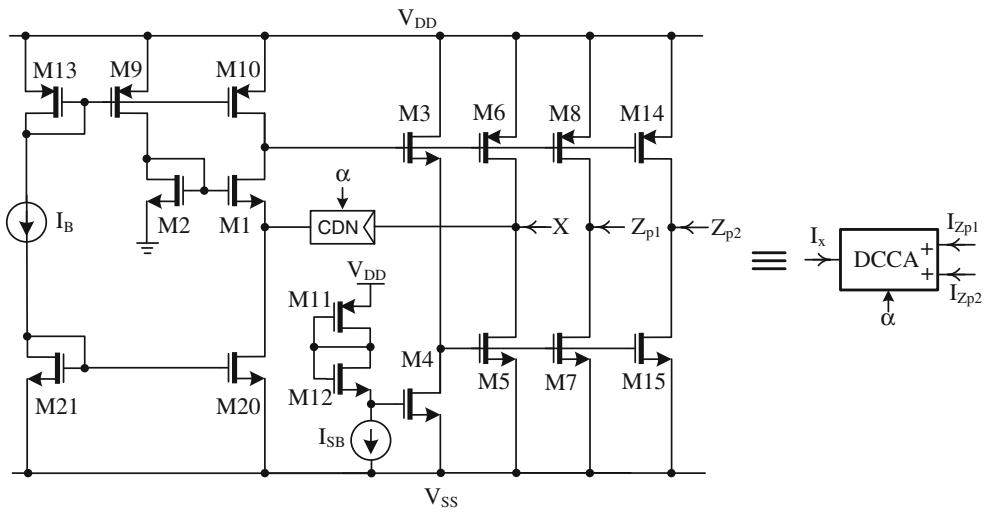

Fig. 3 Dual-output DCCA CMOS realization and its symbol

current follower (CF) has inherent advantages of wide bandwidth, large signal swings, and low power consumption. Similarly a current division network (CDN) can be utilized in the design of the CF to form DCCA, which gives the advantage of programmability. The input port virtual ground property of the DCCA facilitates the addition of different signals. In this paper, DCCAs are used to realize (1). Unlike VM amplifiers, changing the gain of CM amplifiers does not degrade the bandwidth of operation. Recently, digitally programmable devices such as those in [22–25] have become attractive for mixed digital-analog applications. In this paper, DCCAs are used to realize (1). A low-power CMOS realization of the DCCA using the CDN for varying the gain was used in [25]. The CDN exhibits wide bandwidth, inherent linearity (i.e. insensitive to second order effects and valid in all MOS operating regions) and simple structure as shown in Fig. 2. A CMOS realization of a dual output Class-AB DCCA is shown in Fig. 3.

The DCCA exhibits the following relationship:

$$I_{Zp1} = I_{Zp2} = \alpha I_X \text{ with } \alpha = 1/\sum_{i=1}^{n} d_i 2^{-i}, \tag{2}$$

where α represents the current gain of the DCCA, the signs denote the positive type (both currents are going in) and d_i is the ith digital bit and n is the size of control word of the CDN. The gain of the amplifier can be changed digitally by programming the digital word. In addition, a DCCA exhibits ideally zero input impedance and infinite output impedance. The input port virtual ground property of the DCCA facilitates the addition of different signals. In order to allow the distribution of output signal to different nodes, a VB can be added at the output terminal of the DCCA. A class-AB VB with high bandwidth was also presented in [25]. CMOS realization of a low power VB with class-AB output stage is shown in Fig. 4.

The design of high-order continuous-time filters often utilizes signal flow graph adopting integrators as basic building blocks. The general transfer function of the nth-order filter given in (1) can be described by signal flow graph approach shown in Fig. 5. Routine analysis shows that the different outputs for $i = 0$ to n can be expressed as follows:

$$\frac{S_i(s)}{S_s(s)} = \frac{\prod_{k=i}^{n} a_k s^i}{s^n + b_{n-1}a_{n-1}s^{n-1} + b_{n-2}a_{n-1}a_{n-2}s^{n-2} + \cdots + b_1 a_{n-1}a_{n-2}\ldots a_1 s + b_0 a_{n-1}a_{n-2}\ldots a_1 a_0}. \tag{3}$$

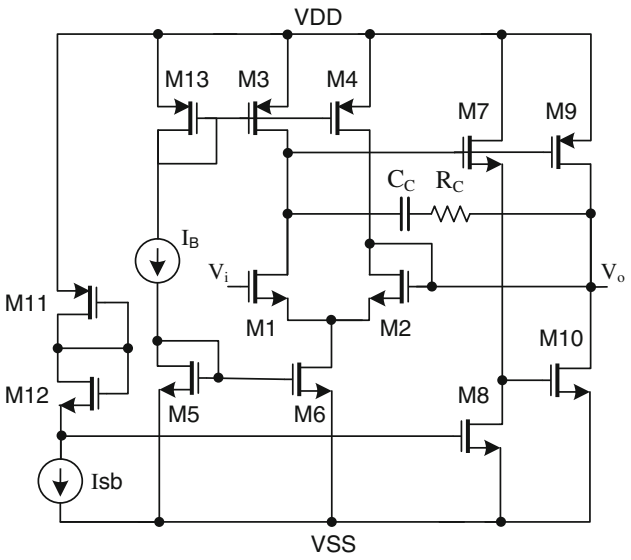

Fig. 4 Class AB VB CMOS realization

The output signals S_i can be properly added to realize the general transfer function of (1) yielding the following relation:

function. First, adjust the coefficients of numerator by choosing a_n, a_{n-1}, …, a_1 and a_0 in the given order. Then, the coefficients of denominator polynomial can be adjusted independently by selecting b_0 through b_{n-1}.

3 Proposed filter

Adoption of DCCAs and VBs makes the realization of the signal flow graph shown in Fig. 5 straightforward. Single-input multi-output topologies are usually used to realize CM UFs. Unlike VM counterparts, basic function ($a_i s^i/D(s)$ for $i = 0$ to n) can be properly added and/or subtracted to generate other functions without additional summer. To realize the feedback factors of Fig. 5, resistors are connected between the outputs of the integrators back to the input virtual ground of the first integrator. An additional CF (a unity gain DCCA) is needed to realize the negative signs in some of the feedback factors as shown in Fig. 6. The CF in the feedback can be eliminated if the use of negative type DCCA is allowed. However, it is expected that the design of Fig. 6 is more

$$T(s) = \frac{a_n s^n + a_n a_{n-1} s^{n-1} + \cdots + a_n a_{n-1} a_{n-2} \ldots a_1 s + a_n a_{n-1} a_{n-2} \ldots a_1 a_0}{s^n + b_{n-1} a_{n-1} s^{n-1} + b_{n-2} a_{n-1} a_{n-2} s^{n-2} + \cdots + b_1 a_{n-1} a_{n-2} \ldots a_1 s + b_0 a_{n-1} a_{n-2} \ldots a_1 a_0}. \quad (4)$$

The switches in Fig. 5 are used to set any coefficient of the numerator polynomial to zero. If the output signals are currents then summation is simply achieved through connections of output wires. The following procedure can be adapted to adjust all parameters to meet a given transfer

power and area efficient than that option. Note that terminal (C) of Fig. 6 will be feedback to terminal (A) if the filter order is odd or terminal (B) if the order is even. It can be shown that the transfer function assuming n is even are given by:

$$\frac{i_n(s)}{i_s(s)} = \frac{\alpha_n \alpha_{n-1} s^n}{s^n + \frac{\alpha_{n-1}}{C_{n-1} R_{bn-1}} s^{n-1} + \frac{\alpha_{n-1}\alpha_{n-2}}{C_{n-1} C_{n-2} R_{n-1} R_{bn-2}} s^{n-2} + \cdots + \frac{\alpha_{n-1}\alpha_{n-2}\ldots\alpha_1}{C_{n-1}\ldots C_1 R_{n-1}\ldots R_2 R_{b1}} s + \frac{\alpha_{n-1}\alpha_{n-2}\ldots\alpha_1\alpha_0}{C_{n-1}\ldots C_0 R_{n-1}\ldots R_1 R_{b0}}} \quad (5a)$$

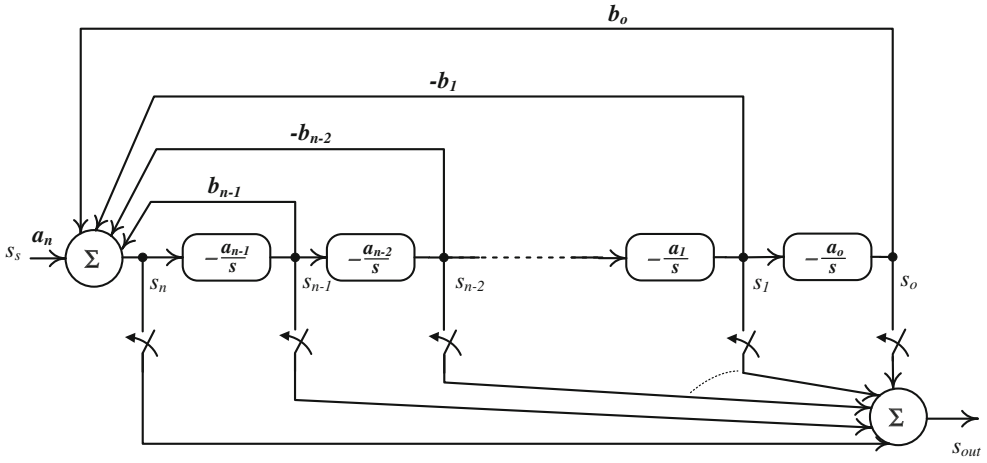

Fig. 5 A signal-flow graph model of T(s) based on integrator-loops

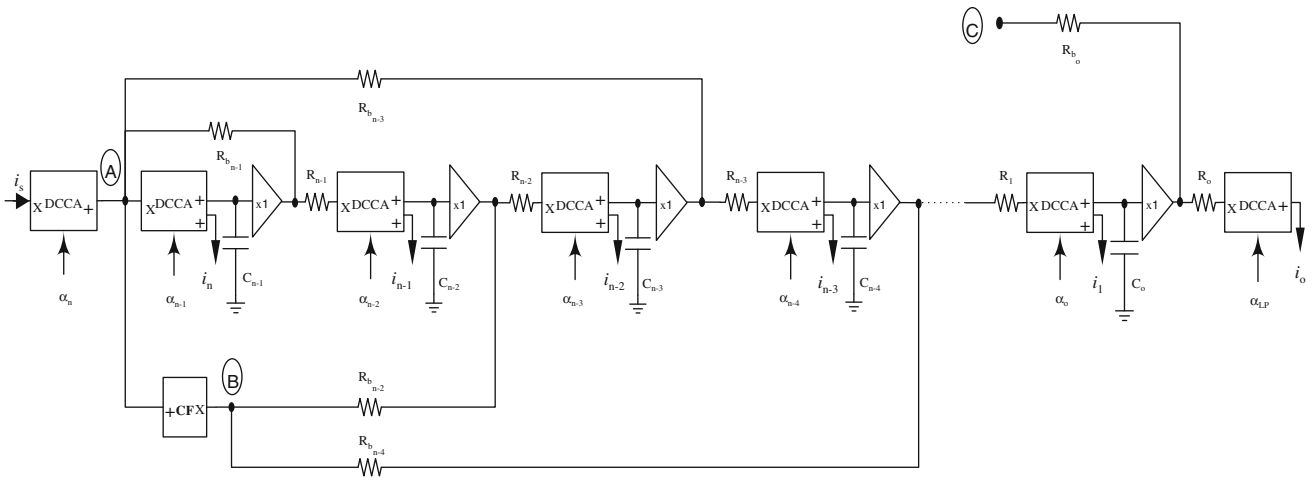

Fig. 6 The original CM filter circuit

$$\frac{i_m(s)}{i_s(s)} = (-1)^m \frac{s^m \prod_{j=m-1}^{n} \alpha_j \prod_{i=m}^{n-1} \frac{1}{C_i R_i}}{s^n + \sum_{i=0}^{n-1} \left((s^i R_i)/R_{bi}\right) \prod_{j=i}^{n-1} \alpha_j/(C_j R_j)} \quad \text{for m} = 1 \text{ to n} - 1 \tag{5b}$$

$$\frac{i_0(s)}{i_s(s)} = \frac{\alpha_{LP} \prod_{j=0}^{n} \alpha_j \prod_{i=0}^{n-1} 1/(C_i R_i)}{s^n + \sum_{i=0}^{n-1} \left((s^i R_i)/R_{bi}\right) \prod_{j=i}^{n-1} \left(\alpha_j/(C_j R_j)\right)}. \tag{5c}$$

For this topology, it can be seen that either the coefficients of the numerator or the denominator can be tuned using the different α_i. For example, the coefficients of D(s) can be adjusted by selecting α_0 to α_n, but the coefficients of the numerator cannot be arbitrarily chosen. In order to provide programmability feature to all coefficients, the feedback paths which uses passive resistors must be modified. New DCCAs can be inserted in series with each resistor as shown in Fig. 7. Note that terminal (C) of Fig. 7 will be feedback to terminal (A) if the filter order is even or terminal (B) if the order is odd. This change leads to the following transfer functions:

$$\frac{i_n}{i_s} = \frac{\alpha_n \alpha_{n-1} s^n}{s^n + \frac{\alpha_{n-1}\alpha_{bn-1}}{C_{n-1}R_{bn-1}} s^{n-1} + \frac{\alpha_{n-1}\alpha_{n-2}\alpha_{bn-2}}{C_{n-1}C_{n-2}R_{n-1}R_{bn-2}} s^{n-2} + \cdots + \frac{\alpha_{n-1}\alpha_{n-2}\ldots\alpha_1\alpha_{b1}}{C_{n-1}\ldots C_1 R_{n-1}\ldots R_2 R_{b1}} s + \frac{\alpha_{n-1}\alpha_{n-2}\ldots\alpha_1\alpha_0\alpha_{b0}}{C_{n-1}\ldots C_0 R_{n-1}\ldots R_1 R_{b0}}}. \tag{6a}$$

In general,

$$\frac{i_m(s)}{i_s(s)} = (-1)^m \frac{s^m \prod_{j=m-1}^{n} \alpha_j \prod_{i=m}^{n-1} 1/(C_i R_i)}{s^n + \sum_{i=0}^{n-1} \left((s^i R_i \alpha_{bi})/R_{bi}\right) \prod_{j=i}^{n-1} \alpha_j/(C_j R_j)} \quad \text{for m} = 1 \text{ to n} - 1 \tag{6b}$$

$$\frac{i_0(s)}{i_s(s)} = \frac{\alpha_{b0} \prod_{j=0}^{n} \alpha_j \prod_{i=0}^{n-1} 1/(C_i R_i)}{s^n + \sum_{i=0}^{n-1} \left((s^i R_i \alpha_{bi})/R_{bi}\right) \prod_{j=i}^{n-1} \alpha_j/(C_j R_j)}. \tag{6c}$$

This means that each R_{bi} in $D(s)$ of (5a–5c) is replaced by R_{bi}/α_{bi}. Now the coefficients of numerator can be adjusted by choosing α_i whereas the coefficients of the denominator can be tuned independently by selecting α_{bi}. Also, the LP function output current is now available from the last DCCA added in the feedback path. This eliminates the use of the extra DCCA of Fig. 6 required to provide i_0.

4 Comparison with other solutions

Table 1 shows a summary of the main characteristics of the proposed filter. For fair comparison, different building blocks are decomposed as number of followers. Each of the CCCII and ECCII is equivalent to a VF and a CF. The following performance characteristics are considered: (1) No need to use extra circuit to generate copies of the input signal, (2) Electronically tuned coefficients, (3) Total number of followers, (4) Low input impedance, (5) High output impedances, (6) Number of resistors, (7) Number of capacitors, and (8) Grounded capacitors. Criteria 2 is further decomposed into criteria 2(i) and 2(ii) which denotes the presence of the programmability feature for the denominator and numerator coefficients, respectively. The

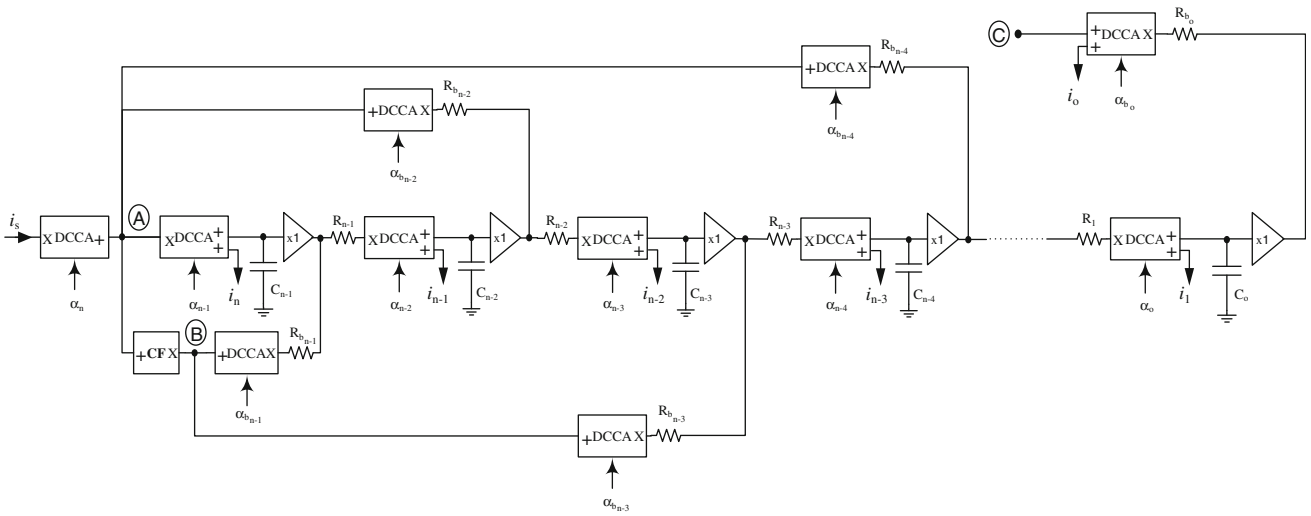

Fig. 7 The modified design of CM filter circuit of Fig. 6 using DCCA in the feedback

Table 1 Comparison of the proposed high-order filter circuits

Proposed filter	(1)	(2)		(3)	(4)	(5)	(6)	(7)	(8)
		(i)	(ii)						
CM based on ECCII [17]	Yes	Yes	Yes	$6n + 4$	Yes	Yes	$3n + 2$	n	Yes
CM based on gm [18]	Yes	Yes	No	NA	No	Yes	None	n	Yes
CM based on OTA [19]	No	Yes	No	NA	Yes	Yes	None	n	Yes
CM based on CCCII [20]	No	Yes	No	$2n$	No	Yes	None	n	Yes
CM filter of Fig. 6	Yes	Yes	No	$2n + 3$	Yes	Yes	$2n$	n	Yes
CM filter of Fig. 7	Yes	Yes	Yes	$3n + 2$	Yes	Yes	$2n - 1$	n	Yes

characteristics of the filters presented in [17–20] are included for comparison.

The filter presented in [17] and the proposed filter of Fig. 7 have the advantage of providing programmability of numerator and denominator coefficients. The proposed filter of Fig. 7 requires considerably less number of followers and passive resistors compared with its counterpart of [17]. On the other hand, the filters of [18–20] and the proposed filter of Fig. 6 employ less number of active elements but do not provide adjustment of the numerator coefficients. Although the filter in [20] uses three followers less than its counterpart of Fig. 6, it requires extra circuit to generate copies of the input signal as well as one of its CCCII must have n outputs. Therefore, Fig. 6 is expected to require less power consumption than the filter of [20] when n is large.

5 Investigate the non-idealities associated with the proposed designs

The non-ideal ac response of the filter can be found by considering the non-ideal effects of the DCCA and CF characterized by input parasitic impedance (Z_x) and output parasitic conductance (Y_z). Since the DCCA is designed to exhibit low input impedance and high output impedance, Z_x and Y_z are dominated by series resistance (r_x) and parallel capacitance (C_z), respectively. Similarly, the non-ideal terminal characteristics of the VB can be modeled by shunt capacitance C_b and series resistance r_b at the input and output ports, respectively.

For the topology of Fig. 6, the effect of C_z for $DCCA_0$ through $DCCA_{n-1}$ can be easily observed as they are in parallel with the passive capacitances. Thus, their values can be absorbed as $C'_i = C_i + C_{zi}$ (for i = 0 to n − 1). Also, r_x for $DCCA_0$ through $DCCA_{n-2}$ are in series with forward path passive resistors. Thus, their values can be absorbed as $R'_i = R_{i+1} + r_{xi}$ (for i = 0 to n − 2). Therefore, the effects of the parasitic will manifest themselves at nodes A due to $r_{x(n-1)}$, C_{zn} and output capacitance of the feedback CF (C_{zf}); and node B due to the input resistance of the feedback transistor r_{xf}. The effect of r_x of the feedback CF can be neglected given that it is much smaller than the passive resistors connected at node B. On the other hand, effect of C_{bi} for all VBs can be easily absorbed as they are in parallel with the passive capacitances. Thus,

their values can be absorbed as $C_i' = C_i + C_{zi} + C_{bi}$ (for i = 0 to n − 1). Also, the effect of r_{bi} can be neglected as the VB are loaded with much larger resistive loads. For example, it can be shown that non-ideal analysis of the fourth-order filter will yield the following relations:

$$\frac{i_4}{i_i} = \frac{s^4\alpha_4\alpha_3}{D(s)} \tag{7a}$$

$$\frac{i_3(s)}{i_s(s)} = -\frac{\alpha_4\alpha_3\alpha_2 s^{n-1}}{C_3R_3}/D(s) \tag{7b}$$

$$\frac{i_2(s)}{i_s(s)} = \frac{\alpha_4\alpha_3\alpha_2\alpha_1 s^2}{C_3C_2R_3R_2}/D(s) \tag{7c}$$

$$\frac{i_1(s)}{i_s(s)} = -\frac{\alpha_4\alpha_3\alpha_2\alpha_1\alpha_0 s}{C_3C_2C_1R_3R_2R_1}/D(s) \tag{7d}$$

$$\frac{i_0(s)}{i_s(s)} = \frac{\alpha_4\alpha_3\alpha_2\alpha_1\alpha_0\alpha_{LP}}{C_3C_2C_1C_0R_3R_2R_1R_0}/D(s) \tag{7e}$$

$$\begin{aligned} D(s) = {} & s^5C_Ar_{x3} + s^4\left(1 + \frac{r_{x3}}{R_{b3}} + \frac{r_{x3}}{R_{b1}}\right) + s^3\frac{\alpha_3}{C_3R_{b3}} \\ & + s^2\frac{\alpha_{CF}\alpha_3\alpha_2}{C_3C_2R_3R_{b2}}\left(1 - \frac{r_{xf}R_{b2}}{K} - \frac{r_{xf}R_{b0}}{K}\right) \\ & + s^1\frac{\alpha_3\alpha_2\alpha_1}{C_3C_2C_1R_3R_2R_{b1}} + \frac{\alpha_{CF}\alpha_3\alpha_2\alpha_1\alpha_0}{C_3C_2C_1C_0R_3R_2R_1R_{b0}} \\ & \times\left(1 - \frac{r_{xf}R_{b2}}{K} - \frac{r_{xf}R_{b0}}{K}\right), \end{aligned} \tag{7f}$$

where

$$K = R_{b2}R_{b0} + r_{xf}R_{b2} + r_{xf}R_{b0}. \tag{7g}$$

It can be seen that r_{x3} results in introducing s^5 term in D(s) and error in its s^4 coefficient. The error s^4 can be safely neglected as long as r_{x3} is kept small. But the s^5 term will cause deviations in the high frequency response compared with the ideal response. It can be shown for frequencies 'ω' much smaller than $1/C_Ar_{x3}$ (C_A is the total capacitance at node A), the effect of s^5 term can be neglected. On the other hand, r_{xf} introduces the error only in the coefficient of s^0 and s^2. These errors can be safely neglected as long as r_{xf} is kept small. It can be seen that the deviation of the non-ideal responses due to the non-ideal terminal characteristics of DCCA and VB is in general small. The main problem is associated with the high pass response where the parasitic pole due to r_{x3} will result in high frequency roll off.

6 Simulation results

A fourth-order filter was simulated using BSIM3 0.18 μm CMOS models available through MOSIS. The aspect ratios of the MOSFETS for DCCA and VB of Figs. 3 and 4 are given in Table 2, whereas, the model parameters of the MOSFETS can be obtained from http://www.mosis.com/Technical/Testdata/tsmc-018-prm.html. The supply voltages were set to ±1.5 V, and biasing currents were $I_B = 20$ μA and $I_{SB} = 5$ μA. The compensation capacitor and resistor for VB were 0.1 pF and 0.5 kΩ.

Figure 8 shows the LP, BP and HP responses obtained when all resistors, capacitors, and alphas are respectively selected as R = 6.4 kΩ, C = 50 pF and α = 1.

The programmability feature will be demonstrated by considering the LP function in the following example.

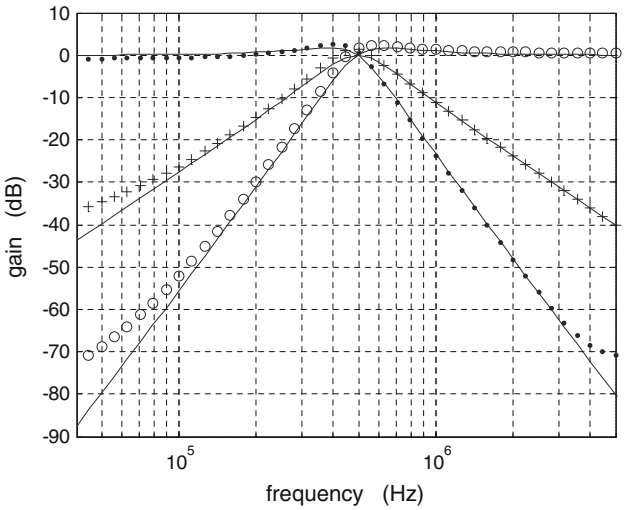

Fig. 8 Simulation results for fourth-order lowpass, bandpass and highpass functions

Table 2 Aspect ratios for DCCA and VB

Aspect ratios for DCCA of Fig. 3		Aspect ratios for VB of Fig. 4	
MOSFETs	W/L (μm)	MOSFETs	W/L (μm)
M1 and M2	4.32/0.36	M1 and M2	20.16/0.36
M3 and M4	2.52/2.52	M3, M4, and M13	5.04/0.36
M6, M8, M11, and M14	6.12/0.18	M5 and M6	4.32/0.36 and 8.64/0.36
M5, M7, M12, and M15	1.8/0.18	M7 and M8	2.52/2.52
M9, M10, and M13	5.04/0.36	M9 and M11	6.12/0.18
M20 and M21	6.12/0.36	M10 and M12	1.8/0.18

Table 3 Values for alphas to provide Butterworth and Chebyshev responses

Filter type	Butterworth			Chebyshev		
Alphas	Theoretical value	Closest value	Digital world	Theoretical value	Closest value	Digital word
α_3	8.20	8.00	001000	1.83	1.83	100011
α_2	4.11	4.00	010000	6.30	6.40	001010
α_1	2.41	2.46	011010	1.09	1.08	111011
α_0	1.20	1.21	110101	1.37	1.36	101111
α_4	1.00	1.02	111111	1.00	1.02	111111

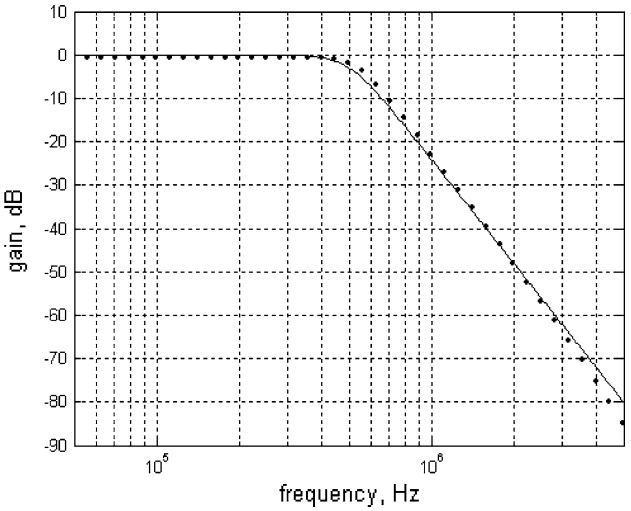

Fig. 9 Simulation results for fourth-order Butterworth lowpass filter

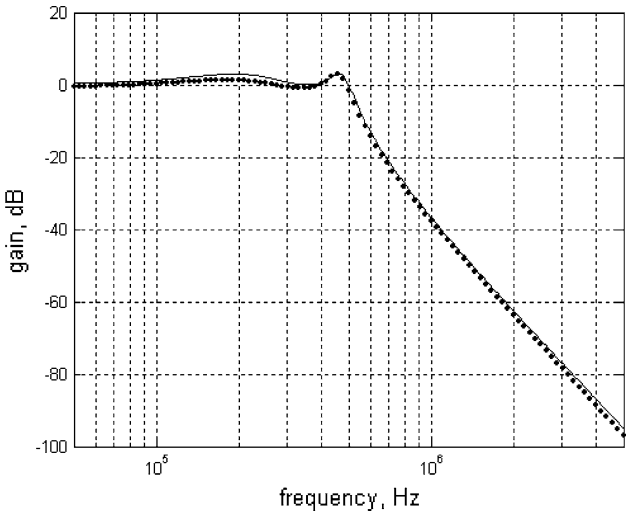

Fig. 10 Simulation results for fourth-order Chebchive lowpass filter after adjusting the filter coefficient digitally

First, the filter is designed to realize a fourth-order Butterworth response with passband frequency of 500 kHz. Then the coefficients will be digitally modified to change the response to Chebyshev response with same bandwidth. Assuming equal R's and C's such that RC product is 0.1 μs, Table 3 shows the required theoretical values of different alphas and the closest available digital word.

Simulation results of the two responses are given in Figs. 9 and 10. It is clear that the simulation results are in very good agreement with the presented theory.

7 Conclusion

This paper presents the design of high-order CM filters. The proposed *n*th-order filters are obtained using signal flow graph technique where simple active elements namely DCCAs and VBs are adopted. The first filter (Fig. 6) requires 'n + 3' DCCAs and 'n' BVs, but it either provides programmability to the numerator or the denominator coefficients. The second filter (Fig. 7) allows programmability of all coefficients. However, it requires 'n − 1' more DCCAs. Comparison with respective filters based on other CMBB shows that the proposed filter of Fig. 6, unlike the filter of [20], requires no additional circuitry to generate copies of the input signal. Also, the proposed filter of Fig. 7 requires less number of followers compared with its counterpart of [17].

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