A sub-1 Volt 10-bit supply boosted SAR ADC design in standard CMOS

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Abstract This paper presents a new very low-power, low-voltage successive approximation analog to digital converter (SAR ADC) design based on supply boosting technique. The supply boosting technique (SBT) and supply boosted (SB) circuits including level shifter, comparator, and supporting electronics are described. Supply boosting provides wide input common mode range and sub-1 Volt operation for the circuits designed in standard CMOS processes that have only high-V_t MOSFETs. A 10-bit supply boosted SAR ADC was designed and fabricated in a standard 0.5 μm, 5 V, 2P3M, CMOS process in which threshold voltages of NMOS and PMOS devices are +0.8 and −0.9 V, respectively. Fabricated SB-SAR ADC achieves effective number of bits (ENOB) of 8.04, power consumption of 147 nW with sampling rate of 1.0 KS/s on 1 Volt supply. Measured figure of merit (FOM) was 280 fJ/conversion-step. Proposed supply boosting technique improves input common mode range of both SB comparator and SAR ADC, allows sub-1 Volt operation when threshold voltages are in the order of the supply voltage, and achieves low energy operation. Thus, SBT is suitable for mixed-signal circuit designed for energy limited applications and systems in where supply voltage is in the order of threshold voltages of the process.

Keywords Supply boosting technique · Analog-digital converter · SAR · Low-power · Supply boosted comparator

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1 Introduction

Supply voltage and power consumption of mixed-signal circuits and systems in energy-limited applications such as self-powered wireless sensor networks, portable biosignal acquisition devices, and energy-harvesting systems are critical. Efficiency degradation due to the sub-threshold leakage current inherent in advanced sub-100 nm CMOS technologies has to be addressed if they are used in energy-limited applications [1]. Besides, threshold voltages have not been scaled as fast as the supply voltages in these advanced processes making analog design challenging in sub-1 Volt supply voltages while accommodating both low-power consumption and wide input range operation. Power consumption and input range are the critical design parameters for most analog to digital converters (ADCs) in sub-1 V applications. A possible solution might be to design sub-1 V analog/mixed-signal circuits by exploring new circuit design techniques while using low cost, mature, and relatively low leakage standard CMOS technologies (typically $L_{min} > 150$ nm). Few of them have been published including bootstrapping [2], charge pump based circuits [3–5], switched opamp technique [6], floating gate based circuits [7], and threshold modulation techniques [8, 9].

Low-leakage mature CMOS processes have their own drawbacks especially for sub-1 V supplies. Typically, the sum of threshold voltages of NMOS and PMOS devices in these processes are in the order of 1 V or more which makes analog design challenging. This is mainly due to the reduced overdrive voltages for active MOSFET transistors. Operating these devices in weak inversion region or using unique circuit design techniques are currently used to address overdrive issue with the expense of speed, complexity, and size.

In this paper, a new mixed-signal design technique called supply boosting is introduced. It is used for designing supply boosted successive approximation register (SBSAR) type analog-to-digital converter (ADC) and supply boosted comparator (SBC). Supply boosting technique and a unique low-energy supply boosted comparator are presented in Sect. 2. The SB comparator was used in a standard 10-bit SAR ADC topology and fabricated in a 0.5 μm/5 V CMOS process. Design of the supply boosted SAR ADC is presented in Sect. 3. Measurement results of the SBSAR ADC are presented in Sect. 4. Discussions and conclusion are given in Sect. 5.

2 Supply boosting technique (SBT) and circuits

In supply boosting technique (SBT), supply voltage is boosted locally when analog signal processing such as level shifting, amplification, or comparison is performed without compromising reliability margins of the process in use. SBT can be used if very low power analog signal processing operations are performed on continuous or discrete time signals. Source follower based level shifters, opamps, and comparators are good candidates for using SBT. In discrete time domain, SBT is well suited for designing clocked comparators due to the fact that the comparison of the input signals is performed in concurrent phases during which supply voltage has to be stable. Supply voltage does not continuously boosted in supply boosted (SB) circuits unlike continuous and discrete time circuits based on charge pump techniques (CPT) [3–5]. This allows simple supply boosting electronics and low energy consumption in SB circuits. Indeed, SBT provides the same benefits of CPT achieving improved input common mode range, increased operating speed and supply voltage range, and strong inversion region operation of all transistors. Major drawback of SBT is that the capacitor(s) used for supply boosting has to be large enough to provide adequate charge during signal processing. Trade off among booster capacitor size (or silicon footprint), speed and, power consumption exists. Complex boosting circuits may

also consume extra power reducing overall energy efficiency of SB circuits. Thus simple supply booting circuits is required. Another possible issue is related to device reliability due to using boosted supply voltages. This issue may not be as critical as it sounds if a larger feature size CMOS processes with higher voltage rating (i.e. 0.25 μm/ 2.5 V) is used while operating circuits in sub-1 Volt supply levels.

Major drive resulted in SBT was the need of a design technique resulting in low-power circuits that could work with sub-1 Volt supply voltages even though the threshold voltages of the MOSFET devices are in the order of supply voltage. This is critical for energy efficient self-powered systems (i.e. wireless sensor networks, implantable biomedical devices, and energy harvesting systems) that have low standby current and low power consumption, operate sub-1 Volt supply voltages, and cost effective.

### 2.1 Supply boosted level shifter (SBLS)

Level shifting is one of the major functions used by analog signal processing circuits. The supply boosted level shifter (SBLS) composes of a continuous time p-type source follower (SF) as shown in Fig. 1(a). Assuming SBLS has very low static current consumption; SBT could be used operating continuous SF in two distinctive phases; idle and signal processing. During idle phase, boosted supply voltage held at the input supply level ($V_{AAB} = V_{AA}$). During signal processing phase, it is boosted to approximately $2V_{AA}$. This way common mode input and output ranges of SF is expanded as depicted in Fig. 1(b) and (c) and given with the following equations.

$$\left.\begin{array}{l} \Delta V_{in} = V_{AA} - |V_{TH1}| - V_{dsat2} \\ \Delta V_{out} = G_{SBLS} \cdot \Delta V_{in} \end{array}\right\} \text{for } V_{AAB} = V_{AA} \quad (1)$$

$$\left.\begin{array}{l} \Delta V_{inx} = 2V_{AA} - |V_{TH1}| - V_{dsat2} \\ \Delta V_{outx} = G_{SBLS} \cdot \Delta V_{inx} \end{array}\right\} \text{for } V_{AAB} = 2V_{AA}$$

$$(2)$$

Here, G_{SBLS} is the small signal voltage gain of SF. Considering threshold voltage of PMOS transistor in modern

Fig. 1 Supply boosted level shifter (SBLS); (a) circuit diagram, (b) common mode input and output range for $V_{AAB} = V_{AA}$, (c) for $V_{AAB} = 2 V_{AA}$
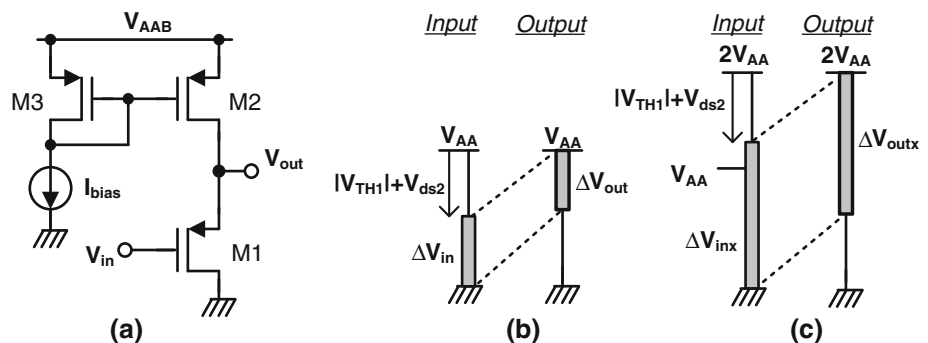
submicron CMOS processes is between −0.4 and −0.7 V, input common mode range of the level shifter could be improved by using SBT from 0.6 to 1.5 V and from 0.2 to 1.2 V, respectively. Thus, achieving rail-to-rail input range for 1 V supply voltage for 0.1 V of V_{dsat2}. Output range is limited by the gain of source follower and by the threshold voltage of the input transistor, M1. Bulk node of the M1 could be connected to the output to attain nominal threshold voltage. The SBT improves output range from 0.16 to 0.96 V for G_{SBLS} of 0.8 V/V. Thus, rail-to-rail input common mode range could be achieved without considering complementary input stages or other type of input expansion techniques [10, 11] if SBLS circuit is used as input stage of analog signal processing circuit such as opamps and comparators.

3 Supply boosted comparator (SBC)

Supply boosted comparator (SBC) core composes of two cascaded, continuous time, n-type differential pairs with clocked and cross-coupled loads as latches as shown on Fig. 2. First latched comparator (SBLC) utilizes supply boosting technique. Second latched comparator (LC) is a regular one receiving input supply voltage (V_{AA}). LC was used for improving resolution and gain of the comparator, and restores the output logic level. Clock signal (BCLK) used by both comparators is boosted to turn reset switches (M5, M6) on and off properly. The SBC works in two phases like regular latched comparators [12, 13]: reset and compare. During reset phase output nodes are connected to supply rail through transistors M5 and M6 by driving the boosted clock signal to ground (BCLK = 0). In compare phase, they are turned off by using boosted clock signal (BCLK = V_{AAB}) allowing input voltages to determine which branch of the differential pair to get larger portion of the tail current through positive feedback. Since the differential pairs are

continuously biased, a static current is consumed both in reset and in compare phases. They were biased in nA levels so that static power consumption is low. Low current biasing also allows supply boosting to be used with higher efficiency. Small signal differential voltage gain of the comparator during comparison phase is approximately given with Eq. 3 [14].

$$G_{comp} = \frac{-g_{m1}r_{o1}r_{o3}}{r_{o1} + r_{o3} - g_{m3}r_{o1}r_{o3}} \qquad (3)$$

where g_{m1} and g_{m3} are the transconductance of input and load transistors M1 and M3, respectively. High gain can be achieved assuring the denominator of Eq. 3 as small as possible while considering regeneration time constant which is inversely proportional to the g_{m3} [14].

## 3.1 Supply and clock booster (SCB)

The supply boosted comparator core and level shifter require two boosted signals. Clock signal (BCLK) to the SBC core seen on Fig. 2 has to be boosted during compare period to about $2V_{AA}$ and connected to ground during reset period. If level shifter is used as first stage driving the inputs of SBC core, than V_{AAB} voltage has to be boosted to $2V_{AA}$ during compare period and connected to V_{AA} during reset. These signals are generated by the supply and clock booster (SCB) circuit as shown in Fig. 3 [15].

SCB composes of two inverters (A, B), three transistors and a boosting capacitor (C). It generates boosted clock (BCLK) and supply (V_{AAB}) voltages. Bulk nodes of the PMOS transistors (M2, M3) are connected to boosted supply (V_{AAB}) bus for improving efficiency of the booster. Also inverter B has to be designed stronger than inverter A to derive larger parasitic load. It is because the bottom plate of boosting capacitor, C, is connected on inverter B side to achieve better boosting efficiency. Node voltages of the SCB block during reset and compare periods are shown in Fig. 3(b). Boosted supply level is given with Eq. 4.

Fig. 2 Circuit diagram of the supply boosted comparator core
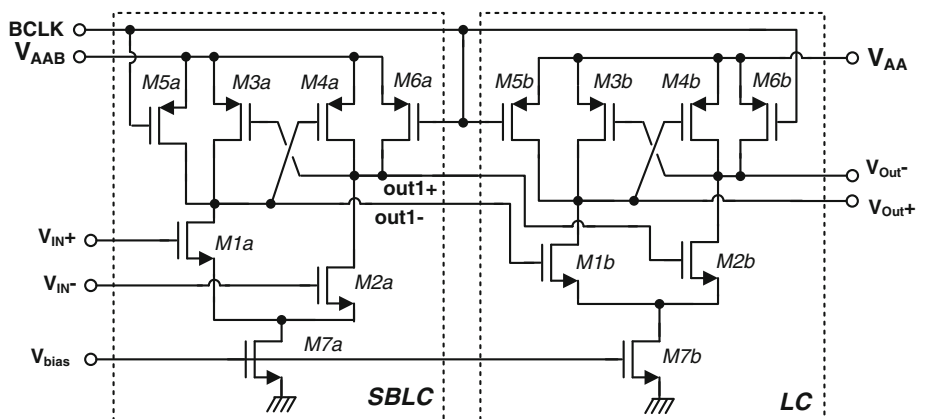
Fig. 3 Supply and clock booster (SCB): (a) circuit diagram, (b) node voltages
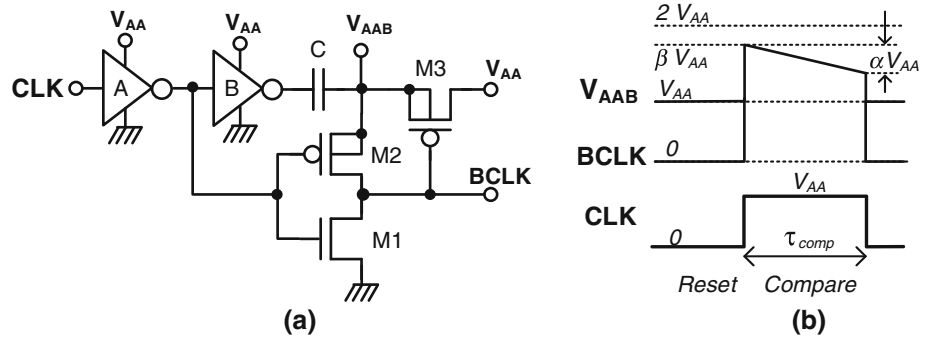
$$V_{AAB} = \left(\frac{2 \cdot C + C_L}{C + C_L} - \alpha \right) \cdot V_{AA} = \beta \cdot V_{AA} \qquad (4)$$

Here, α is the discharge ratio in percent V_{AA} observed on V_{AAB} and BCLK during compare period due to DC load current (I_L). β is the boosting factor. Boosting capacitor value (C) is related to the DC load current drained, discharge ratio, and compare time period (τ_{comp}) and it is given with (5).

$$C = \frac{\tau_{comp} \cdot I_L}{\alpha \cdot V_{AA}} \qquad (5)$$

For load capacitor being 10% of the boosting one, discharge ratio of 10%, comparison time of 0.1 μs, and load current of 1 μA necessitates boosting capacitor value of 1 pF resulting in boosting factor of 1.81× and charge pump efficiency of about 90%.
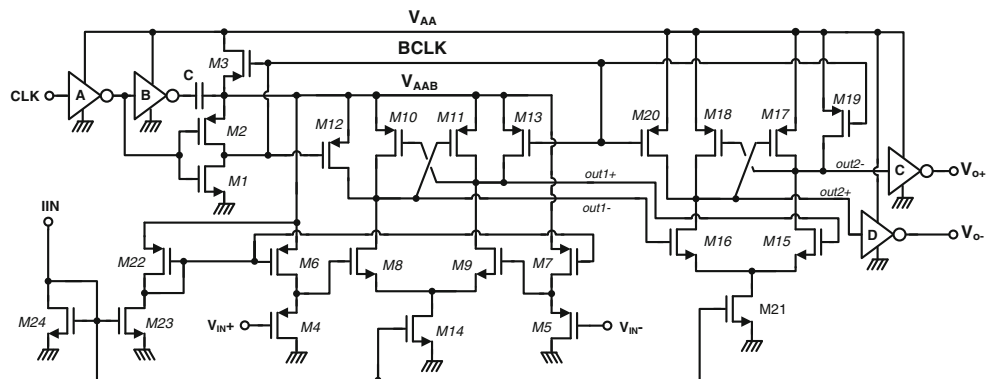
3.2 Supply boosted comparator (SBC) design

Complete circuit diagram of supply boosted comparator (SBC) is shown in Fig. 4 including bias network. The SCB provides boosted clock and supply voltages for SBC. M4–M7 form SBLS. M8–M14 form the SBLC while second stage LC made up of M15–M21. Reset switches (M12–13, M19–20) are driven by boosted clock signal BCLK. SBLS and its bias network and SBLC receive boosted supply voltage (V_{AAB}) while SCB inverters and LC use input supply voltage (V_{AA}). Outputs of the LC are buffered by

two digital inverters with high switching point. Transistors M22–M24 delivers the bias currents to the SBC. Boosted supply level V_{AAB} was used on the bias branch (M22–23) making sure that the reference current for the SPLS is stabilized and constant during comparison phase. Transistors in SPLS and first comparator were kept in strong inversion region during comparison phase as a result of the supply boosting.

The SBC was designed to have high open loop gain and wide input range to achieve 10-bit resolution for sub-1 V supply. Threshold voltages of MOSFETs in selected CMOS process allows only 0.3 and 0.1 V common mode input ranges for 1.2 and 1.0 V supply voltages if conventional clocked comparator topology with p-type differential input pair is used. Maximum input ranges for these supply voltages would be rail-to-rail and 0.7 V for 1.2 V and 1.0 V supply voltages assuming boosting factor of 1.6× for SCB. Minimum supply voltage was as low as 0.8 V assuming boosting factor of 1.6× and SBLS gain of 0.8 V/V. The SBC design was simulated using bias currents of as low as 10 nA for SBLS and 20 nA for each latched comparators resulting in less than 100 μs comparator delay. A 20 pF booster capacitor was used based on maximum static current consumption of less than 500 nA and comparator delay time of 10 μs for 1.0 V supply. Parasitic load capacitance of the charge pump circuit estimated to be around 4 pF resulting in boosting factor of 1.6×. Device sizes used in the SBC design were listed in Table 1. Long

Fig. 4 Circuit diagram of the supply boosted comparator (SBC)

Table 1 Device sized used for the supply boosted comparator (SBC)

Transistors (M#)	Width (μm)	Length (μm)	M
1,2,3	6.0	0.6	4
4,5,10,11,17,18	6.0	1.2	8
6,7,22,23	6.0	3.0	2
8,9,15,16	6.0	1.5	8
12,13,19,20	6.0	0.6	1
14,21,24	6.0	3.0	4
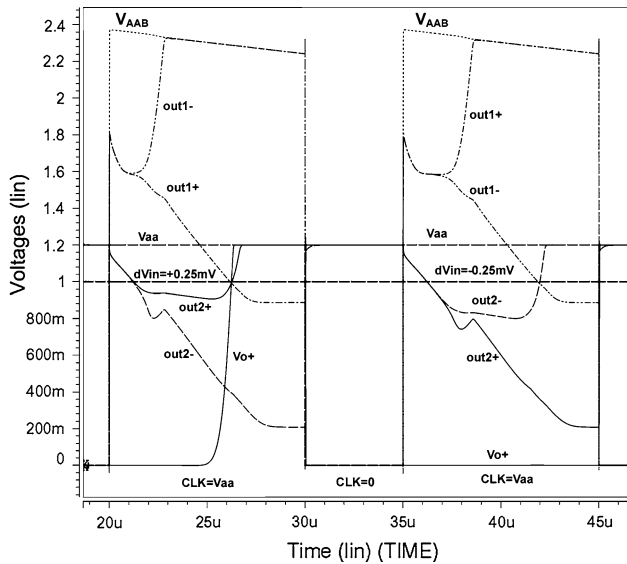
Fig. 5 Hspice simulation result of the SBC for $V_{AA} = 1.2V$, $V_{IN,DC} = 1.0$ V, $dV_{IN} = \pm0.25$ mV

channel lengths were used to reduce input refereed offset voltage, increase gain, and improve matching.

Operation of proposed comparator was verified through Spice simulation at different process, supply voltage and temperature (PVT) corners. An HSpice simulation result for 1.2 V supply, 1.0 V common mode input, and ±0.25 mV delta input voltage is shown in Fig. 5. Better than 10-bit resolution was verified at PVT corners for 0.5 μm CMOS process (C5 from MOSIS).

4 Supply boosted SAR ADC design

A sub-1 V, 10-bit, shift-register based standard SAR ADC [16] and supporting circuits were designed using supply boosting technique (SBT). Circuit diagram of the supply boosted (SB) SAR ADC is shown in Fig. 6. It composes of low-voltage optimized successive approximation register logic (SARL) blocks, dynamic shift registers (DSR), on-chip programmable bias generator (not shown), supply boosted comparator (SBC), clock phase generators, boosting buffers (BBF), CMOS switches (CSW), and a 10 bit charge-redistribution binary DAC. Each SARL contains one DSR while implementing SAR ADC algorithm. DSR in SARL holds the conversion bit. Circuit diagrams of the SARL and DSR are shown in Fig. 8(a) and (b), respectively. Binary weighted poly1-poly2 capacitors were used in the DAC. No offset compensation or error correction methods or optimized capacitor layout techniques were used in the design [17, 18].

Two reference voltages were generated off chip to set input low level (V_{REF_LO}) and full scale input range (V_{FS}) of the ADC. A low-noise off chip track-and-hold circuit was used for driving analog input (V_{INPUT}). Clock signal is alternated between DSR and SARL using RST signal as shown on timing diagram (Fig. 7.). Conversion took place when RST is low in $(n + 1)$ clock cycles. Digital bits are shifted out by SARL blocks when RST signal is asserted high. Total $2(n + 1)$ clock cycles are required for each conversion in proposed architecture if serial data output (S_{DATA}) mode is used. Parallel outputs of SARLs could also
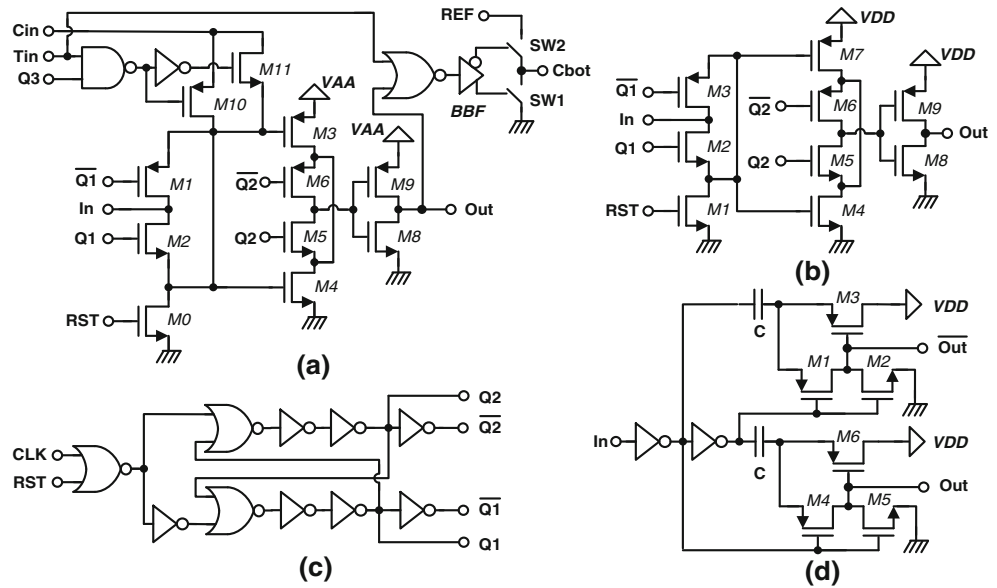

Fig. 6 Circuit diagram of the 10-bit supply boosted SAR ADC
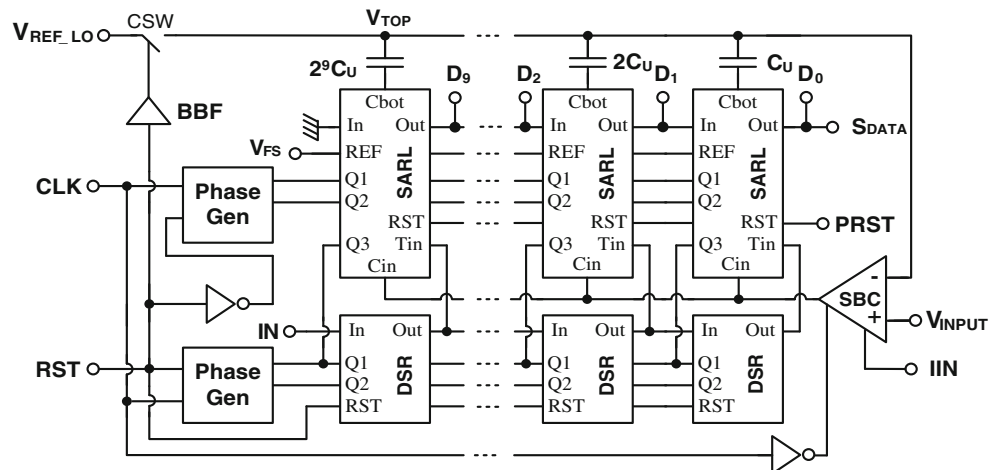
**Fig. 7** Timing diagram of the 10-bit supply boosted SAR ADC
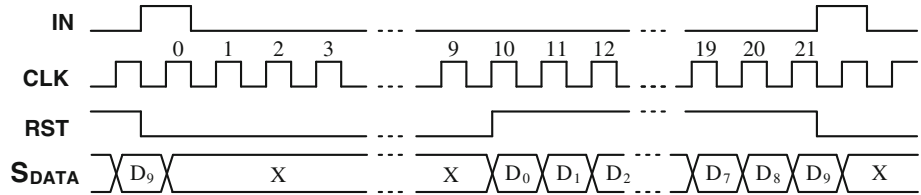
Fig. 8 Circuit blocks of SB-SAR ADC: (**a**) low-voltage SAR logic (SARL), (**b**) dynamic shift register (DSR), (**c**) non-overlapping clock generator, (**d**) boosting buffer (BBF) for clock signals

be used reducing conversion time to $(n + 1)$ clock cycles. Conversion speed can be increased by shifting out ADC bits faster in series mode. SAR ADC algorithm was implemented in SARL blocks with the help of dynamic shift registers (DSR), and associated control circuits such as non-overlapping clock generators and boosting buffers (BBF) as show on Fig. 8 (c) and (d), respectively. BBF boosts the clock signals for the CMOS switches (CSW) in the design. BBF is the modified version of the SCB generating both inverted and non-inverted version of its input. 100 fF boosting capacitor was used in BBF. Size of transistors M1–M6 in BBF was 3 μm/0.6 μm. CMOS switches were uses in design (SW1-2, CSW). Unit capacitor size (C_u) used in binary weighted DAC was 40 fF. HSpice simulation of the design is shown on Fig. 9 for 1.2 V supply, 0.75 V input range, and 10 KS/s conversion speed. In this simulation, clock frequencies for SARL and DSR were 100 and 500 kHz respectively achieving close to 10 KS/s ADC speed. No layout parasitics were included in this simulation.

5 Measurement results

The proposed supply boosted SAR ADC was fabricated in a standard 2P3M 0.5 μm CMOS process (C5 from MOSIS). The reason this process was chosen is that the
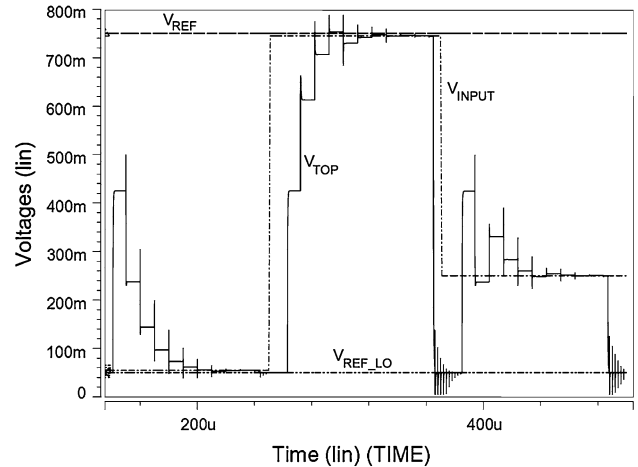
Fig. 9 Simulation result of SB-SAR ADC for $V_{AA} = 1.2$ V, $V_{REF\_LO} = 50$ mV, $V_{REF} = 750$ mV

MOSFET transistors in this process have had relatively high threshold voltages (+0.8 V for NMOS and −0.9 V for PMOS) making sub-1 V analog and mixed-signal designs challenging. Microphotograph of the fabricated 10-bit supply boosted SAR ADC is shown in Fig. 10. Layout size of the design was 950 μm × 260 μm or 0.25 mm². Supply boosted comparator (SBC) occupies almost 25% of the SB-SAR ADC. The boosting capacitor occupies more than 50% of SBC layout. It was 20 pF.
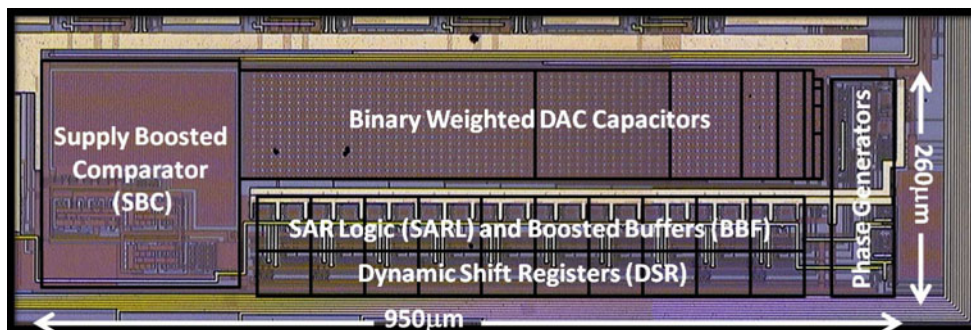
Fig. 10 Microphotograph of the 10-bit supply boosted SAR ADC

All measurements were performed at 1 V supply. Total measured supply current was 147 nA. Static current consumption of the SBC was about 110 nA, while rest was dynamic power consumed by supporting electronics. Two clock frequencies were used during conversion and shift out periods resulting in the conversion rate of 1.0 KS/s. ADC power supply was separated from rest of the chip. Thus, measured power consumption does not include power consumed by peripheral electronics and pads driving instrumentation equipment.

Figure 11 shows measured integral nonlinearity (INL) and differential nonlinearity (DNL) errors of the design at 1 KS/s. The major error occurred at half full scale code of 512. This is mainly due to the routing and layout design of the capacitor bank which was not optimized for matching. Thus the performance is suffered resulting in −0.6/+0.9 LSB DNL and −2.7/+1.1 LSB INL. Figure 12 shows full-scale, 34 Hz sine-wave input spectrum measured at 1 V supply with sampling rate of 1 KS/s. 16384 data point was collected for fast fourier transform (FFT) spectrum analysis. The spurious free dynamic range (SFDR) as approximately 62 dB and effective number of bit (ENOB) was 8.04. Total harmonic distortion (THD) including first 10 harmonics was 58.6 dB. Effect of supply boosting could be observed on the harmonics of the output spectrum. Energy efficiency of the supply boosted SAR ADC was determined by using the figure-of-merit (FOM) defined in [19]. 280 fJ/conv.-step was achieved by proposed SB SAR ADC. This FOM shows that supply boosting technique does not degrade the energy efficiency of circuits. We have to also note that this FOM is achieved without doing any circuit or architectural improvement on standard SAR ADC topology chosen, and unlike the recently reported SAR ADCs [17–24] a mature 0.5 μm CMOS technology with high-Vt devices was used.

Further measurements were performed to check the limit of supply voltage and conversion speed of the SB SAR ADC. It was found that the ADC works down to 0.85 V supply voltage. We did not be able to test the design below this supply level due to the limitations of our test system.
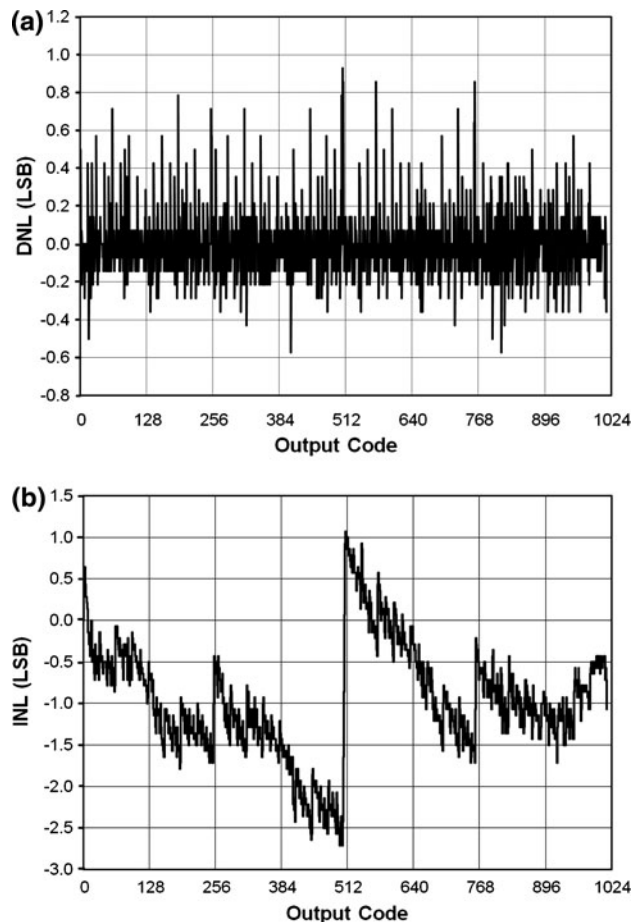
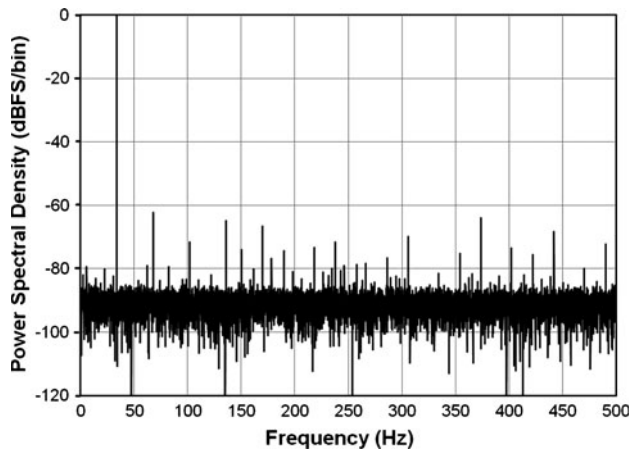**Fig. 11** Measured static characteristics of the SB-SAR ADC. **a** Differential nonlinearity (DNL), (**b**) integral nonlinearity (INL)

At 1.2 V supply 1.2 KS/s conversion speed with 320 pJ/conv.-step was achieved. Measurement result at 1 V supply is reported on Table 2.

6 Conclusion

A low-voltage design technique called supply boosting technique (SBT) is proposed to design very-low voltage

Fig. 12 Measured dynamic characteristics of the SB-SAR ADC. FFT spectrum with 34 Hz input tone (V_{AA} = 1.0 V, f_{clk} = 10 kHz, f_{conv} = 1KS/s)

Table 2 Measured characteristics of the supply boosted SAR ADC

Resolution	10-bit
Technology	0.5 μm CMOS
Supply voltage range	0.85–1.2 Volt
Input range	0.63 Volt
Supply voltage	1.0 Volt
Conversion speed	1.0 KS/s.
Differential nonlinearity (DNL)	+0.9 LSB/−0.6 LSB
Integral nonlinearity (INL)	+1.1 LSB/−2.7 LSB
ENOB (34 Hz input @ 1 V supply)	8.04 bits
THD	58.6 dB
SNDR (34 Hz input @ 1 V supply)	50.1 dB
SFDR (34 Hz input @ 1 V supply)	62.3 dB
Power consumption @1 V and 1KS/s	147 nW
Figure of merit (FoM)	0.28 pJ/conv.-step
Layout area	0.25 mm^2

analog/mixed-signal CMOS circuits in standard CMOS processes in where only high-V_t devices exist or supply voltage is in the order of the threshold voltages or below. One such process was chosen to implement supply boosted circuits and to realize 10-bit supply boosted SAR ADC. Other low voltage design techniques such as clock boosting were also used in conjunction with the supply boosting to address overdrive voltage issue of CMOS switches. A unique supply boosted comparator (SBC) was designed. Input common mode range of SBC was extended by using supply boosted level shifter (SBLS) circuit. Designed SBC was used as an integral part of a standard shift-register based SAR ADC architecture. Proposed supply boosted SAR ADC was fabricated in a mature, low cost 0.5 μm CMOS process which has high-V_t transistors.

It was observed from measurements that supply boosting does not degrade energy efficiency of the circuits as long as very low currents are drained from the boosted supply. Despite none of the circuits were optimized for speed, matching, or power efficiency, very low FOM of 280 fJ/conv.-step was attained. Comparing with recently published SAR ADC designs [20–24] supply boosted SAR ADC achieves; smallest layout footprint, lowest power consumption, and reasonable FOM as shown on the Table 3. Normalized areas of the designs were determined by dividing the reported design areas with the minimum gate area (1.5 * L_{min}^2) of the process in use and normalized further with the minimum one which is our design. CMOS processes (0.18 μm CMOS) used in published works had devices with thresholds voltage between 0.4 and 0.5 V [20, 23], as oppose to 0.8 and 0.9 V in this work, making their design suitable sub-1 V supply operation. Reported designs have rail-to-rail input ranges, because they use complementary differential pairs or fully differential input stages. The proposed SB-SAR ADC uses compact PMOS type SBLS resulting in smaller layout size, yet less than full

Table 3 Comparison of supply boosted SAR ADC with published works

	JSSC'07 [20]	JSSC'07 [21]	ISSCC'08 [22]	VLSI'09 [23]	ISCAS'09 [24]	This work
Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.50 μm
Supply voltage	1.0	1.0	1.0	0.6	1.0	1.0
Power dissipation (μW)	6.15	25.00	3.80	1.30	0.95	0.15
ENOB	7.44	10.55	9.4	8.7	7.2	8.04
Sampling rate (KS/s)	400	100	100	100	10	1
INL (LSB)	−0.5/+0.6	−0.16/+0.19	−0.8/+0.8	−0.5/+0.5	−0.89/0.6	−2.7/+1.1
DNL (LSB)	−0.9/+0.1	−0.14/+0.16	−0.6/+0.4	−0.5/+0.1	−0.41/+0.38	−0.6/+0.9
FoM (fJ/conv.-step)	60	165	56	31	3230	280
Input range (V)	1.00	1.00	0.80	0.60	1.00	0.63
Area (mm2)	0.7	0.65	0.24	0.125	0.12	0.25
Area (normalized)	31.1	28.9	10.7	5.6	5.3	1.0

scale input range. However, SBT improves the input range more than six times (6×) achieving 0.63 V input range.

The experiment results demonstrate that very low voltage (<0.5 V) and low power (<100 nW) mixed-signal circuit and systems could be designed using supply boosting technique (SBT) for low speed applications such as self-powered energy harvesting systems, portable bio-signal acquisition devices, and autonomous wireless sensor networks without requiring expensive CMOS processes. Also, proposed SB SAR ADC topology showed a potential for power and hardware efficient analog to digital conversion with room for performance improvement.

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