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Symbolic analysis of analog circuits containing voltage mirrors and current mirrors

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Abstract The pathological elements voltage mirror (VM) and current mirror (CM) have shown advantages in analog behavioral modeling and circuit synthesis, where many nullor-mirror equivalences have been explored to design and to transform voltage-mode circuits to current-mode ones and viceversa. However, both the VM and CM have not equivalents to perform automatic symbolic circuit analysis. In this manner, we introduce nullor-equivalents for these pathological elements allowing to include parasitics and to perform only symbolic nodal analysis. The nullor-equivalent of the CM is extended to provide multiple-outpus (MO-CM). Finally, two active filters containing VMs, CMs and MO-CMs are analysed to show the usefulness of the models.

Keywords Nullor · Voltage mirror · Current mirror · Symbolic analysis · Nodal analysis · Active filter

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1 Introduction

The nullator and norator elements are quite useful in analog design automation (ADA). For instance, the ideal behavior of the voltage follower (VF) can be modeled using nullators, with the aim to synthesize different VF topologies. Further, the VF can be evolved to synthesize the voltage mirror (VM) [35]. The norator is useful to model the behavior of the current follower (CF), and it can be superimposed with the VF to design more complex devices, e.g. current conveyors [38].

The VF, VM, CF and the current mirror (CM) form the four unity-gain cells (UGCs) [34]. Among them, the CM could be the most useful cell covering a wide range of applications [9, 13, 31, 33, 43], and also it can provide multiple-outputs (MO-CM). The four UGCs can be combined to model the behavior of already known and new active devices [3]. For example, the inverting properties of the VM and CM leads us to design inverting and positive-type current conveyors [1, 25, 26, 27], which properties can improve the ones provided by the four terminal floating nullor (FTFN) [12].

In symbolic analysis of analog and VLSI circuits, several methods are described in [7, 17]. In particular, the nullator and the norator are quite useful to perform symbolic analysis by only applying nodal analysis (NA) [11, 22, 39]. Besides, the symbolic NA method requires that all active devices be modeled using nullors [14, 22, 39].

The modeling of active devices possessing inverting characteristics can be done by using the VM and CM, as pathological elements [2, 20, 30, 42]. An important thing is that an analog circuit containing VMs and CMs also allows to transform circuit topologies or voltage-mode to current-mode circuits and vice-versa [5, 8, 10, 15, 28, 29, 41]. However, both the VM and CM can not be used in

symbolic NA because their inverting characteristics imposse addition/subtraction limitations in the formulation process, i.e. there is not way to perform addition or deletion of columns or rows to preserve the inverting characteristics of either or both the VM and CM, as it is done in a nullor network [37]. In this manner, we are introducing nullor-equivalents for the VM, CM and MO-CM to take advantage of the symbolic NA of nullor networks [7, 37, 39].

2 Symbolic NA method

As already shown in [22, 37, 39], the main advantage of transforming an analog circuit to a nullor network is to apply only NA in the formulation process, and to obtain a reduced system of equations for operational amplifier based circuits [7, 37], and in general for circuits containing non-NA compatible elements.

The first step of the NA-formulation consists to model all circuit elements, such as: active devices, controlled sources and independent voltage sources using nullors [5, 14, 39]. The modeling process must include grounded admittances as much as possible, because they have only one entry in the NA formulation [37], while floating ones may have up to four entries requiring more computational work. The symbolic NA formulation method ($i = Yv$) can be summarized as follows:

1. Step 1: Describe the interconnection relationships of norators P_j, nullators O_j, and admittances by generating tables including names and nodes (m, n).
2. Step 2: Calculate the indexes associated to set row and set column, and group grounded and floating admittances:
   (a) ROW: Contains all nodes ordered by applying the norator property which nodes (m, n) are virtually short-circuited. These indexes are used to fill vector i and the admittance matrix Y.
   (b) COL: Contains all nodes ordered by applying the nullator property which nodes (m, n) are virtually short-circuited. These indexes are used to fill vector v and the admittance matrix Y.
   (c) Admittances: They are grouped into two tables: Table A includes all nodes (ordered), and in each node is the sum of all admittances connected to it. Table B includes all floating admittances and its nodes (m, n).
3. Step 3: Use sets ROW and COL to fill vectors i and v, respectively. To fill Y: if in Table A a node is included in ROW and COL, introduce that admittance(s) in Y at position (ROW index, COL index). For each admittance in Table B, search node m in ROW and n in COL (do the same but search n in ROW and m in COL), if both nodes exist the admittance is introduced in Y at position (ROW index, COL index), and it is negative.

The solution of the formulation can be obtained by boolean logic operations [32], or by determinant decision diagrams [23, 40]. Elsewhere, we can formulate a much reduced system of equations in a nullor network, because it also allows us to apply circuit reduction methods [6, 16, 21, 24].

3 VM and CM nullor-equivalents

The pathological elements VM and CM are shown in Fig. 1 [2]. These representations are useful in circuit modeling [2, 20, 30, 42], circuit transformation [28, 29, 41], and circuit synthesis [18, 19]. However, these representations do not allow to include parasitics and they can not be used within the symbolic NA method, because their inverting characteristics do not allow to perform operations as it is done for networks containing nullators and norators [7, 22, 37, 39]. In this manner, we introduce nullor-equivalents for the VM, CM and MO-CM to solve these problems.

3.1 Nullor-equivalent of the VM

Among all the possible combinations to generate the nullor-equivalent of the VM, we propose to use the one shown in Fig. 2. In this description Z_{in} and Z_{out} are connected in parallel to the input-port and in series to the output-port, respectively, and they model the input and output parasitics. The resistor of value $1/A_v$ is very useful in the NA formulation because the admittance becomes A_v, and it models the gain or tracking error of the VM. In the ideal case, $Z_{in} = \infty$, $Z_{out} = 0$, and $A_v =$ unity.

From Fig. 2, $v_1 = v_{in}$, and since the voltage across a nullator is zero, $v_2 = v_1 = v_{in}$. Because the current through a nullator is zero, v_2 generates a loop-current through nodes 2, 3 and ground. That way, $i_a = \frac{v_2}{1/A_v} = A_v v_{in}$ and $i_b = i_a = A_v v_{in}$. Now $v_3 = -1 \times i_b$ and $v_4 = v_3 =$

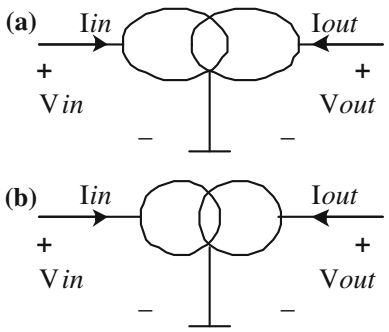

Fig. 1 Representations of **a** VM and **b** CM

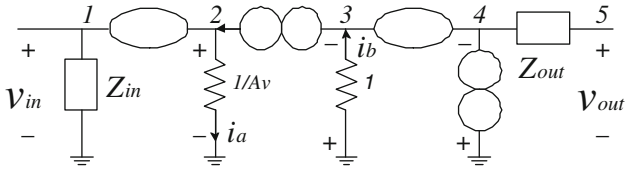

Fig. 2 Nullor-equivalent of the VM including gain, input and output impedances

$-A_v v_{in}$. Finally, we obtain (1). In an ideal VM $v_{out} = -v_{in}$.

$$v_{out}|_{open-circuit} = -A_v v_{in} \tag{1}$$

3.2 Nullor-equivalent of the CM

Among all the possible combinations to generate the nullor-equivalent of the CM, we propose to use the one shown in Fig. 3. Indeed, by applying the adjoint network theorem to transform a voltage-mode circuit to a current-mode one [5, 8, 10, 15, 28, 29, 41], this topology is really the adjoint of the VM shown in Fig. 2. In this representation Z_{in} and Z_{out} are connected in serie to the input-port and in parallel to the output-port, respectively, and they model the input and output parasitics. Again, the resistor of value $1/A_i$ is very useful in the NA formulation because the admittance becomes A_i, and it models the gain or tracking error of the CM. In the ideal case, $Z_{in} = 0$, $Z_{out} = \infty$, and A_i = unity.

From Fig. 3, the nullator connected at node 2 does not allow current to flow, so that a loop-current is formed through nodes 1, 2, 3 and ground. In this manner $i_a = i_{in}$, and $v_3 = 1 \times i_a = i_{in}$. The voltage across the nullator is zero so that $v_4 = v_3 = i_{in}$, this generates $i_b = \frac{v_4}{1/A_i} = A_i i_{in}$. By applying Kirchhoff's current law: $i_{out} = -(i_b + i_{Zout})$. Finally, we obtain (2). In an ideal CM $i_{out} = -i_{in}$.

$$i_{out}|_{short-circuit} = -A_i i_{in} \tag{2}$$

3.3 Nullor-equivalent of the MO-CM

An extention of Fig. 3, leads us to generate the nullor-equivalent of the MO-CM, as shown in Fig. 4. In this representation we are allowed to include independent gain and output impedance for each output n.

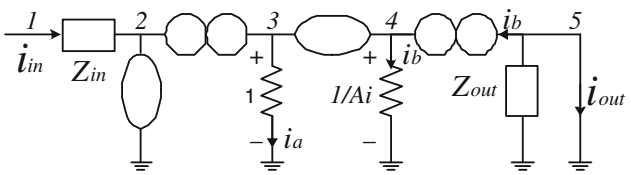

Fig. 3 Nullor-equivalent of the CM including gain, input and output impedances

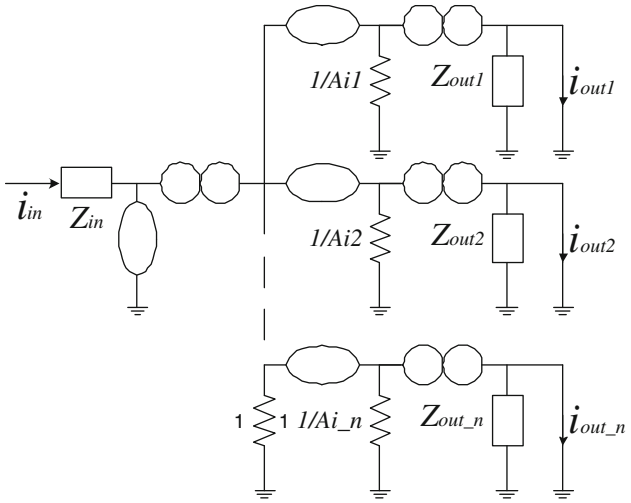

Fig. 4 Nullor-equivalent of the MO-CM including input impedance and independent gain and output impedance for each output (n)

4 Symbolic analysis of analog circuits containing VMs, CMs and/or MO-CMs

The nullor-equivalents of the VM, CM and MO-CMs can be used directly in symbolic NA of analog circuits, where the output of the VM is not connected to the input of the CM or MO-CM. Furthermore, when the circuit to be analysed contains a VM which output is connected to a norator or the input of a CM or MO-CM, we need to apply the superimposing method given in [38], to generate a nullor network containing the same number of nullators and norators, in order to apply the symbolic NA formulation.

Let's us consider the non-inverting and inverting low-pass filter using an inverting positive-type second generation current conveyor (ICCII+) [27]: Its representation using the VM and CM is shown in Fig. 5. As one sees, the output of the VM is connected to the input of the CM. By applying the superimposing method from [38], we obtain the nullor-equivalent network shown in Fig. 6. Basically, the impedance, nullator and norator connected at node 4 in Fig. 2, are superimposed with the impedance, nullator and norator connected at node 2 in Fig. 3. Other nullor-equivalents of inverting and non-inverting current conveyors can be found in [39], which also include parasitic impedances.

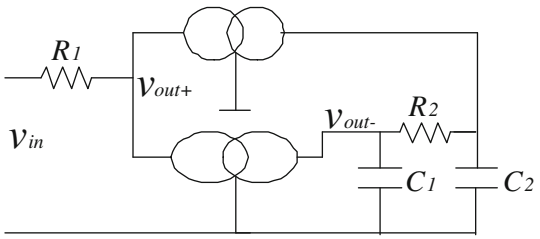

Fig. 5 Non-inverting and inverting low-pass filter taken from [27]

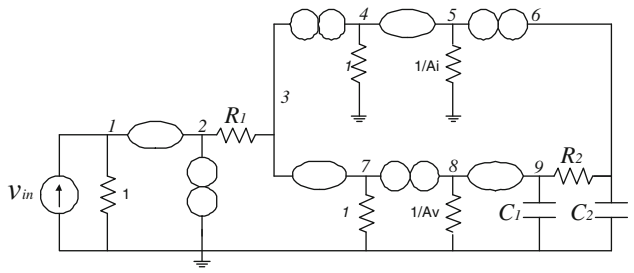

Fig. 6 Nullor-equivalent of Fig. 5

Were we applying the modified nodal analysis (MNA) formulation to Fig. 6, the system of equations becomes order 6, because we need to introduce two stamps: one for the VM with a voltage-controlled voltage source and other for the independent voltage source. On the other hand, by applying the symbolic NA formulation, the order is reduced to 5, because the independent voltage source has been transformed to a current source [37], and the order becomes to be the number of nodes minus the number of nullator-norator pairs [7]. As a result, for large networks containing many VMs, the symbolic NA formulation is better than by applying the MNA method. For instance, by performing the NA formulation from Fig. 6, the following sets are obtained:

$$ROW = \{(1), (3,4), (5,6), (7,8), (9)\}$$
$$COL = \{(1,2), (3,7), (4,5), (6), (8,9)\}$$

The summation of the admittances at each node is presented in Table 1, while the floating admittances are given in Table 2. The NA formulation is given by (3).

$$\begin{bmatrix} v_{in} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -G_1 & G_1 & 1 & 0 & 0 \\ 0 & 0 & A_i & G_2 + sC_2 & -G_2 \\ 0 & 1 & 0 & 0 & A_v \\ 0 & 0 & 0 & -G_2 & G_2 + sC_1 \end{bmatrix} \begin{bmatrix} v_{1,2} \\ v_{3,7} \\ v_{4,5} \\ v_6 \\ v_{8,9} \end{bmatrix} \quad (3)$$

Table 1 Admittances at each node

Node	Admittances
1	1
2	G1
3	G1
4	1
5	Ai
6	G2+sC2
7	1
8	Av
9	G2+sC1

Table 2 Floating admittances

Nodes	Admittance
(2,3)	G1
(9,6)	G2

The solution of this system taken node 9 as the inverting-output is given by (4). However, in the ideal case $A_v = A_i$=1, and then (4) is reduced to the symbolic transfer function already provided in (5) [27].

$$v_9 = -\frac{A_i v_{in}}{A_v A_i + sR_1C_1 + sR_1C_2 + s^2R_1C_1R_2C_2} \quad (4)$$

$$H(s) = -\frac{1}{1 + sR_1(C_1 + C_2) + s^2R_1C_1R_2C_2} \quad (5)$$

From this example, we can conclude on the usefulness of the proposed nullor-equivalents to perform symbolic NA which can be very suitable to enhance the synthesis procedures already introduced in [4, 18, 19, 34, 36].

A second example is provided herein by analyzing a universal biquadratic filter using only dual-output CMs and grounded capacitors, it is taken from [33]. Its nullor-equivalent is shown in Fig. 7. More complex active filters based on CM arrays can be found in [31].

From the integrated circuit (IC) design point of view, a CM can provide multiple-outputs (MO-CM), but all of them with the same sign. Besides, when an output with an opposite sign is needed, another CM must be connected, as it is done in this example.

In this manner, the representation in Fig. 7 shows two dual-ouput CMs (DO-CM) labeled by letters a and c, they include the input resistance R_{ina} and R_{inc}, their gains A_{a1}, A_{a2} and A_{c1}, A_{c2}, and their output resistances R_{oa1}, R_{oa2} and R_{oc1}, R_{oc2}.

To invert the sign in one output of the DO-CMs, two CMs are also included labeled by letters b and d, they include the input resistance R_{inb} and R_{ind}, their gains A_b, A_d, and their output resistances R_{ob}, R_{od}.

By applying the symbolic NA method, the formulation generates a system of order 9 (19 nodes minus 10 nullors) [7, 22, 37]. The sets for the rows and cols become:

$$ROW = \{(1, 11, 19), (2, 14), (3, 6), (4, 5), (7, 8), (9, 10), (12, 13), (15, 16), (17, 18)\}$$
$$COL = \{(1), (2), (3), (5, 6, 7), (8), (10, 11), (13, 14, 15), (16), (18, 19)\}$$

The four floating resistances are associated to the input-resistance of the CMs, there are six gains and six output-resistances.

The exact symbolic expression has many symbolic product-of-terms. However, when the output-resistances equal to ∞, the reduced symbolic expression is given by

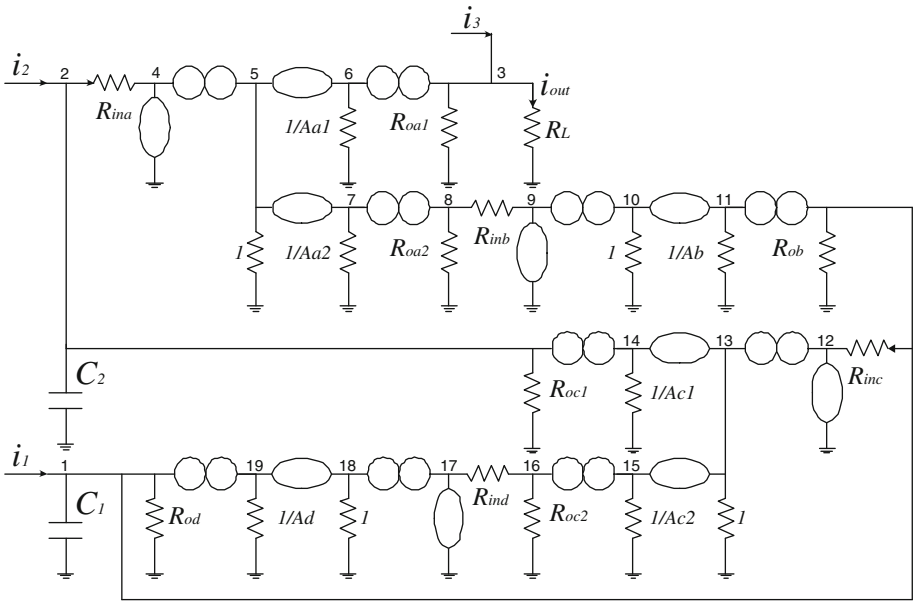

Fig. 7 Nullor-equivalent of the current-mode filter taken from [33]

(6). As one sees, only the input resistances R_{ina} and R_{inc} are included in the reduced symbolic expression, as already shown in [33]. When the gains are set to unity, (6) becomes (7).

$$I_{out} = I_3 + \frac{-sA_{a1}I_2C_1R_{inc} - A_{a1}I_2 + A_{a1}I_2A_{c2}A_d + A_{c1}A_{a1}I_1}{s^2R_{inc}C_1C_2R_{ina} + s(C_1R_{inc} + C_2R_{ina} - A_{c2}A_dC_2R_{ina}) + A_{c1}A_bA_{a2} - A_{c2}A_d + 1} \tag{6}$$

$$I_{out} = I_3 + \frac{I_1 - sI_2C_1R_{inc}}{s^2C_1C_2R_{ina}R_{inc} + sC_1R_{inc} + 1} \tag{7}$$

5 Conclusion

We introduced new nullor-equivalents to represent the pathological elements possessing inverting characteristics, they were the VM and CM, and we introduced also the nullor-equivalent for the MO-CM. These nullor-equivalents were used in the symbolic NA formulation of two active filters. From the results, it can be appreciated that our proposed nullor-equivalents are quite useful to perform symbolic NA to gain insight on the behavior of the circuits, because they include the input and output parasitics and gain. Furthermore, the generated expressions were the same as the ones already provided in the references, but we calculated first the exact symbolic expressions and then we reduced them by approximating ideal characteristics. In this manner, we conclude that our proposed nullor-equivalents are very suitable to perform symbolic NA which can be used within an ADA environment to enhance circuit modeling and synthesis methods, and to validate circuit-equivalents in the transformation of circuit topologies.

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