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DC offset control with application in a zero-IF 0.18 μm CMOS Bluetooth receiver chain

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Abstract A compact DC offset correction circuit based on the intrinsic properties of quasi-floating gate (QFG) transistors is presented. The proposed scheme uses a tuning mechanism to make its initial response faster improving the traditional large settling time of these circuits. A zero-IF baseband receiver chain suitable for Bluetooth that includes the proposed dc offset correction has been designed in a 0.18 μm CMOS technology at 1.2 V supply voltage.

Keywords Direct-conversion receivers · DC offset · Low power and low-voltage circuits · QFG transistors

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1 Introduction

Zero-IF receivers can meet the stringent requirements of transceivers for Bluetooth applications in terms of cost, size, integration and power consumption compared to the conventional superheterodyne architecture. Nevertheless, among the drawbacks the DC-offset is one of the most important ones as the desired signal is down converted directly to baseband [1–3]. Moreover, as most of the amplification takes place in the baseband chain, any small DC offset that appears at the baseband will be amplified to a level that could saturate the remaining stages. Typical schemes for removing DC offset use low value resistances in order to minimize the noise and high value capacitances that are off or on chip. Due to the low frequency time constant of the RC filter, long transients at the startup phase during power on can occur that can also affect the circuit performance. We propose in this paper a compact and efficient circuit to control the offset that features a low pass filtering behavior using QFG transistors. In order to show the operation of the proposed DC offset cancellation circuit, a zero-IF 0.18 μm Bluetooth receiver chain has been designed. Simulation results about the effect of the DC offset control circuit in the whole receiver chain will be presented. Special care will be paid to show how the startup circuitry aids to a fast DC settling avoiding long saturation transients when powering up the circuit.

2 Proposed DC offset circuit correction

The proposed scheme (Fig. 1) is based on sensing the DC offset component at the output of any baseband processing block (VGA, Filter, Limiter, etc.) and feeding it back to its input. The DC sensing circuitry is basically a current

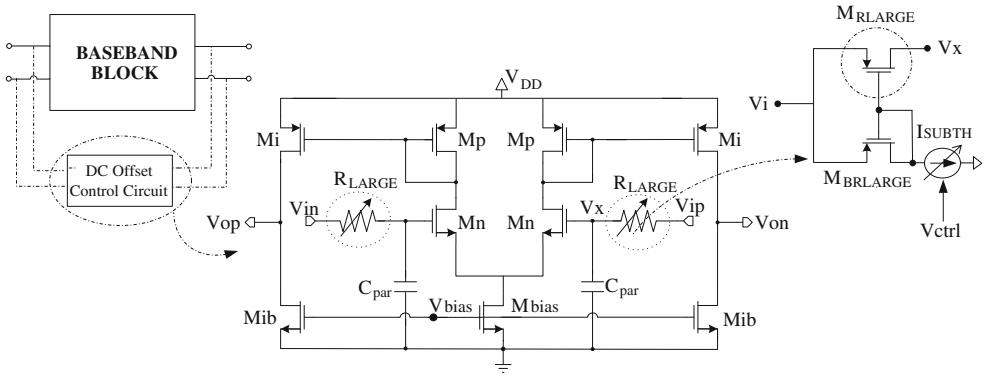

Fig. 1 Proposed offset control circuit

mirror operational amplifier with a low pass RC filter at the input stage. Depending on the implementation of the baseband block, the output of the DC-offset correction circuit will be in the form of voltage or current. The RC low pass filter is implemented by a high-resistance active element (R_{LARGE}) while the capacitor (C_{par}) can be implemented by the parasitic capacitor of the amplifier input transistor M_n.

The key issue is how to implement a large resistive active element to produce a large time constant (low cutoff frequency) that can also be tuned in order to avoid large transients at startup phase. As it is known, slow transients at this initial phase can saturate the receiver chain. The large resistive active element has already been implemented by some of the authors using the large (and nonlinear) leakage resistance of reversed-biased p-n junctions of MOS transistor operating in cutoff region [4]. Recently this technique has also been used in [5]. Nevertheless, this implementation for R_{LARGE} limits the voltage transfer from V_i *to* V_X. This is due to the voltage divider formed by the leakage resistance of a reverse biased floating junction (such as the p-diffusion within an n-well) and the distributed leakage resistance of the well-substrate junction. As a result the voltage applied to the gate V_X can significantly differ from the input voltage V_i. V_X might also show drift with temperature changes. The circuit solution proposed in this paper is to use MOS transistors operating in subthreshold region [6] to emulate a large resistor. The advantage of this approach is that the resistance of a transistor operating in subthreshold is very large (tens of GΩ) but still several orders of magnitude lower than the leakage resistance of a reverse biased PN junction, preventing the voltage divider effect previously addressed. This also leads to a well controlled and temperature independent voltage $V_X = V_i$.

This will allow to control at startup phase the value of this large resistor to solve the tradeoff between low cutoff frequency and large settling time. Figure 1 shows the tuning mechanism. The gate control voltage of the biasing transistor M_{RLARGE} is generated using another diode connected transistor M_{BRLARGE}, which is forced to operate in subthreshold by biasing it with a very small current I_{SUBTH}. The value of I_{SUBTH} can be tuned in order to provide a resistive active element M_{RLARGE} with a tunable channel resistance. This way it is possible to feature a smaller resistance at startup using two biasing currents: a first one, $I_{\mathrm{SUBTH}} = I_{\mathrm{startup}}$, which makes the circuit to reach quickly a stable working point, and a second one, $I_{\mathrm{SUBTH}} = I_{\mathrm{bias}}$, which allows the circuit to reject the offset using a low cutoff frequency. These currents depend on the block under control since it flows also at its output stage, but I_{startup} must be always slightly larger than the current I_{bias} in order to obtain a faster time constant. In fact, with the use of the proposed structure, a quasi-floating gate (QFG) transistor [4] is being emulated at the input of the circuit in Fig. 1. The use of QFG transistors has two advantages: The presence of a low pass filter at the gate of transistor Mn allows the current mirror opamp to sense and feed back only low frequency signals (DC offset); and the large resistance allows the use of low valued capacitors (parasitic capacitance) for the implementation of a large time constant. The use of the proposed technique is also dependent on the position of the block under control within the receiver chain as typically noise figure of each block increases as the signal advances through the receiver.

3 Bluetooth receiver chain

The baseband receiver chain (Fig. 2) consists of two variable gain amplifiers (VGA) with programmable gain of 0–20 dB in 10 dB steps, a third order Chebyshev low pass filter with a nominal cut-off frequency of 1 MHz and 10 dB gain, and a limiter formed by four voltage gain

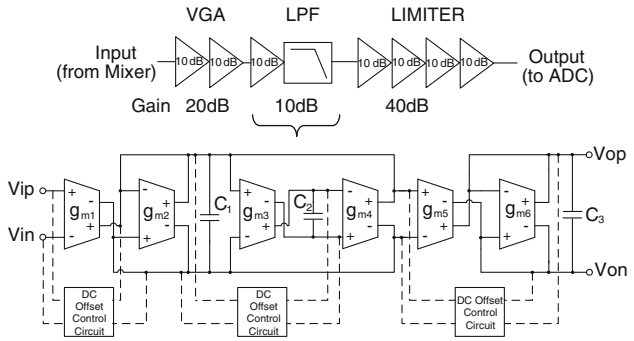

Fig. 2 Zero-IF receiver chain and detail of the 3rd order Chebyshev low pass filter with the proposed DC offset cancellation

amplifiers with programmable gain of 0–40 dB in 10 dB steps. The two VGAs have been implemented using a transconductor and a programmable resistance. The transconductor is a telescopic topology with a pair of nMOS input transistors operating in the triode region that provide linear V–I conversion, and a gain boosting scheme to increase the output resistance. For the two VGAs, the DC offset control circuit has been placed between the input of the second VGA and the output of the first one in order not to affect the noise figure of the first VGA and so, the noise figure of the whole chain.

The third order Chebyshev low pass filter is shown in Fig. 2. A Gm-C topology has been chosen and the mentioned telescopic transconductor is used as building block. Two DC offset correction blocks have been implemented, one for the second order biquad and another for the first order integrator. The last block of the receiver chain is a limiter composed by four variable gain amplifiers with 10 dB gain each. These VGAs are composed basically by a classical two-stage Miller opamp in negative feedback configuration with two resistances, one of them with a fixed value and the other one with a programmable value in order to obtain the desired programmable gain. Moreover, a capacitance has been included in the structure to provide further out of bad signal rejection. The power consumption for the DC offset control circuit depends on the consumption of the circuit in which this block is going to be used. In the blocks described before the currents used in the case of the first two VGAs are $I_{\text{startup}} = 20$ nA and $I_{\text{bias}} = 17.85$ pA, for the filter $I_{\text{startup}} = 20$ nA and $I_{\text{bias}} = 874$ fA and for the limiter $I_{\text{startup}} = 300$ pA and $I_{\text{bias}} = 100$ fA.

4 Simulation results

In order to prove the efficiency of the circuit proposed, some simulations have been performed. Figure 3 illustrates the transient response of the whole receiver chain for a 70 μVpp sinusoidal input with a DC offset level of 1 mV and 70 dB gain in the receiver chain. It can be noticed the good performance of the circuit proposed as it is able to remove high DC offset levels. Figure 4(a) shows the effect of the DC offset control circuit in the magnitude of the frequency response of the whole receiver chain, with DC offset control (solid trace) and without it (dashed trace). A high pass first order filter behavior with very low cut off frequency can be observed. A detail of the variation of this cutoff frequency against mismatch between M_{BRLARGE} and M_{RLARGE} can be found in Fig. 4(b).The transient response

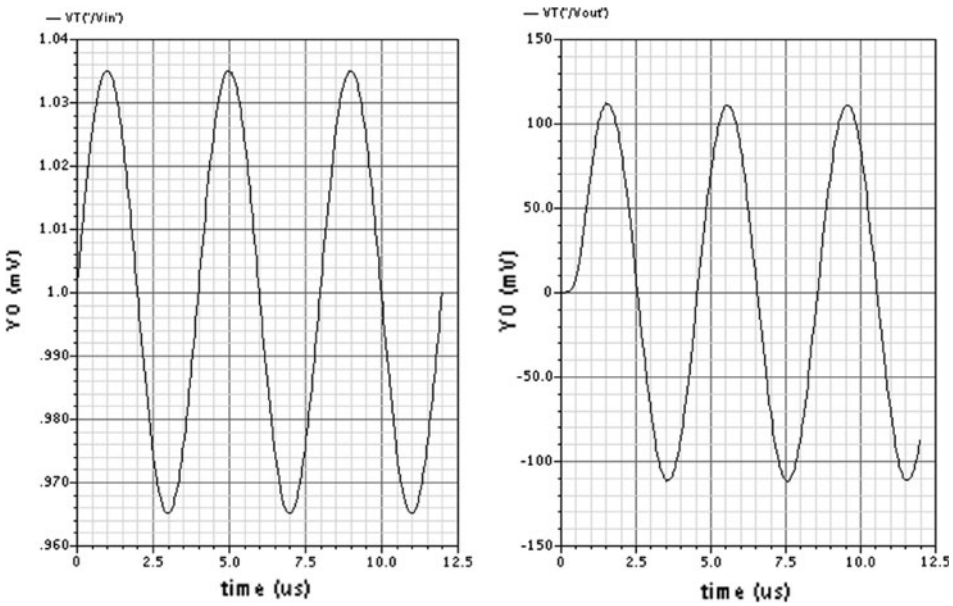

Fig. 3 Input/output waveforms to a 70 μVpp sinusoidal input with a DC offset input level of 1 mV and 70 dB gain in the receiver chain

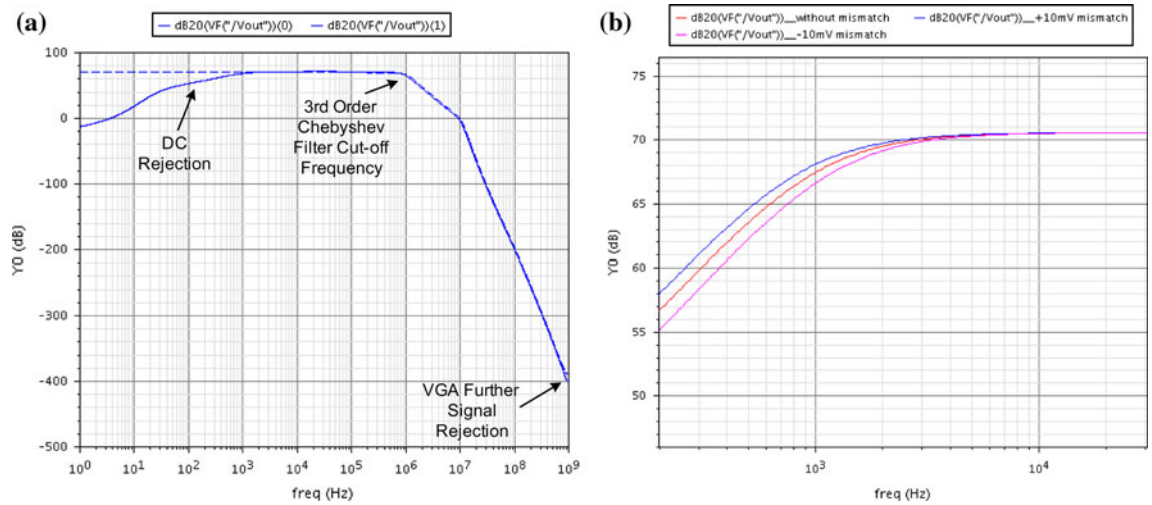

Fig. 4 **a** Frequency response magnitude of the whole receiver chain, **b** detail of high pass cut off frequency variation against threshold voltage mismatch between M_{BRLARGE} and M_{RLARGE}

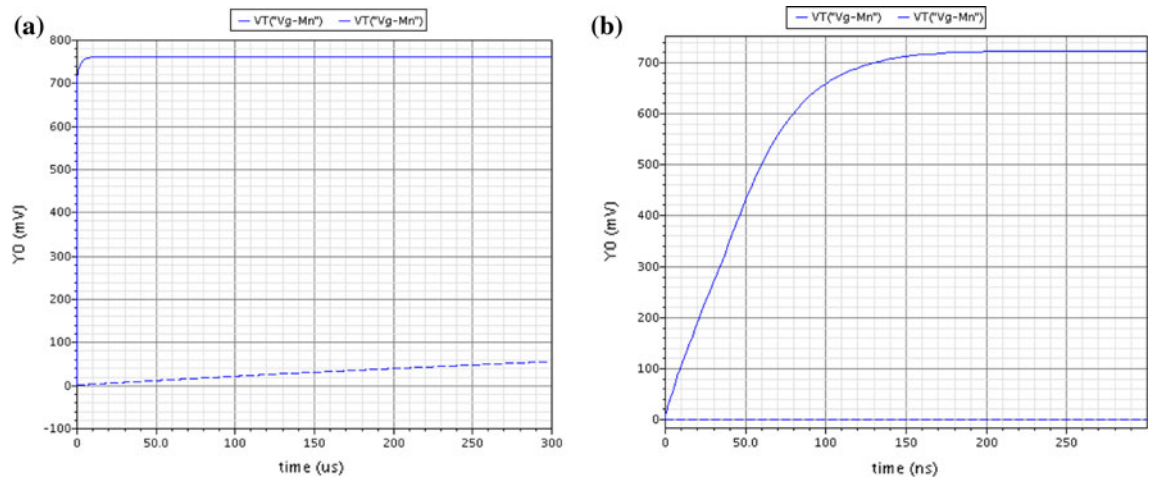

Fig. 5 **a** Transient response of the gate of transistor M_n using the DC offset control circuit proposed in [5] and the one proposed in this paper, **b** detail of the initial settling time

of the circuit proposed in this paper is compared to the scheme reported in [5], which uses a cascade of transistors operating in cutoff region to emulate the large resistive element. Figure 5 shows how the proposed tuning for transistors operating in subthreshold region, emulating a large active resistance R_{LARGE}, allows the circuit to improve the settling time at the startup. In Fig. 5(a), the transient response of the voltage at the gate of the input transistor M_n (Fig. 1) using the scheme reported in [5] is depicted in dashed trace, and the scheme proposed in solid trace. Note the large difference in the settling time for reaching the DC operating point of the voltage between both circuits. Figure 5(b) shows a detail of this initial settling time. The proposed circuit achieves a good performance with small area and low power consumption.

5 Conclusions

A DC offset cancellation with a novel tuning mechanism to control the settling time has been presented. The proposed scheme is based on QFG transistors where the large resistor is implemented with transistors operating in subthreshold region whose channel resistance can be adjusted. The features of the proposed DC offset circuit have been shown in a zero-IF Bluetooth receiver chain designed in a 0.18 μm CMOS technology from a 1.2 V supply voltage.

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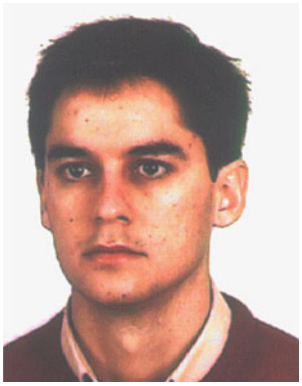

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