

Analysis of a high frequency and wide bandwidth active polyphase filter based on CMOS inverters

Johan Wernehag · Henrik Sjöland

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Abstract An active polyphase filter capable of high frequency quadrature signal generation has been analyzed. The resistors of the classical passive polyphase filter have been replaced by transconductors, CMOS inverters (F. Tillman and H. Sjöland, *Proceedings of the Norchip Conference* (pp. 12–15), Nov. 2005; *Analog Integrated Circuits and Signal Processing*, 50(1) 7–12, 2007). A three-stage 0.13 μm CMOS active polyphase filter has been designed. Simulations with a differential input signal show a quadrature error less than 1° for the full stable input voltage range for frequencies from 6 GHz to 14 GHz. Phase errors in the differential input signal are suppressed at least three times at the output. Corner simulations at 10 GHz show a maximum phase error of 3° with both n- and pMOS slow, in all other cases the error is less than 0.75° . The three-stage filter consumes 34 mA from a 1.2 V supply. To investigate the robustness of the filter to changes in inverter delay, an inverter model was implemented in Verilog-A. Linear c_{in} and g_{in} were used, whereas g_m , c_{out} , and g_{out} were non-linear. It was found that the filter could tolerate substantial delays. Up to 40° phase shift resulted in less than 1.5° quadrature phase error at the output.

Keywords Active polyphase filter · RF · CMOS · Quadrature generation

1 Introduction

Popular architectures for integrated radio transceivers, like direct conversion and low-IF, require quadrature local oscillator signals. As the carrier frequency increases in the quest for more bandwidth, generating accurate quadrature signals becomes a major challenge. There are a number of ways to generate high frequency quadrature signals, some are: (i) Quadrature oscillator, (ii) Frequency division of a differential oscillator running at twice the frequency. After the frequency division quadratures phases can be obtained, (iii) Differential oscillator followed by a passive polyphase filter, and (iv) Differential local oscillator + active polyphase filter [1, 2].

To build quadrature *LC* oscillators at high frequencies is possible but more difficult than at lower frequencies, since the coupling of the oscillators adds capacitance to the oscillating nodes and thus reduces the tuning range. Despite this some high frequency *LC* quadrature voltage controlled oscillators can be found in [3–6]. In ring oscillators the quadrature phases can be obtained more or less for free, but the phase noise is much higher than in the CMOS *LC* counterparts [7–9]. Using other processes like SiGe the obtainable phase noise will be of the same level as for CMOS *LC* oscillators [10]. To divide the frequency of an oscillator running at twice the frequency is also possible, but might be difficult with low phase noise at high frequencies. Using a passive polyphase filter and a differential local oscillator is a well proven way of generating quadrature signals. At high frequencies, however, losses become problematic. At frequencies of tens of GHz the component values must be made small, resulting in poor matching and low input impedance. An active polyphase filter has the same demands on low resistance values. These can, however, be implemented by increasing the

J. Wernehag (✉) · H. Sjöland
Department of Electrical and Information Technology,
Lund University, Box 118, 211 00 Lund, Sweden
e-mail: Johan.Wernehag@eit.lth.se

H. Sjöland
e-mail: Henrik.Sjoland@eit.lth.se

transconductance, g_m , of the active part in the filter, see Fig. 17. The active elements eliminate the problem of signal attenuation, and also increase the input impedance.

Also after downconversion, at Intermediate Frequency (IF), quadrature signals are often used, and active or passive polyphase filters can be used to suppress signals at the image frequency [1, 2, 11–14].

In this paper the capability of using an active polyphase filter based on CMOS inverters for high frequency quadrature generation is investigated. Compared to a passive polyphase filter an active one is more complicated, as it contains non-linear devices in the signal path, and although the architecture is known [2] more investigations in this area are needed. The investigated three stage active polyphase shows a $\pm 40\%$ bandwidth from 6 GHz to 14 GHz with less than 1 degree quadrature error.

The rest of this paper is organized as follows: in Sect. 2 the passive polyphase filter is shortly recaptured. In Sect. 3 the transistor is examined and a transistor model is derived and verified against transistor level simulations. Parameters of the model are stretched and the effects on the active polyphase filter are observed. Section 4 shows simulated results of the active polyphase filter in a 130-nm 1p8M CMOS process. Section 5 investigates the stability of the active polyphase filter through PVT simulations.

2 Passive polyphase filter

We start with a short summary of the passive polyphase filter, Fig. 1. It is well known [2, 15, 16] that the voltage gain of this filter is $\sqrt{2}$ for an unloaded stage and $1/\sqrt{2}$ for a stage in a cascaded chain of identical stages. Assuming all R and C to be perfectly matched, a differential input signal at V_I^+ and V_I^- will be converted to a perfect quadrature output signal, if the frequency is exactly equal to $1/2\pi RC$. If quadrature signals must be generated over a

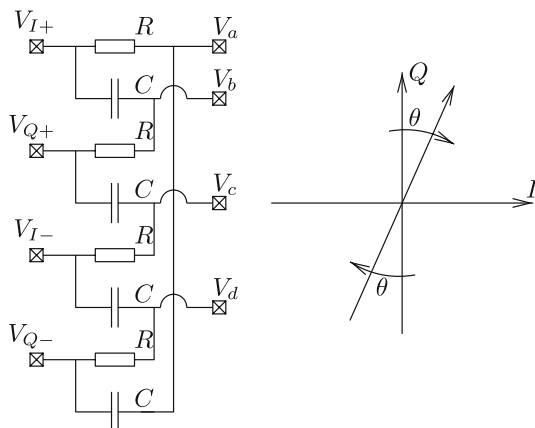


Fig. 1 A passive RC polyphase filter

wide frequency range, or if process variations are significant, several stages can be cascaded, tuned to different frequencies. Good matching of the components in each stage is essential, as it limits the achievable quadrature accuracy.

The Image Rejection Ratio (IRR) of a quadrature receiver depends on the quadrature accuracy, and can be written as:

$$IRR \approx \frac{4}{\epsilon^2 + \theta^2} \Big|_{\text{Small } \epsilon \text{ and } \theta}, \tag{1}$$

where ϵ denotes the relative amplitude error and θ the quadrature error in radians between the I and Q phases.

In a receiver architecture relying on quadrature downconversion, the achievable image rejection ratio is typically in the range of 30–40 dB [13, 17–19], without calibration schemes. In order to increase the image rejection, very accurate quadrature signals, both phase and amplitude, must be generated. As can be seen in [12] a phase error of $\pm 5^\circ$ leads to a maximum image rejection of 30 dB, whereas an amplitude error of $\pm 12\%$ is allowed for the same rejection ratio. In practice typically switching mixers are used, and the amplitude error is then less important.

3 Active polyphase filter analysis

In this paper the resistors of the passive polyphase filter are replaced by transconductors. With ideal transconductors g_m should be equal to $1/R$ not to change the frequency of operation. The gain of the active filter can be larger than unity and the load on the preceding stage reduced thanks to the higher input impedance of the transconductor compared to the resistor. Since the active polyphase filter is a feedback structure, with many different feedback paths, the stability is examined in Sect. 3.1.

The transconductor investigated in this paper is designed using a 1p8M 130-nm CMOS process and an extraction frequency of 10 GHz, but the procedure and derived equations are not dependent on the process, only some numerical values calculated.

3.1 Stability of the active polyphase filter

A three-stage active polyphase filter was designed and simulated. It was found that the filter becomes unstable at small input signal amplitudes. The input amplitude should be larger than 200 mV to stop the filter from self oscillating and instead lock to the input signal. At 280 mV input amplitude the full saturated output amplitude of 600 mV was reached.

When instability occurs the filter oscillates in a differential mode. The inverters in the second stage then forms a

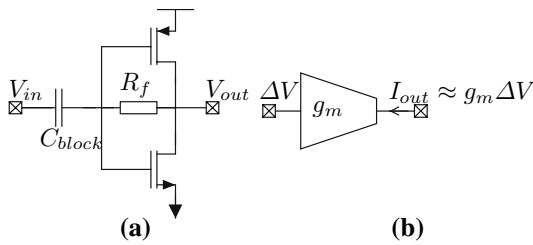


Fig. 2 **a** Schematic of the transconductor with internal feedback and DC-block capacitance. **b** Symbol of the transconductor

4-stage ring oscillator. The same happens in the third stage. Due to the internal structure of the transconductor, see Fig. 2(a), also a ring with an even number of stages can self-oscillate. When the input signal is too small to force the inverters to switch, the positive feedback of the ring will make them saturate at high or low. The internal feedback through R_f then slowly changes the gate potentials, through the RC time-constant between the feedback resistor and the capacitance at the gate, until the inverters switch. This causes the whole ring to change state. The periodicity is set by the feedback resistance and the capacitance at the gate. The loop gain at the self oscillation frequency decreases with increasing input amplitude and the filter eventually stops oscillating and instead locks to the input signal.

Not having the internal feedback and DC-block, DC-offsets would be amplified and the filter could saturate at high or low potential. Thus there is a trade-off between voltage gain, feedback resistance, and minimum input amplitude. However, this high frequency polyphase filter is intended to transform a differential oscillator signal into a quadrature one, and generally the amplitude from an oscillator is quite large. Thus instability should not be a problem in this application.

3.2 Transconductor

The transconductor is to be used as a component in the high frequency polyphase filter, therefore the fewer internal nodes the better. The transconductor used in this analysis is a CMOS inverter with input DC-block and bias voltage feedback (Fig. 2). The purpose of the DC-block and bias feedback is to set the DC potential at the outputs to $V_{DD}/2$, so that any DC offset that might occur does not get amplified in the filter chain.

The analysis is not restricted to this implementation of the transconductor, however, since an extracted model is used in all the analysis and such a model can be extracted for any implementation of the transconductor. However, when numerical results are given these are, of course, for this transconductor.

The objective is to extract a model which captures the non-linearities of the transconductor when both input and output amplitude are large, and yet is not more complex than necessary. The approach we took was to start from the transistor behavior. From that it was assumed that the most non-linear elements are the transconductance, g_m , and the output admittance, y_{out} , which is modeled as g_{out} in parallel with c_{out} . The other elements in the model are considered linear in the analysis. The transconductor model is shown in Fig. 3 together with the values extracted at 10 GHz (the extraction frequency $f_0 = 10$ GHz).

This model was implemented in a Verilog-A transconductor used to verify the validity of the extraction. The extraction was performed in three steps using transient simulations:

1. The output admittance, amplitude and phase, was simulated versus output voltage amplitude while the input was at its DC bias level. The output conductance and capacitance were fitted to third order polynomials, see Fig. 4.
2. g_m was extracted by stimulating the transconductor with a sinusoidal input voltage and loading the output with a small signal short circuit. The transient output current and input voltage were then used to calculate the g_m polynomial, see Fig. 5.
3. The small signal c_{in} and g_{in} were extracted from a transient simulation. By observing the magnitude and phase relation of the input voltage and current the complex admittance was calculated and g_{in} and c_{in} extracted.

The voltage gain of the transconductor was simulated (Fig. 6). There is a good agreement between the extracted model and transistor up to about 50% of full swing. The error at large amplitudes is due to the extraction procedure, where large signals were not simultaneously applied to input and output. To capture this a more complicated

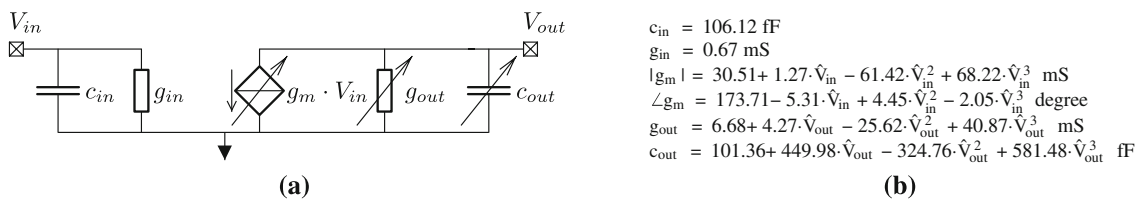


Fig. 3 Model extracted for the transconductor at $f_0 = 10$ GHz. **a** A lumped model. **b** The corresponding parameters

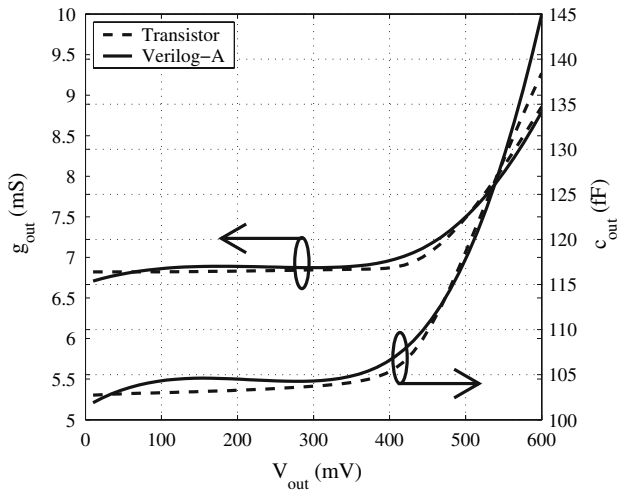


Fig. 4 Output admittance extracted as g_{out} and c_{out} compared to the transistor model

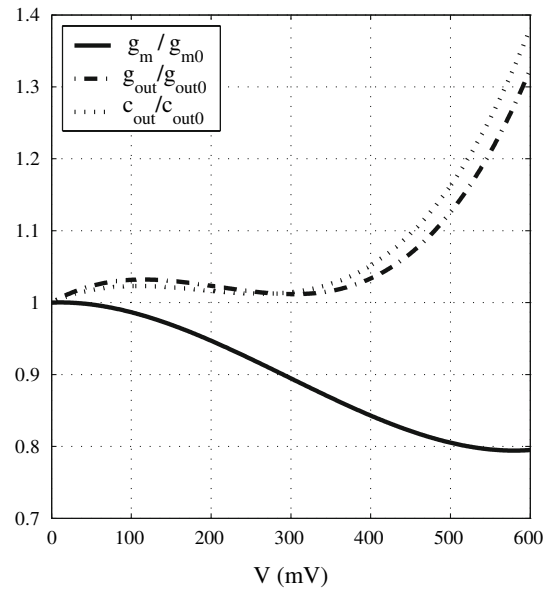


Fig. 7 Plot of three of the non-linear transconductor parameters as they change with the voltage at input or output of the transconductor

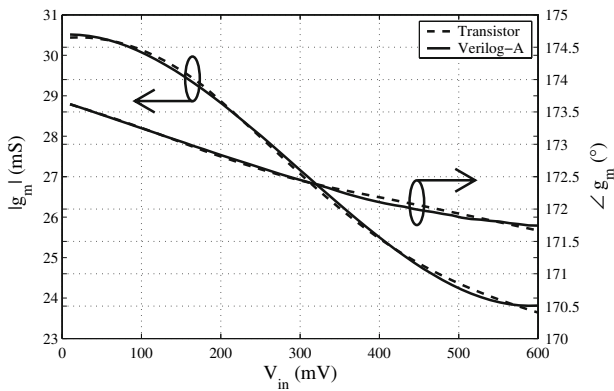


Fig. 5 The transconductance fitted to the Verilog-A model and compared to the transistor model

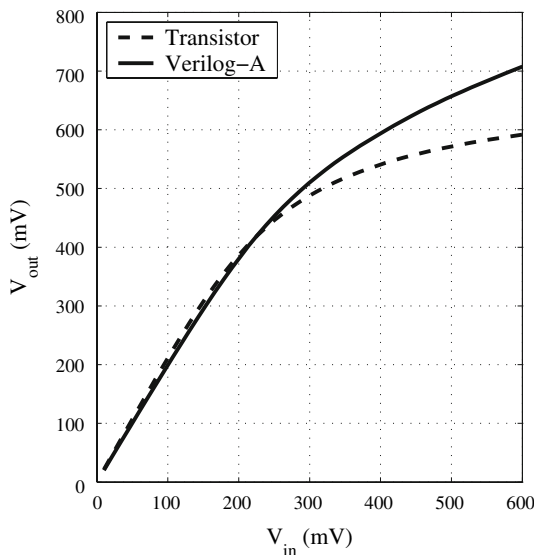


Fig. 6 Output voltage magnitude versus input magnitude for both transistor and Verilog-A implementation. Full voltage swing is 600 mV

model would be necessary, but for our purposes the level of accuracy achieved is sufficient.

To give an indication of the level of non-linearity, the three non-linear parameters, normalized with their small signal values, are plotted in Fig. 7. The magnitude of g_m is within 20% of its small signal value over the amplitude range, g_{out} and c_{out} are within 20% of their small signal values, up to an amplitude of 510 mV, which corresponds to 85% of the full voltage swing. The phase of g_m only changes by a few degrees over the full range (Fig. 5).

3.3 Voltage gain

To calculate the voltage gain of a stage in the active polyphase filter Fig. 8 was used. By applying Kirchoff's current law in node a , by inspection one gets (2a). Inserting the expressions for the currents (2b)–(2e) and solving (2a),

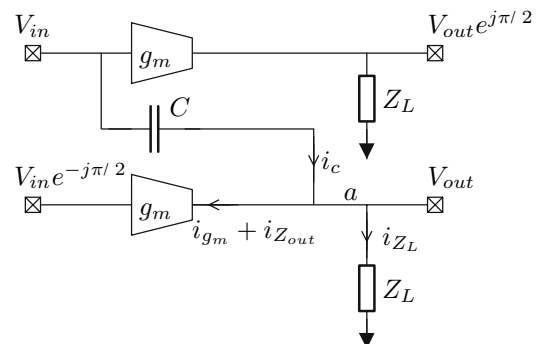


Fig. 8 Schematic of a part of the polyphase filter suitable to calculate the voltage gain of a stage

results in the voltage gain (3). At the designed frequency, where $g_m = \omega_0 C$, (3) can be simplified to (4). The unloaded voltage gain with ideal transconductor ($Z_{out} = \infty$) can then be found to be equal to 2, as in [2]

$$0 = i_c - i_{g_m} - i_{Z_{out}} - i_{Z_L} \tag{2a}$$

$$i_c = (V_{in} - V_{out})j\omega C \tag{2b}$$

$$i_{g_m} = g_m V_{in} e^{-j\frac{\pi}{2}} \tag{2c}$$

$$i_{Z_{out}} = V_{out}/Z_{out} \tag{2d}$$

$$i_{Z_L} = V_{out}/Z_L \tag{2e}$$

$$A_V = \frac{V_{out}}{V_{in}} = j \frac{\omega C + g_m}{j\omega C + 1/Z_{out} + 1/Z_L} \tag{3}$$

$$A_V|_{\omega C = g_m} = j \frac{2g_m}{jg_m + 1/Z_{out} + 1/Z_L} \tag{4}$$

Equation 2e through 4 contain the load impedance, Z_L . In a chain of cascaded stages, the load impedance can be calculated as Z_{in} of the transconductor in parallel with the impedance looking into the filter capacitance, C . Making the observation that the voltage is in phase¹ at both sides of the capacitance leads to an equivalent impedance of the filter capacitance:

$$Z_C = \frac{1}{j\omega C(A_V - 1)} \tag{5}$$

The equivalent impedance of the filter capacitance is determined by the voltage gain of the stage. When the voltage gain is high the capacitance is increased. When the filter is saturated ($A_V = 1$) the capacitance becomes a virtual open circuit. The effect can be expressed as charge efficiency,

$$\frac{C_{in}}{C_{eqv}} = \frac{C_{in}}{(A_V - 1)C}, \tag{6}$$

which is a measure of the energy it takes to make a transition for the transconductor compared to charging the filter capacitances. The charge efficiency is simulated for a three-stage active polyphase filter in Sect. 3.5. When the polyphase filter is saturated the charge efficiency becomes infinite.

With (5) the load impedance, or rather admittance, can be expressed:

$$Y_L = Y_{in} + Y_C = Y_{in} + (A_V - 1)j\omega C \tag{7}$$

Assuming the stage is loaded by an identical one, the voltage gain (3) can be solved by inserting (7) and solving for A_V :

¹ The input of the second transconductor in Fig. 17 is 270° out of phase with respect to the one above, the transconductor inverts the signal to the output changing the phase to 90°. The output current is integrated reducing the phase by 90°. Thus the signals are in phase.

$$A_V = -\frac{Y_{out} + Y_{in}}{2j\omega C} \pm \sqrt{\left(\frac{Y_{out} + Y_{in}}{2j\omega C}\right)^2 + 1 + \frac{g_m}{\omega C}} \tag{8a}$$

$$= -\frac{g_{out} + g_{in} + j\omega(c_{out} + c_{in})}{2j\omega C} \pm \sqrt{\left(\frac{g_{out} + g_{in} + j\omega(c_{out} + c_{in})}{2j\omega C}\right)^2 + 1 + \frac{g_m}{\omega C}} \tag{8b}$$

The negative root in (8) is discarded since it yields a negative voltage gain. Imposing small signal and low frequency (*SSLF*) conditions reduces (8b) to:

$$A_V|_{SSLF} = -\frac{g_{out} + g_{in}}{2j\omega C} + \sqrt{\left(\frac{g_{out} + g_{in}}{2j\omega C}\right)^2 + 1 + \frac{g_m}{\omega C}} \tag{9}$$

From (9) the *SSLF* voltage gain at the designed centre frequency ($g_m = \omega C$) and with ideal transconductor, that is $g_{in} = g_{out} = 0$, equals $\sqrt{2}$. From (4) the unloaded voltage gain, when Z_L is infinite, is equal to 2, also that with ideal transconductor. This agrees with the findings in [2].

In Fig. 9(a) the voltage gain (8), is plotted together with the *SSLF* voltage gain (9), and in Fig. 9(b) the simulated voltage gain is compared to (8) for an input amplitude of 440 mV². In Fig. 9(a) the achievable voltage gain is limited by the *SSLF* curve and can approach that for an ideal transconductor. For the implemented transconductor the small signal gain is just above 1.2 at the centre frequency. The correspondence between the simulated voltage gain and (8) is excellent from 8 to beyond 14 GHz, see Fig. 9(b).

3.4 Phase analysis

The output phases from a stage in the filter are analyzed using the schematic in Fig. 10. It is assumed that Z_L is equal to Z_{in} , which is valid inside a saturated filter. The output voltages, V_A and V_B , can then easily be expressed as (10a)–(10b),

$$V_A = \frac{1}{Z + Z_C} \left(XZ_C e^{-j\theta} + Z e^{-j\theta} - ZZ_C g_m e^{-j\pi/2} \right) \cdot V_{in} e^{-j\pi/2} = \frac{1}{Z + Z_C} Q_A V_{in} e^{-j\pi/2} \tag{10a}$$

$$V_B = \frac{1}{Z + Z_C} \left(XZ_C - ZZ_C g_m e^{-j(\pi/2+\theta)} + Z \right) V_{in} = \frac{1}{Z + Z_C} Q_B V_{in} \tag{10b}$$

$$Q_A = XZ_C e^{-j\theta} + Z e^{-j\theta} - ZZ_C g_m e^{-j\pi/2} \tag{10c}$$

² An iteration has been performed to accurately calculate the large signal g_{out} and c_{out} .

Fig. 9 **a** Small signal voltage gain of the active polyphase filter (8) and small signal low frequency approximation 9. **b** Analytic large signal voltage gain (8) (solid), and simulated voltage gain (dashed), $V_{in} = 440$ mV

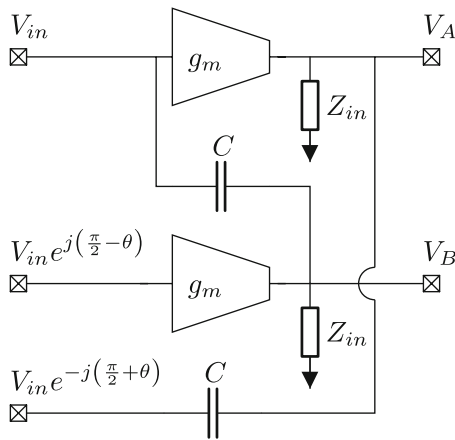
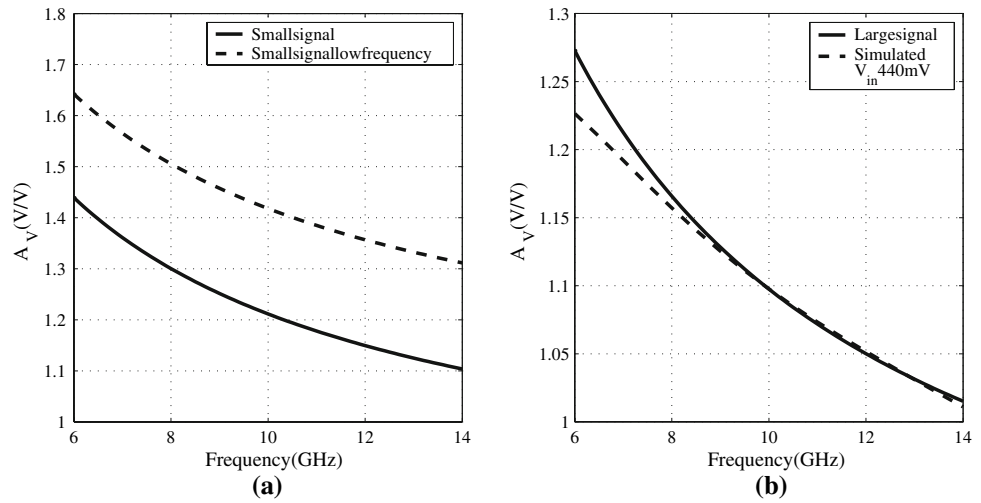


Fig. 10 Schematic used to calculate the output phase after a filter stage

$$Q_B = XZ_C + Z - ZZ_C g_m e^{-j(\pi/2+\theta)}, \tag{10d}$$

where X and Z are given by (11a)–(11b) and θ is defined in Fig. 1 as the input quadrature phase error. For quadrature output signals the phase of Q_A and Q_B should be equal, which happens only if $\theta = 0$.

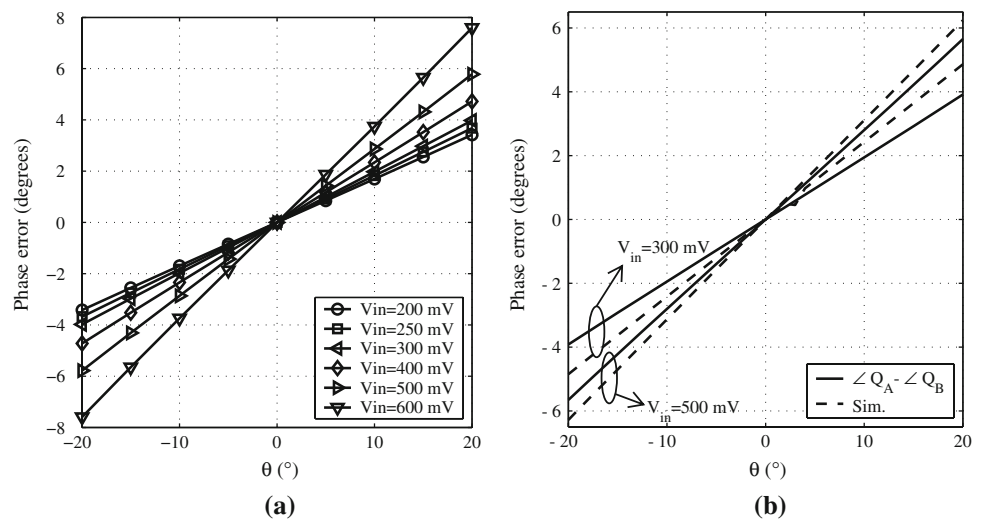
$$X = \frac{Z_{out} \parallel Z_{in}}{Z_{out} \parallel Z_{in} + Z_C} \tag{11a}$$

$$Z = Z_{out} \parallel Z_{in} \tag{11b}$$

The phase difference, $\angle Q_A - \angle Q_B$, as a function of input quadrature phase error is plotted in Fig. 11(a).

To verify the analytic expressions a comparison to simulated phase error was performed for two different input amplitudes, Fig. 11(b). The agreement is very good, justifying the assumption of Z_L being equal to Z_{in} made in the derivation.

Fig. 11 **a** Sensitivity of the phases of Q_A and Q_B with respect of the quadrature offset, θ . **b** Comparison of analytic expression (solid) and simulation (dashed)



3.5 Model simulations of the polyphase filter

In this section the three-stage active polyphase filter (Fig. 17) is simulated using the Verilog-A transconductor model from Sect. 3.2. Five aspects are investigated, the first three with quadrature input signal: (i) voltage gain versus transconductor phase delay, (ii) effective capacitance in the filter versus phase delay, (iii) charge efficiency versus frequency with scaled filter capacitance, (iv) quadrature phase error after three stages versus phase delay with differential input signal, and (v) voltage gain after the three stage filter versus phase delay with differential feed.

The voltage gain versus phase delay of the three-stage active polyphase filter is plotted in Fig. 12. At low input amplitudes the filter is unstable for large phase delays. The curves are therefore cut. The extra phase delay is added to the extracted phase of g_m in the previous section. The voltage gain reaches a maximum at about 30° phase delay for small input signals, and up to 70° for large signals.

The filter capacitances were set to $C = g_{m0}/\omega_0 = 486$ fF. The effective capacitance was calculated from the reactive part of the impedance looking into a filter capacitance. The phase delay was swept from 0 to 90 degrees for different input amplitudes. For phase delays above 50 degrees the effective capacitance becomes negative for low input amplitudes and the curves are cut, see Fig. 13. The curves in Figs. 12 and 13 show an interesting resemblance.

The effective capacitance increases with phase delay until it reaches a peak, then decreases and becomes negative. The explanation is that with no additional phase delay the current injected by g_m to the output load is almost 90°

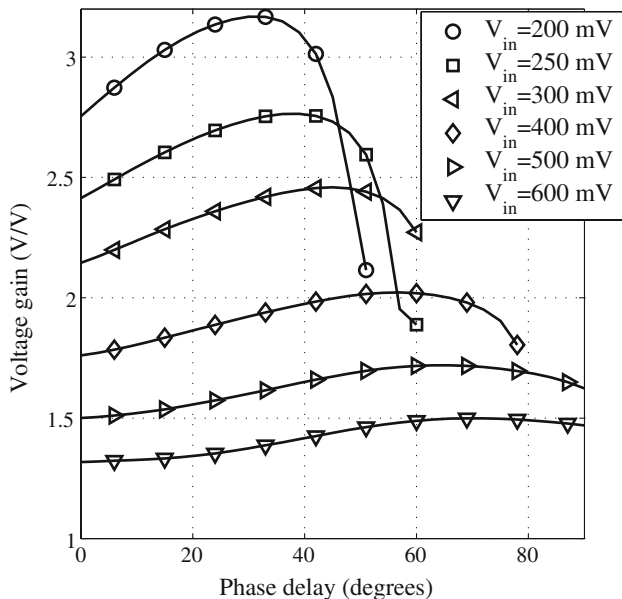


Fig. 12 Voltage gain of the three-stage active polyphase filter versus phase delay of the transconductor for six different input amplitudes

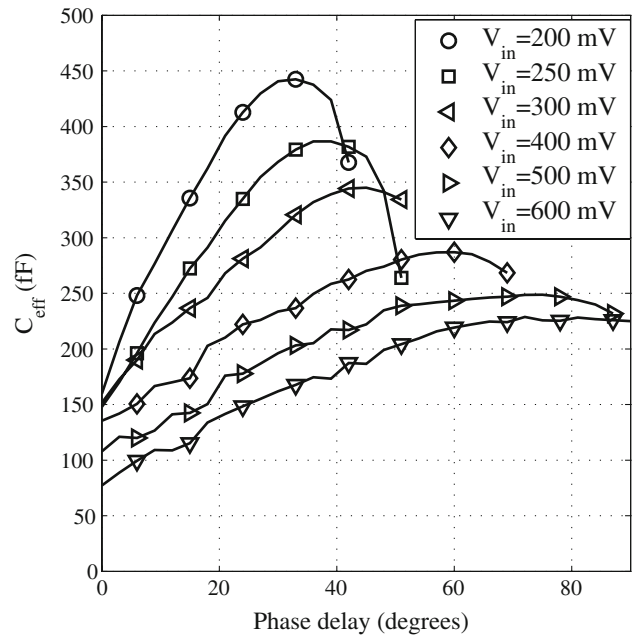


Fig. 13 Effective filter capacitance of the three-stage active polyphase filter versus phase delay of the transconductor for six different input amplitudes

out of phase with respect to the voltage at the other side of the filter capacitance, see Fig. 17. When the current is fed into the mainly capacitive impedance at the output, the output voltage will be almost in phase with the voltage at the other side of the filter capacitance. If the gain is close to unity the signal voltage over the capacitance is then small, and so is the effective capacitance. A low effective capacitance will result in a reduced power consumption and an increased capability of high frequency operation. The effective capacitance is not zero at zero additional delay, however, since there is a phase delay in g_m at 10 GHz, and that even at small amplitudes the effect of g_{out} and g_{in} is not negligible, preventing the nodes from being purely capacitive. The effect of g_{out} increases with amplitude, which is the reason why the effective capacitance does not drop until a larger phase delay is applied.

The charge efficiency is defined as the ratio between the input capacitance of the transconductor, c_{in} , and the effective capacitance in the filter, $C_{eff} = C(A_V - 1)$. The charge efficiency was simulated versus frequency, where the filter capacitance was scaled with frequency, $C = g_{m0}/\omega$, and the effective capacitance was extracted. Since the frequency was changed also the phase delay had to be changed accordingly. The delay in the transistor can be expressed as, [20]:

$$y_m = \frac{g_m}{1 + j\omega\tau_1 + (j\omega\tau_2)^2 + \dots}, \tag{12}$$

where all time-constants, τ , are $\propto 1/f_r$. Staying well below f_r , (12) can be reduced to (13):

$$y_m \approx \frac{g_m}{1 + j\omega\tau_1}, \tag{13}$$

where $\tau_1 = \frac{4}{15\omega_i}$. The transit frequencies were simulated for the transistors constituting the transconductor. The f_i used in (13) is the 43 GHz f_i of the pMOS. Equation 13 then gives a delay of 3.55° compared to the modeled 6.29° . In the simulation $\angle g_{m0}$, where g_{m0} is the small signal component of g_m , were given as $\omega \cdot \tau_1$ instead of the extracted value and the simulations were run up to 19 GHz. At this frequency τ_1/τ_2 is 13, still making the approximation (13) valid.

The simulation shows that the charge efficiency varies from 0.8 to infinity with frequency and input amplitude, see Fig. 14. The charge efficiency is smaller (1.0–2.0) at midrange frequencies and larger at higher and lower frequencies. As expected from the effective capacitance plot the charge efficiency is larger for large input amplitudes. The high charge efficiency at high frequencies indicates that the active polyphase technique can be used at frequencies close to the maximum of a chain of cascaded inverters. The addition of the cross-coupling capacitors will not slow the inverters down significantly. This also means that the additional power consumption due to the capacitors will be small.

The influence of phase delay in the transconductor on the quadrature accuracy was investigated with the three-stage active polyphase filter fed by a differential input signal (Fig. 15). The extra phase delay was, as before, added to the delay of g_m . For input amplitudes larger than

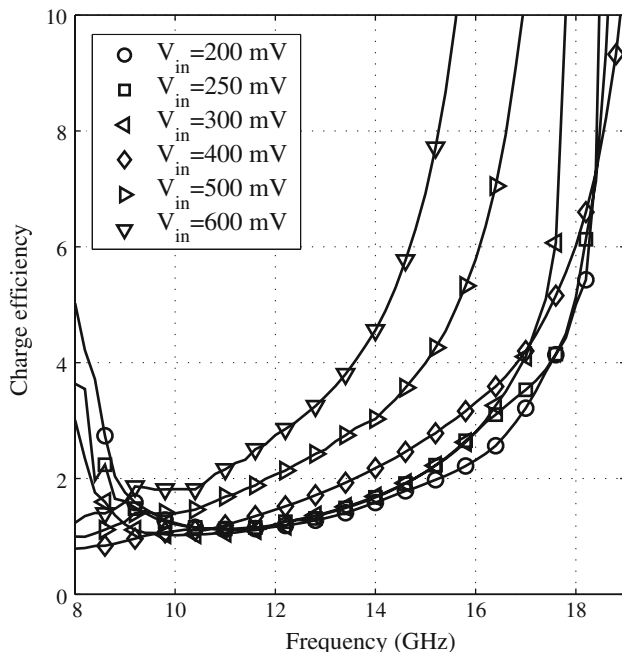


Fig. 14 Charge efficiency of the three-stage active polyphase filter for a frequency range up to approximately $f_i/2$

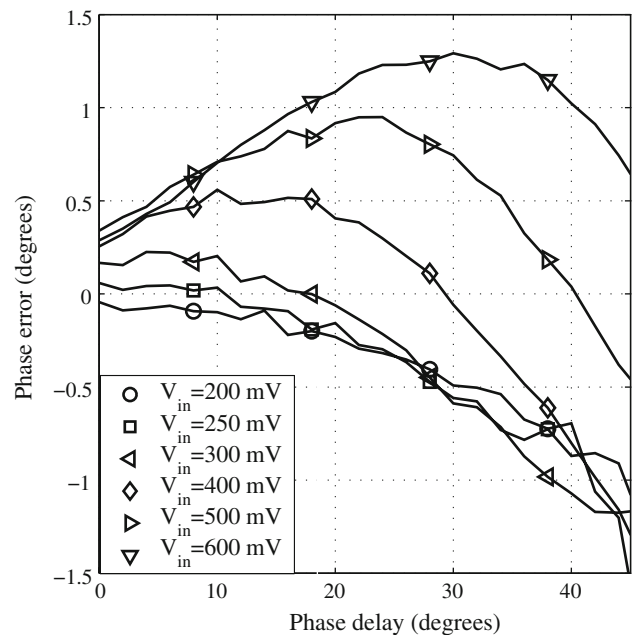


Fig. 15 Quadrature phase error versus phase delay

300 mV ($V_{DD}/4$) the quadrature error first increases to a maximum at 15–35 degrees delay and then decreases. The quadrature error for smaller signals starts close to zero and then increases with the phase delay.

A sweep of the delay over a full 360° revolution was then performed. Also the voltage gain was plotted this time (Fig. 16). The gain is still high with differential feed, it is reduced by less than 15% compared to quadrature feed (Fig. 12). Only the stable parts where the filter is locked to the input signal is shown. For phase delays in ranges above 0 and 180 degrees the polyphase filter is locked and achieves a quadrature error of less than 4° . When the filter is locked at 180° phase delay the polarities of the outputs are reversed. Surprisingly, the filter is unstable for phase delays just below 360° and 180° .

4 Active polyphase filter simulation

The three-stage active polyphase filter (Fig. 17) was simulated on transistor level to evaluate the performance and verify some of the findings of the previous section. The capacitances in the stages are decreasing in size, tuning the three stages to 8, 10, and 12 GHz by weighting the capacitances as {1.2 1.0 0.8} with respect to the nominal value found at the extraction frequency of 10 GHz. The power consumption of the three-stage filter was 40.6 mW from a 1.2 V supply.

Transient simulations in Spectre were used to evaluate the filter. The phase relations were calculated from the time of the zero crossings of the voltage waveforms, that is their

Fig. 16 Simulation of a Quadrature phase error. **b** Voltage gain versus phase delay

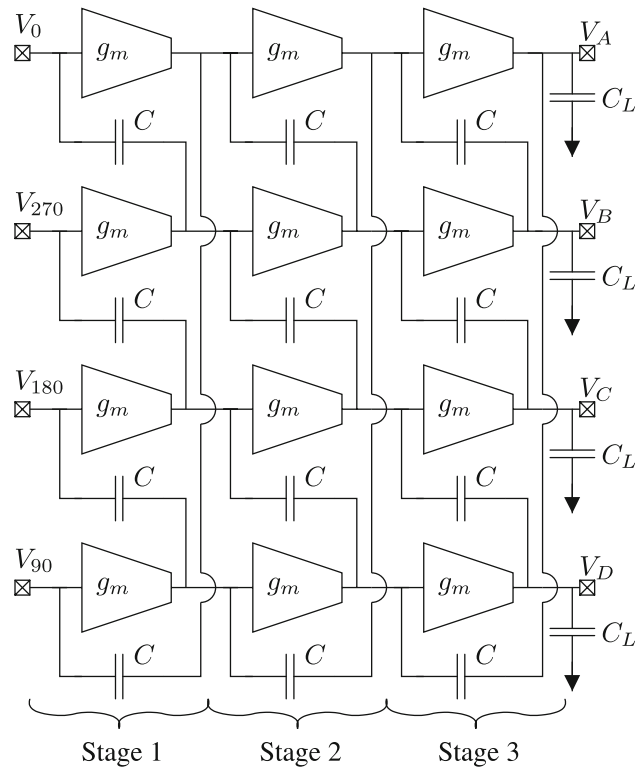
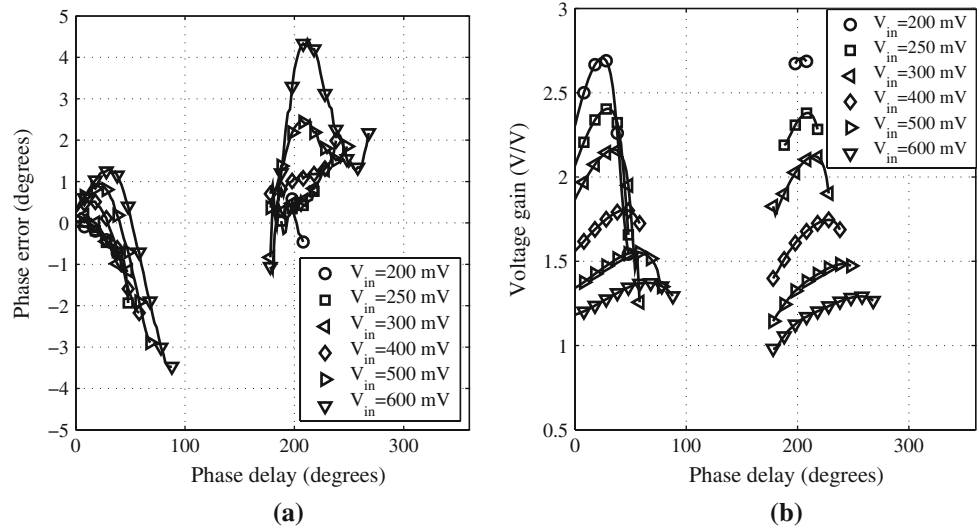


Fig. 17 An active three-stage polyphase filter, where the capacitances $C_{1,2,3}$ are weighted as $\{1.2 \ 1.0 \ 0.8\} \times g_m/\omega_0$

crossings with the bias level, after that the initial transients had settled for 100 periods. All phases are relative to the phase of V_A in Fig. 17, called I+ hereafter.

The following simulations were performed:

- Quadrature phase error versus input voltage and frequency with differential feed of the filter, Fig. 18.
- The voltage gain with differential feed for the same frequency and amplitude range as above, Fig. 19.

- Quadrature phase error versus input voltage and input differential phase error, δ , with differential feed of the filter (Fig. 20(a)).
- To verify the robustness of the active filter, corner simulations were performed for five process corners, Fig. 22. The five corners are: tt—typical n- and pMOS, ss—slow n- and pMOS, ff—fast n- and pMOS, sf—slow nMOS and fast pMOS, and fs—fast nMOS and slow pMOS. For each corner the input amplitude was swept at 10 GHz.
- The phase noise was simulated using the SpectreRF pnoise analysis and compared to an equivalent passive polyphase filter at 10 GHz, Fig. 21. Equivalent means that the passive filter resistances were set to $R = 1/g_{m0}$.

The differential feed was realized by connecting the positive phase of the input signal to the 0° and 90° inputs in Fig. 17 and the negative to the two other inputs.

As can be seen in the plot in Fig. 18(a) the quadrature phase error is less than 1° from 6 GHz to 14 GHz over the stable input voltage range. The non-stable range has been left out in Figs. 18, 19 and 20, hence the absence of data for some parts of the plots. There are also some missing data points due to simulation convergence issues. The phase error is frequency dependent, which makes it interesting to view Fig. 18(a) in the phase error-frequency-plane, Fig. 18(b). One can clearly see that the quadrature error is below 1.0° for all stable amplitudes and frequencies.

As can be seen in Fig. 19, the voltage gain at 10 GHz ranges from 5.2 to 0.2 dB when the filter is stable, ($V_{in} = 280\text{--}600$ mV). The filter is stable for $V_{in} = 200$ mV up to 6.5 GHz with a gain of more than 9 dB. At

Fig. 18 Transistor simulation results of the active polyphase filter. **a** Quadrature error versus V_{in} and frequency. **b** Quadrature error versus V_{in} for the full frequency range. Error of Q- and Q+ phases shown with respect to I+

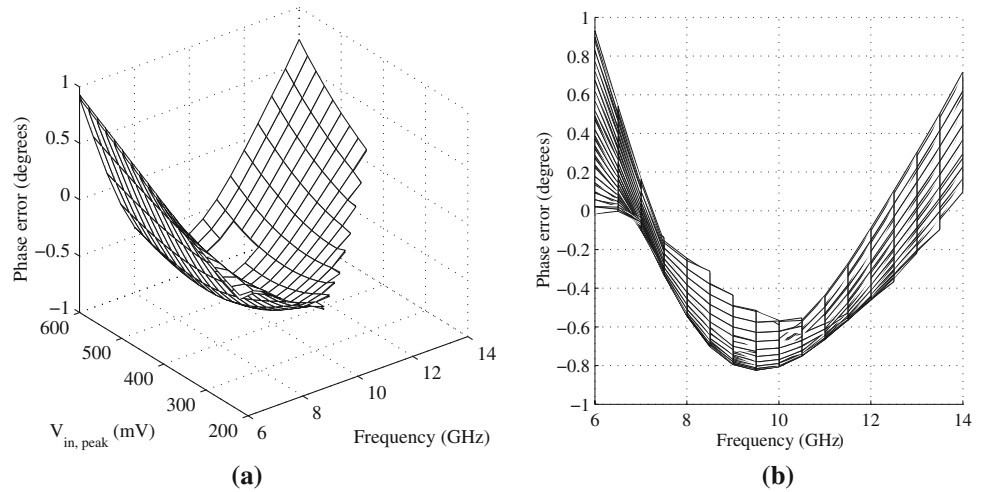


Fig. 19 Transistor simulation results of the active polyphase filter. **a** Voltage gain versus frequency and input V_{in} . **b** Voltage gain orthogonal to the frequency axis

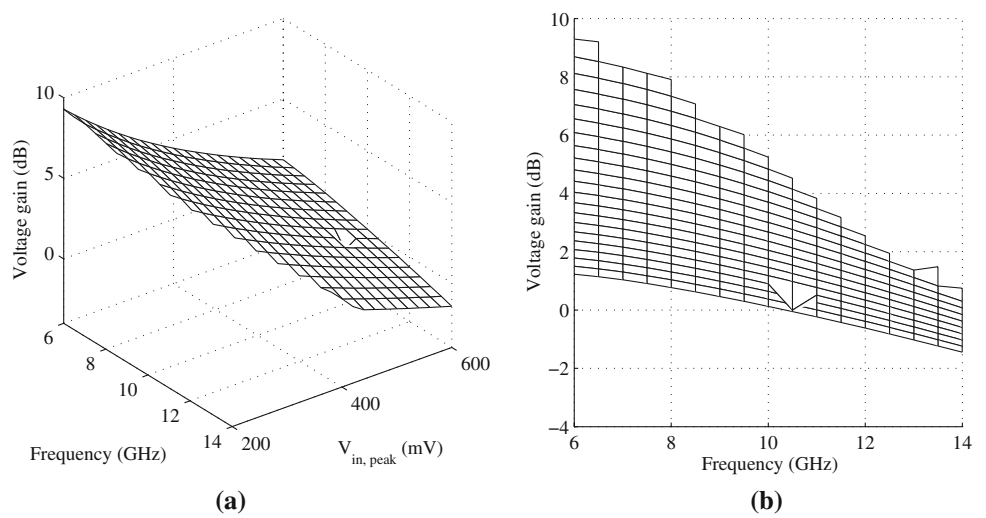
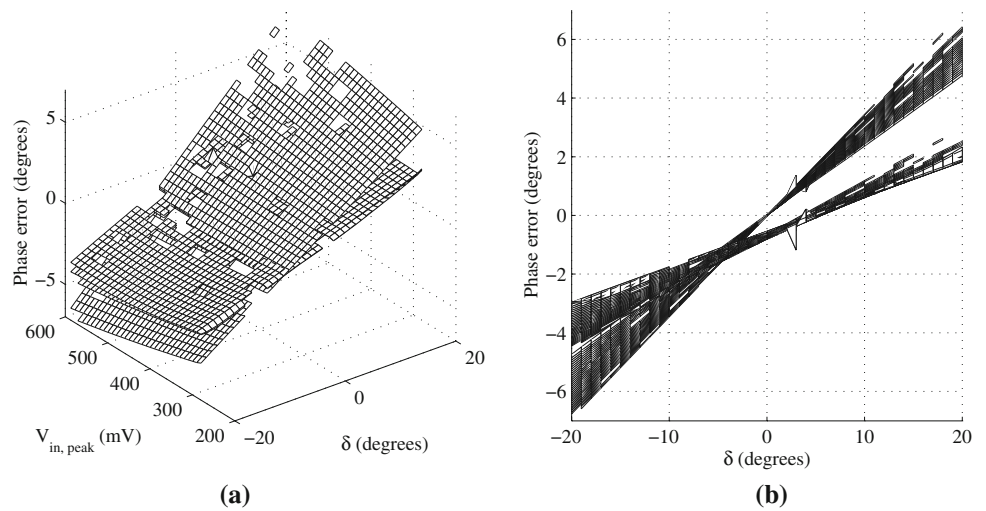


Fig. 20 **a** Quadrature phase error versus V_{in} and δ at 10 GHz. **b** The quadrature error for all three phases versus δ for full range input amplitudes



higher frequencies, larger amplitudes are required to lock the filter to the input signal. At 14 GHz 440 mV is needed, and the gain is then also lower, see Fig. 20(b).

In Fig. 20(a) the output quadrature error is plotted versus input differential errors and input amplitude. Over the full stable input voltage range the output phase error is

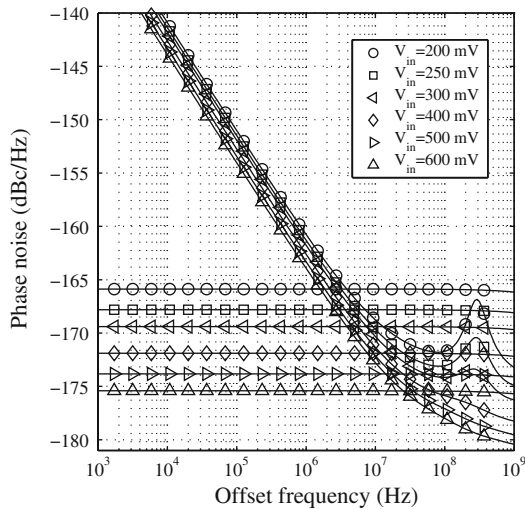


Fig. 21 Noise simulation of the active three-stage polyphase filter and its passive counterpart at 10 GHz

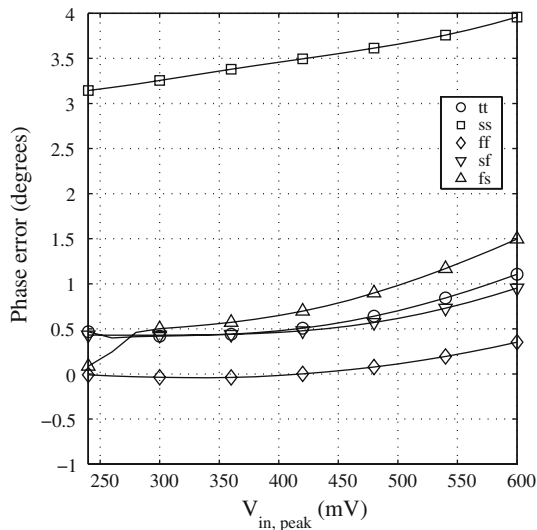


Fig. 22 Corner simulation of the active polyphase filter at 10 GHz

below $\pm 6.5^\circ$ for differential errors δ up to $\pm 20^\circ$, that is the attenuation of errors is at least three times. The error increases somewhat with the input amplitude, approximately by 2° for large mismatches. This is illustrated by the thickness of the curves in Fig. 20(b), which is Fig. 20(a) viewed in the phase error- δ -plane. There one can also clearly see that the quadrature phase error is within $\pm 6.5^\circ$ for $\delta = \pm 20^\circ$ and full input amplitude range.

The phase noise of the passive and active polyphase filters are plotted in Fig. 21. The noise of the passive filter is constant and depends solely on the resistances in the filter. Thus the phase noise level is constant versus offset frequency and decreases as the input amplitude increases, and as expected there is a 6 dB difference between $V_{in} = 300$ mV and $V_{in} = 600$ mV. For the active

polyphase filter the phase noise has a $1/f$ behavior below 10 MHz offset.

The far out phase noise of the active polyphase filter is about 5 dB better than the passive implementation, flattening out at -173 dBc/Hz ($V_{in} = 200$ mV) to -180 dBc/Hz ($V_{in} = 600$ mV).

5 Active polyphase filter robustness simulations

In this section the robustness of the active polyphase filter is examined through different simulations, usually called Process, Voltage, and Temperature (PVT) simulations. Two different process simulations are performed (i) corner simulation and (ii) statistical simulations. Since there are no Monte Carlo data available to us, the physical dimensions of the transistors have been varied in a random fashion in the statistical simulations.

5.1 Process variations

The effect of process variations on the phase error is investigated by corner and statistical simulations of the active three-stage polyphase filter at its centre frequency.

The variations of V_T , I_{dsat} , and f_T in the different process corners are given in Table 1. The quadrature error of the Q- phase is plotted in Fig. 22 at 10 GHz, for the five corners including the typical in the process. The Q- phase was chosen since it shows the largest quadrature error in Fig. 18(b). The simulations show that the largest quadrature phase error is 4° , when both n- and pMOS are slow. For all other simulated corners the error is below 1.5° . It is worth noticing that the quadrature errors for the corners are in the same order as the speed (\uparrow), current (\uparrow), and threshold (\downarrow) for the corners, that is high speed results in low quadrature error and vice versa.

The statistical simulations were performed by changing the length and width of each transistor and each capacitance of the filter randomly. The physical dimensions of the transistor was changed by $\pm 10\%$ of its minimum feature size, e.g.

Table 1 Corner parameters, variation relative to tt

	pMOS (%)	nMOS (%)		pMOS (%)	nMOS (%)		
ss	V_T	22	18	sf	V_T	-11	9
	I_{dsat}	-24	-15		I_{dsat}	8	-7
	f_T	-22	-19		f_T	10	-11
fs	V_T	11	-10	ff	V_T	-22	-19
	I_{dsat}	-14	7		I_{dsat}	18	16
	f_T	-14	8		f_T	19	15

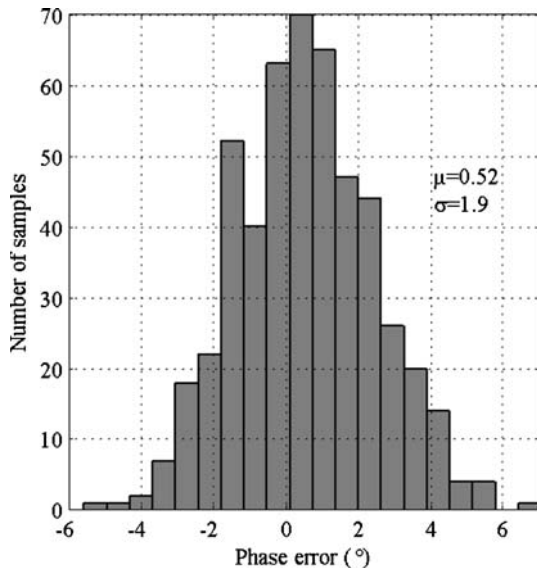


Fig. 23 Statistical simulation of the active polyphase filter at 10 GHz. Input amplitude 600 mV and 500 runs. Uniform distribution used

$$L = L_{nom} + Rand \cdot L_{min}, \tag{14}$$

where *Rand* is a rectangular distributed from -0.1 to 0.1 and L_{nom} is the desired value. The filter capacitances were altered $\pm 10\%$ in the same manner. This can be considered rather conservative, as with good layout optimized for matching the standard deviation should not exceed a few %. A run of 500 simulations was performed at 10 GHz with input amplitude of {400, 500, 600} mV. The mean phase error, μ , was $\{-0.1, 0.1, 0.5\}$ degrees with an associated standard deviation, σ , of $\{1.91, 1.99, 1.90\}$ degrees. In Fig. 23 the phase error distribution is plotted.

A comparison to the passive polyphase filter counterpart was made by varying the capacitance and resistance by $\pm 10\%$. The mean phase error was 0 degrees with an associated standard deviation of 3.8° .

5.2 Supply voltage variation

The supply voltage was changed from 0.8 V to 1.8 V for four different input amplitudes at 10 GHz (Fig. 24) to investigate the quadrature sensitivity.

For small input amplitudes the filter needs almost 1.2 V supply³ to achieve quadrature output. As the input amplitude increases also the supply variation can increase without penalty in quadrature error. With 400 mV input amplitude the supply can be down to 1 V.

³ The datapoints where the filter was not producing quadrature output have been cut out of the figure.

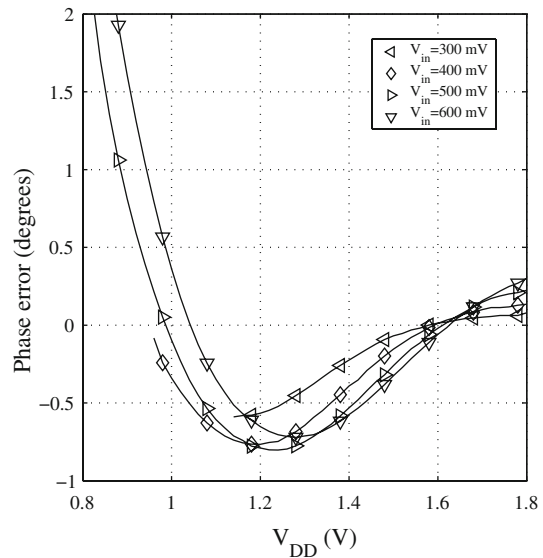


Fig. 24 Supply voltage variation of the active polyphase filter at 10 GHz

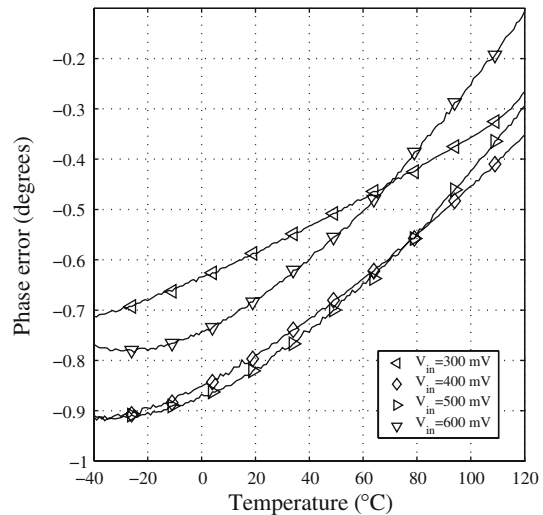


Fig. 25 Temperature dependence of the phase error at 10 GHz

5.3 Temperature variation

A temperature sweep from -40 to 120°C was performed with four different input amplitudes at 10 GHz and 1.2 V supply, see Fig. 25. The temperature variation does not significantly affect the quadrature phase error. It changes by no more than 0.7° over the full temperature range.

6 Conclusion

A high frequency active polyphase filter has been investigated through model and transistor simulations. The filter uses transconductors instead of resistors as in a passive polyphase filter. When a transconductor is used the input

impedance is larger and the filter can amplify the signal. In the simulations the transconductor was a CMOS inverter with a local bias feedback.

Simulations show a robust filter over wide frequency range (6–14 GHz) with an output quadrature error less than 1° for stable input amplitudes. The filter also shows robustness against input differential phase error and inverter delay. The potential of the technique has been demonstrated using the concept of effective capacitance. This indicates that high frequency filters can be realized with low power consumption. Corner simulations have been performed at 10 GHz, and for both n- and pMOS slow the phase error is below 4° , but for all other corners the error is less than 1.5° . The simulated far out phase noise is below that of the corresponding passive filter.

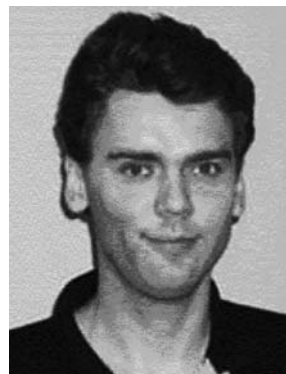
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Johan Wernechag received the M.Sc. degree in Electrical Engineering from Lund University, Lund, Sweden in December 2002. He is currently a Ph.D. student at the Analogue/RF Group at Lund University, working towards the Ph.D. degree. His research interests include design of beam steering transmitters for WLAN/WPAN networks aiming at the frequency band round 60 GHz (IEEE P802.15), automotive radar, and quadrature generation. During the years 1998–2003 he was a part-time teaching assistant at the Dept. of Physics, Lund University and since 2003 at the Department of Electrical and Information Technology (former Electrosience), Lund University.



Henrik Sjöland received the M.S. degree in Electrical Engineering and the Ph.D. in Applied Electronics from Lund University, Lund, Sweden, in 1994 and 1997, respectively. He is a Professor in Analog Circuit Design at Lund University. His research interests include the design and analysis of analog integrated circuits, feedback amplifiers, and RF CMOS. In 1999, he spent 1 year as a Fulbright Postdoctoral with the Abidi group at UCLA. He is the author of *Highly Linear Integrated Wideband Amplifiers* (Boston, MA: Kluwer, 1999).