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Novel multiple-selected and multiple-valued memory design using negative differential resistance circuits suitable for standard SiGe-based BiCMOS process

Kwang-Jow Gan · Cher-Shiung Tsai · Dong-Shong Liang

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Abstract A novel multiple-selected and multiple-valued memory (MSMVM) design using the negative differential resistance (NDR) circuits is demonstrated. The NDR circuits are made of Si-based metal-oxide-semiconductor field-effect-transistor (MOS) and SiGe-based heterojunction bipolar transistor (HBT). During suitably designing the parameters and connecting three MOS–HBT–NDR circuits, we can obtain the three-peak current–voltage (I–V) curves with different peak currents in the combined I–V characteristics. For the traditional resonant-tunneling-diode (RTD) memory circuit, one can only obtain four-valued memory states using a constant current source to bias the three-peak NDR circuit. However in this paper, we utilize two switch-controlled current sources to bias the three-peak NDR circuit at different current levels. By controlling the switches on and off alternatively, we can obtain the four-valued, three-valued, two-valued, and one-valued memory levels under the four different conditions. Our design is based on the standard 0.35 μm SiGe BiCMOS process.

Keywords Multiple-selected and multiple-valued memory · Negative differential resistance circuits · SiGe BiCMOS

K.-J. Gan (✉) · C.-S. Tsai · D.-S. Liang
Department of Electronic Engineering and Nano Technology Research and Development Center, Kun Shan University, 949 Da-Wan Rd, Yung-Kang City, Tainan County 710, Taiwan, ROC
e-mail: gankj@ms52.hinet.net

1 Introduction

The negative differential resistance (NDR) devices and circuits have been widely studied in many applications including the logic circuit [1–3], memory circuit [4–7], oscillator [8], analog-to-digital converter [9], frequency divider [10, 11], flip-flop circuit [12, 13], delta sigma modulator [14], and cellular neural network [15]. Especially the multiple-peak NDR circuit is a suitable element to apply to the multiple-valued memory (MVM). That is because the folded current–voltage (I–V) characteristics can greatly reduce the circuit complexity and enhance the functionality. The MVM provides lots of simplifying opportunities for implementation of sophisticated algorithms in computational process than traditional binary logic. It can offer more compact solutions for these problems and better functional capabilities in information process. Most of the NDR-based multi-valued memory circuits are utilized the resonant tunneling diode (RTD) as the basic device. The RTD is made of compound semiconductor, so the fabrication process is complicated and the cost is expensive in comparison with the standard CMOS or BiCMOS process. Besides, the RTD is difficult to combine with other devices and circuits to achieve the system-on-a-chip (SoC).

In this paper, we first demonstrate a novel NDR circuit that is composed of metal-oxide-semiconductor field-effect-transistor (MOS) and heterojunction bipolar transistor (HBT). The major advantage of this MOS–HBT–NDR circuit is that we can combine it with other standard Si-based or SiGe-based devices in applications. Then we connect three MOS–HBT–NDR circuits in cascode structure to obtain three-peak I–V characteristics. Compared to the traditional multiple-valued memory design, we can use a constant current source to bias the three-peak I–V

characteristics and obtain four stable states at the output. However in this paper, we utilize two switch-controlled constant current sources to bias the three-peak NDR circuit at different current levels. By controlling the switches on and off alternatively, we can totally obtain ten stable states at the output. We regarded this novel circuit as multiple-selected and multiple-valued memory (MSMVM) structure. This circuit can be applied to the one-input four-valued and two-input ten-valued logic gates. Certainly, we can use this MSMVM to design the multiple-valued multiplexer, counter, and memory array. In addition, there are two gates to control the path of the load current sources. The data-path logic can provide many variations and conveniences from MVM. Although this MSMVM consumes too much power, the advantage of this circuit is that we can implement it by the standard 0.35 μm SiGe BiCMOS process. It might provide much convenience in the NDR-based applications, and the power dissipation can be further reduction by upgrading the process.

2 MOS–HBT–NDR circuit

The basic MOS–HBT–NDR circuit is shown in Fig. 1(a), which is made of three Si-based n-channel MOS and one SiGe-based HBT devices. This circuit is derived from a Λ-type topology described in Refs. [16, 17]. By suitably designing the MOS width/length (W/L) parameters, we can obtain the HSPICE simulated I–V curve with the NDR characteristic, as shown in Fig. 1(b). The parameters are $W_{MN1} = 2$ μm, $W_{MN2} = 50$ μm, $W_{MN3} = 15$ μm, and $L_{MN1,2,3} = 0.35$ μm. The magnitude of the Vgg value is 3 V. The HBT is used the ln02 cell based on the standard 0.35 μm SiGe BiCMOS process provided by the TSMC foundry.

The segment resistance of the I–V characteristic can be distinguished with three regions defined as the first positive differential resistance (PDR) region, the NDR region, and the second PDR region in order. When a fixed voltage Vgg is applied to this circuit, and we increase the bias V_S gradually, the operating condition for the first PDR region can be described as MN1 is saturated, MN2 is cutoff, HBT is saturated, and MN3 is cutoff. The NDR region indicates the case as MN1 is saturated, MN2 is saturated, HBT is active, and MN3 is saturated. The second PDR region expresses the state as MN1 is saturated, MN2 is linear, HBT1 is cutoff, and MN3 is saturated.

We can obtain various I–V characteristics by modulating the parameters with (a) W_{MN1}, (b) W_{MN2}, (c) W_{MN3}, and (d) Vgg, as shown in Fig. 2, respectively. Notice that, the cut-in voltage is not located at zero voltage. It is because the initial operating state for the HBT device is saturated. So there exists a reverse current back to the V_S terminal. The magnitude of the cut-in voltage is determined by the parameters of the circuit.

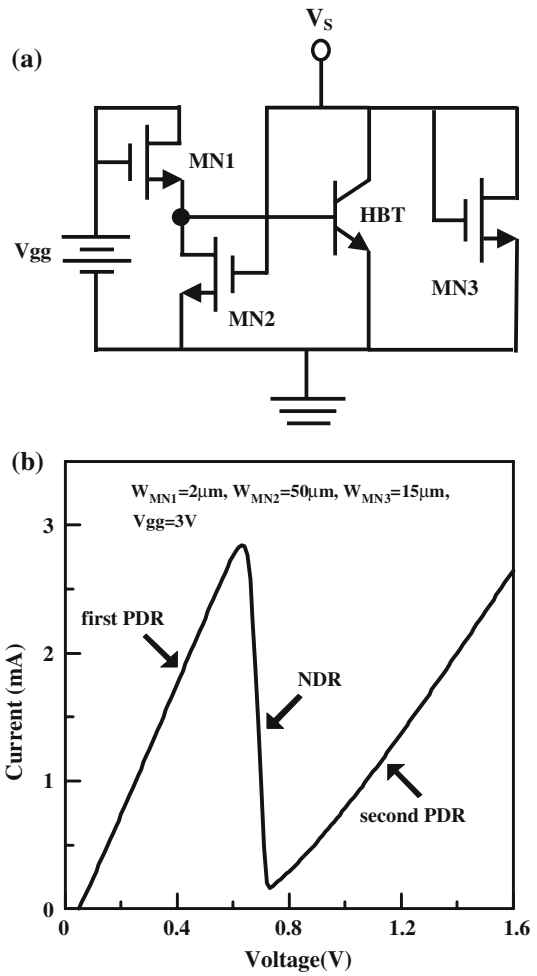


Fig. 1 (**a**) The configuration of the MOS–HBT–NDR circuit. (**b**) The simulated I–V curve of the NDR circuit by modulating the Vgg as 2.7, 3, and 3.3 V, respectively

As shown, this MOS–HBT–NDR circuit has a wide range of adjustable I–V characteristics. Even if this MOS-HBT-NDR circuit has been taped-out, we also can modulate the peak currents by changing the Vgg values, as those shown in Fig. 2(d). The combined current is dominated by the collector current of the HBT and the drain current of MN3. Therefore, the power dissipation of the NDR circuit is dependent on the magnitude of the bias V_S and the combined current. This power dissipation can be reduced by further decreasing the width of MN2. In addition, we can control the magnitude of the peak currents, so the power consumption can be reduced by decreasing the Vgg values.

Compared to the RTD, this MOS–HBT–NDR circuit has advantages in terms of easy control and fabrication by the standard SiGe-based BiCMOS process. Especially, it is much easier to obtain the multiple-peak NDR circuit by

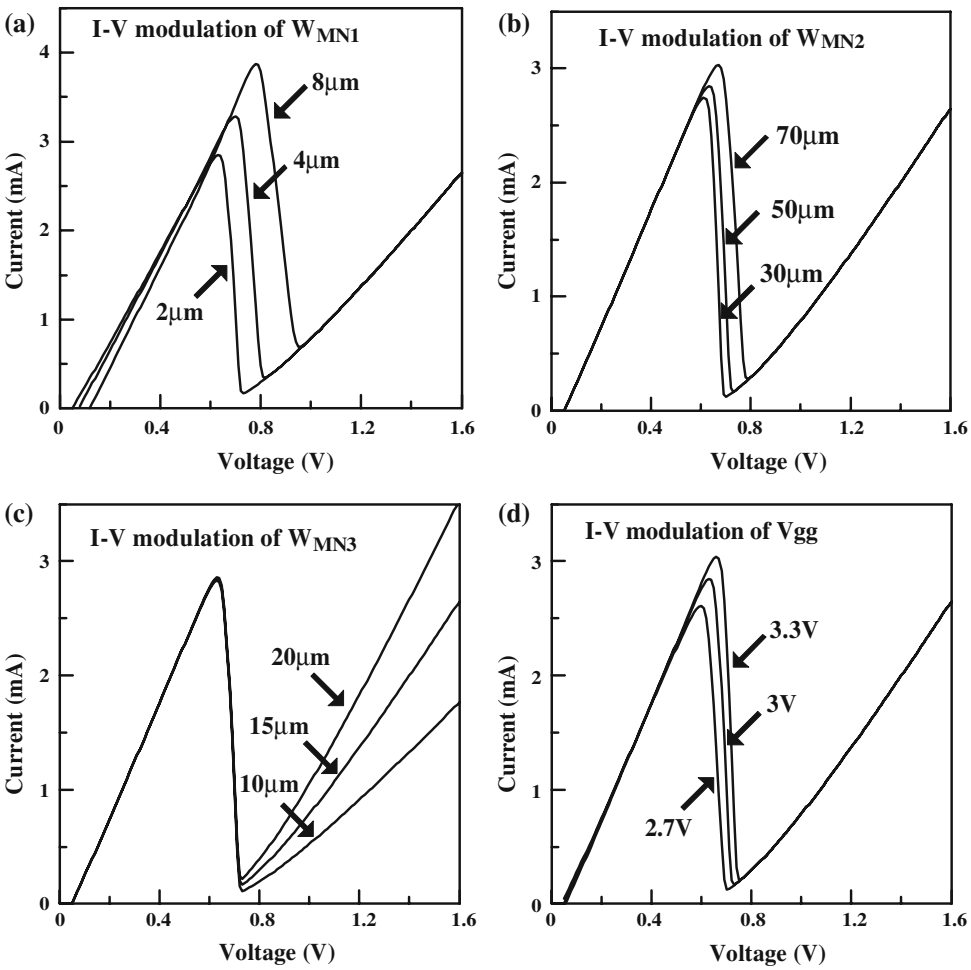


Fig. 2 The simulated I–V characteristics by modulating the (**a**) W_{MN1}, (**b**) W_{MN2}, (**c**) W_{MN3}, and (**d**) Vgg values, respectively

series-connected or parallel-connected MOS–HBT–NDR circuits.

3 Memory circuit design

The novel MSMVM circuit using three-peak MOS–HBT–NDR circuit as the driver and two constant current sources as the load is shown in Fig. 3. The parameters for the circuits are designed as $W_{MN11} = 1$ μm, $W_{MN12} = 80$ μm, $W_{MN13} = 50$ μm, Vgg1 = 2.5 V, $W_{MN21} = 1$ μm, $W_{MN22} = 80$ μm, $W_{MN23} = 50$ μm, Vgg2 = 2.4 V, $W_{MN31} = 1$ μm, $W_{MN32} = 80$ μm, $W_{MN33} = 15$ μm, and Vgg3 = 1.9 V. The lengths of all MOS are 0.35 μm. The bias voltage Vs is 3.3 V. Figure 4 shows the three combined I–V curves under three different groups of Vgg values.

Two gates C1 and C2 are used to control the path of the current sources I1 and I2, respectively, which can bias the three-peak MOS-HBT-NDR circuit at suitable operating points. Figure 5 shows the load-line analysis of this MSMVM. Referring to the current I1, it can intersect the PDR segments of the three-peak I–V curve with four stable operating points from Q1 to Q4. The current I2 can intersect the combined I–V curve with three stable operating points from Q5 to Q7. If both current I1 and I2 pass through the NDR circuit simultaneously, we can obtain two stable operating points Q8 and Q9. If there is no current passing through the NDR circuit, we can obtain an operating point Q0. It means that there are multiple selections of the load current path by controlling C1 and C2 on or off in this memory circuit. Compared to traditional three-peak RTD-based memory circuit, we can obtain only four stable states under the load-line I1. However we can obtain more stable states at the output in this MSMVM circuit.

The input voltage Vin provides and controls the voltage at the three-peak MOS–HBT–NDR node by controlling the write clock on and off. Figure 6 shows the waveform of write clock and Vin signal. A saw-tooth wave is applied to the input with amplitude of 3.8 V. The voltage to be stored is provided by Vin signal and loaded to the main circuit by enabling the write clock in order. We use a square wave as the write clock that can alternately turn the MN1-MOS on and off. When the write clock is from on to off state, the voltage across the three-peak MOS–HBT–NDR circuit will be modulated to the nearest stable operating point.

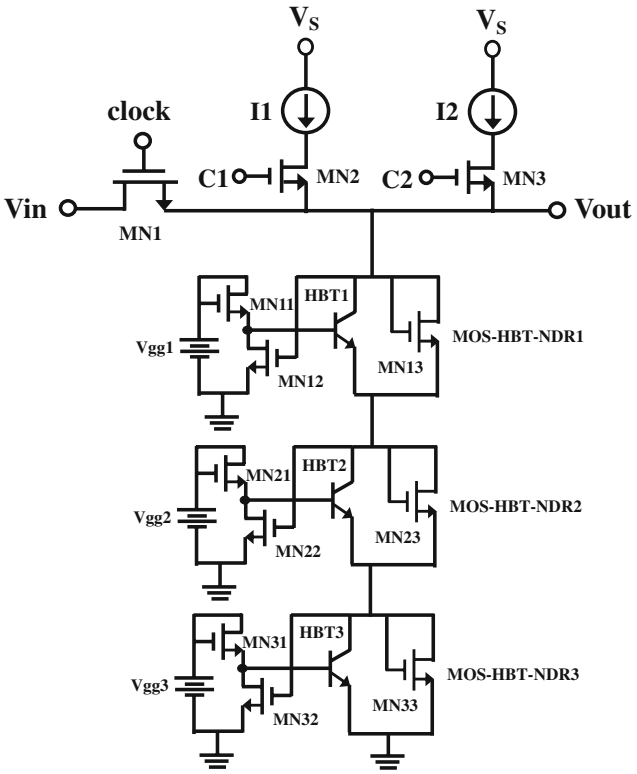


Fig. 3 The circuit configuration of the novel multiple-selected and multiple-valued memory (MSMVM)

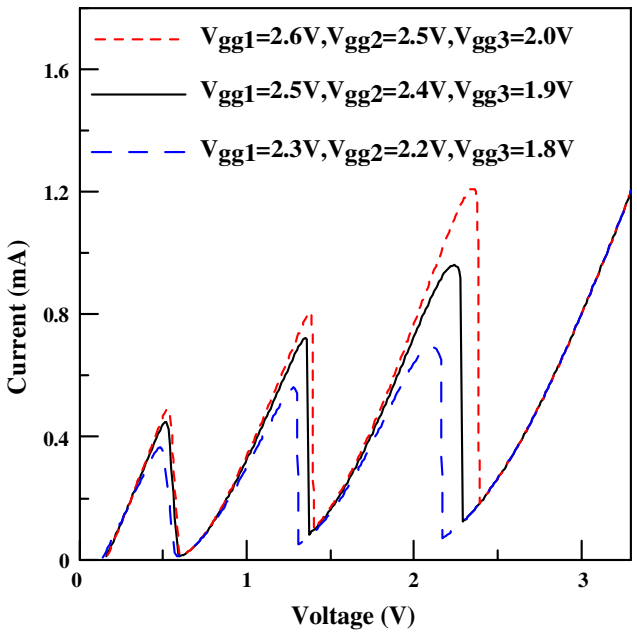


Fig. 4 Three combined I–V curves under three different groups of Vgg values

Therefore, the corresponding voltage level will be transferred to the output terminal in sequence.

The on and off sequences of the C1 and C2 are shown in Fig. 7. The state "1" means the load current can pass

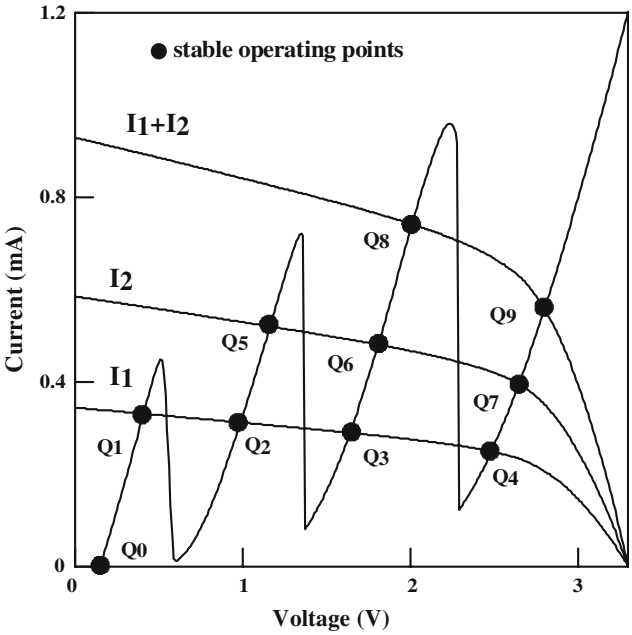


Fig. 5 The load-line analysis for the MSMVM circuit. We can obtain ten operating points from Q0 to Q9 which is dependent on the controlled conditions of load current

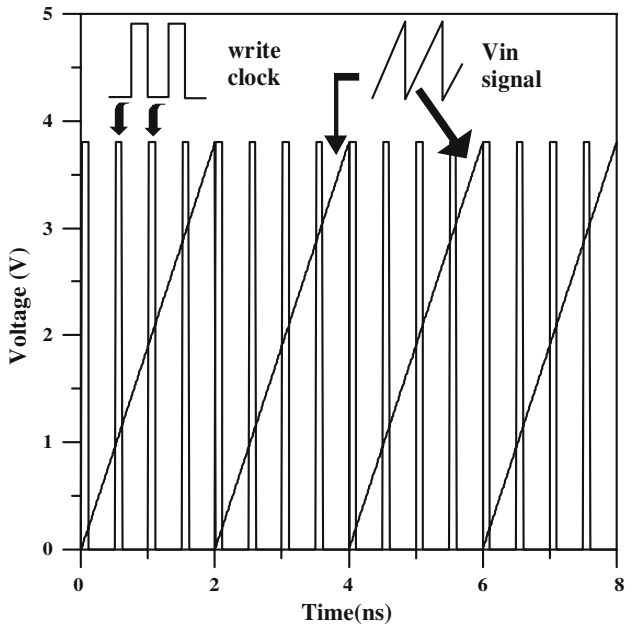


Fig. 6 The waveform of the write clock and Vin signal for the MSMVM circuit

through the NDR circuit. The simulated results of this MSMVM are shown in Fig. 8. The stable states from V0 to V9 are the corresponding voltage levels with respect to the operating points from Q0 to Q9, respectively. When both of two gates C1 and C2 turn on, we can obtain two voltage levels V8 and V9. When C1 turns off and C2 on, there are three voltage levels from V5 to V7. Similarly, When C1

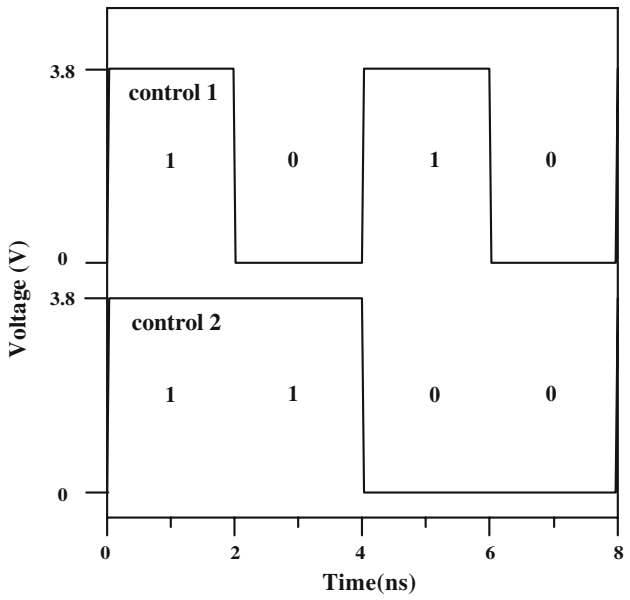


Fig. 7 The on and off sequences of the C1 and C2 gates

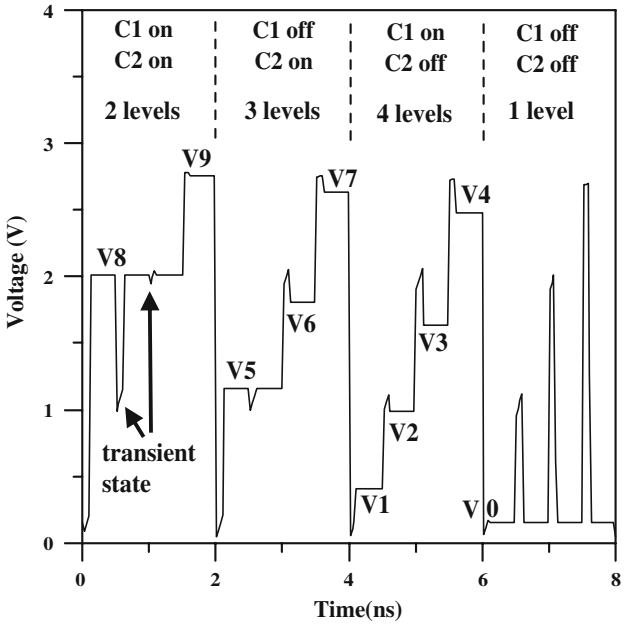
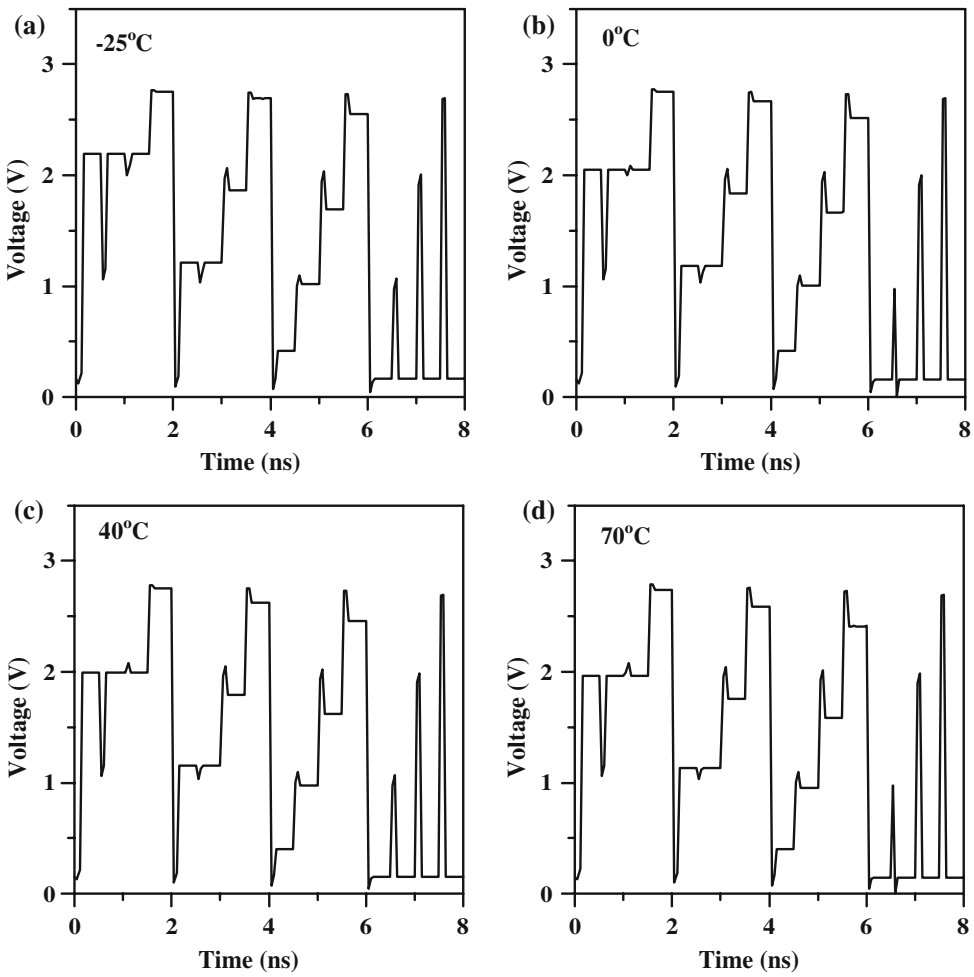


Fig. 8 Simulated results for the MSMVM under different conditions

Fig. 9 Simulated results under different temperature



turns on and C2 off, there are four voltage levels from V1 to V4. When both C1 and C2 turn off, there is only one state V0 which is the cut-in voltage of the three-peak MOS–HBT–NDR circuit. Therefore the output of the MSMVM circuit gives totally ten memory states. Those values are V0 = 0.13 V, V1 = 0.41 V, V2 = 0.98 V, V3 = 1.64 V, V4 = 2.48 V, V5 = 1.16 V, V6 = 1.81 V, V7 = 2.64 V, V8 = 2.01 V, and V9 = 2.76 V, respectively.

The agreement between the load-line analysis and simulated output is very good. Notice that there exists some voltage levels which are possessed of the same magnitude. It is because the voltage provided by the Vin signal is not large enough to drive the operating point from one stable state to another nearest stable state. The transfer from one stable state to another stable state will be occurred only when enough voltage is provided. Also, there exists the transient state between the stable states. That is resulted from the write clock pulse.

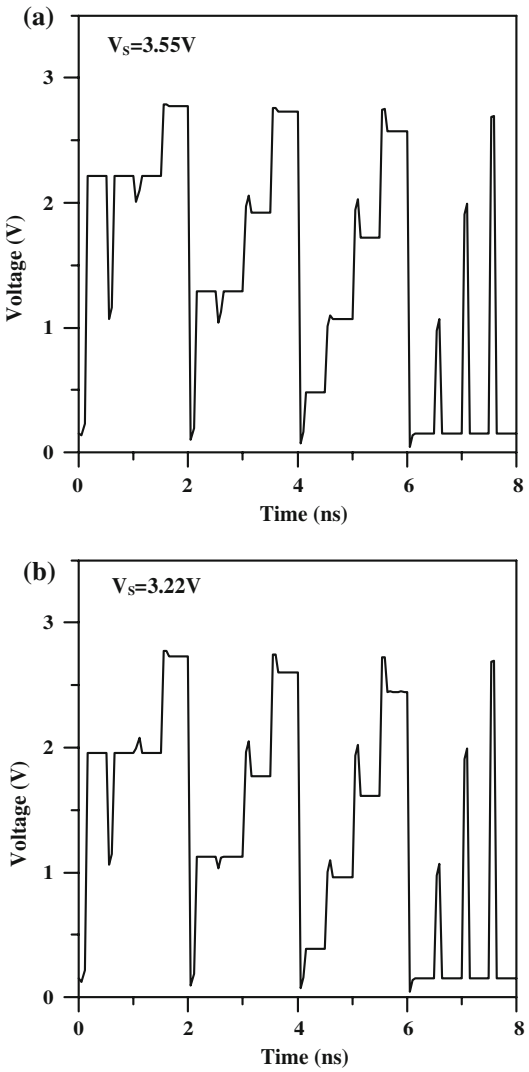


Fig. 10 Simulated results under different bias Vs

Figure 9 shows the simulated results under different temperature −25, 0, 40, and 70°C, respectively. As shown, this MSMVM is stable for temperature. We also show the simulated results in Fig. 10 under different Vs as 3.55, and 3.22 V, respectively. The magnitude of Vs will affect the load-line I1 and I2. Therefore, the voltage levels have a small deviation compared to the results shown in Fig. 8.

4 Conclusions

Compared to the traditional N-peak NDR I–V characteristics, one can at most obtained N + 1 stable states of memory circuit. However we propose this novel MOS–HBT–NDR-based MSMVM circuit using two switch-controlled current sources as the load. We can obtain ten stable states for this memory circuit under a whole circle of switch on and off. It is worth investigating to obtain the ten states from small to large stable levels step by step by further controlling the write clock, input signal and load currents for this MSMVM circuit. Furthermore, the fabrication of this MSMVM circuit can be implemented by the standard SiGe-based BiCMOS technique, which is the major advantage in comparison with the RTD-based memory circuit.

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Kwang-Jow Gan was born in Tainan, Taiwan (ROC), on March 9, 1966. He received the B.Sc. and M.Sc. degrees in the department of electrical engineering of National Cheng Kung University of Taiwan, in 1988 and 1990, respectively, and the Ph. D. degree from 1992 to 1997 at the same department and university. In August 1992 he joined the Department of Electronic Engineering, Kun Shan University, Tainan, Taiwan (ROC), where he is currently a Professor. His research interests include nano material and device, ULSI technique and process, ULSI design, computer-aided design software, nonlinear circuit analysis, novel negative differential resistance circuit analysis and application, multiple-valued logic design, signal processing and cellular neural network.

Cher-Shiung Tsai was born in Tainan, Taiwan (ROC), on January 17, 1955. He received the B.Sc. in the department of electronics engineering of National Chiao Tung University of Taiwan in 1978 and received M.Sc. degrees in the department of electrical engineering of National Cheng Kung University of Taiwan in 1987. He had been a process, assembly and QC engineer on power transistor company (MOSPEC) for almost four years. He also was been a consumer IC designer in Wind Bond and HMC companies for four and half years more. His IC design included clock, timer, PC computer real time clock, melody and speech. In August 1992 he joined the Department of Electronic Engineering, Kun Shan University, Tainan, Taiwan (ROC), where he is currently a assistant Professor. His research interests include VCO, PLL, ULSI technique and process, ULSI design, nonlinear circuit analysis, novel negative differential resistance circuit analysis and application.

Dong-Shong Liang was born in Kaohsiung, Taiwan (ROC), on Nov. 25, 1949. He received the M.S. degrees in the department of electronic engineering of Monmouth University of New Jersey U.S.A. In August 1991 he joined the Department of Electronic Engineering, Kun Shan University, Tainan, Taiwan (ROC), where he is currently a Lecturer. His research interests include VLSI technique and process, novel negative differential resistance circuit analysis and application, embedded system design, microprocessor system design and cellular neural network.