A CMOS digitally programmable filter technique for VLSI applications

Hussain Abdullah Alzaher

Abstract A novel technique for designing analog CMOS integrated filters is proposed. The technique uses digitally controlled current amplifiers (DCCAs) to provide precise frequency and/or gain characteristics that can be digitally tuned over a wide range. This paper provides an overview of the possibilities of using the DCCA as the core element in programmable filters. In mixed analog/digital systems, the digital tuning feature of the proposed approach allows direct interfacing with the digital signal processing (DSP) part. Basic building blocks such as digitally programmable amplifiers, integrators, and simulated active inductors are given. Systematic designs of second-order filters are presented. Fully differential architectures of the proposed circuits are developed. Experimental results obtained from 0.5 μm standard CMOS chips are provided.

Keywords CMOS mixed analog/digital systems · Current-mode circuits · Active filters · Variable gain amplifiers

1 Introduction

Active-RC filters based on the operational amplifier (op-amp) exhibit high linearity. However, the constant gain-bandwidth product of the op-amp limits their frequency range and the lack of programmability restricts them to discrete applications. Tuning properties are essential for analog integrated circuit filtering techniques to compensate

H. A. Alzaher (✉)
Electrical Engineering, King Fahd University of Petroleum
& Minerals, P.O. Box 1225, Dhahran 31261,
Eastern Province, Saudi Arabia
e-mail: alzaherh@kfupm.edu.sa

for process, component and temperature variations as integrated RC time constants can vary by as much as 50% [1]. Transconductance (gm) circuits are programmable and can operate at high frequencies. However, their linearity and tuning range are poor particularly at low supply levels [2]. The MOSFET-C approach provides wide tuning range [3] but it suffers from poor linearity and limited bandwidth. In addition, linearization techniques of MOSFET-C and gm-C circuits assume the classical MOS transfer characteristics in saturation or triode region. In submicron technologies, the second order effects such as short-channel and mobility degradation become significantly important, further degrading the linearity of these circuits. Switched capacitor (SC) filters exhibit high linearity and accurate frequency response; however, their frequency operation range is limited since they need to operate at sampling frequencies much greater than the signal bandwidths.

On the other hand, the current-mode approach of designing analog integrated circuits shows promising characteristics. This stems from its wide frequency operating range, high slew rate and simple circuitry [4, 5]. Recently, design of current and voltage-mode filters based on current followers and/or voltage buffers (VBs) such as [6–10] has been of growing interest due to their inherent large bandwidth, high linearity, and low power consumption. However, there are two major limitations associated with this approach, which hinder its use in analog integrated circuits. The first is the absence of the programmability feature and the second is the lack of providing fully differential structures with accurate common mode signal level control. In this work, programmability is introduced through varying the gain of the current amplifier and the extension to fully differential architectures is developed. Thus, the proposed technique is expected to become a fundamental analog filtering

approach in future. This paves the way for the proposed circuits to be used in high-performance analog and mixed-signal ICs where fully differential signal paths are incorporated. Fully differential architectures are essential to enhance the performance of mixed analog/digital systems in terms of supply noise rejection, dynamic range and harmonic distortion and to reduce the effect of coupling between various blocks [11].

More recently, digitally programmable devices such as those in [12–14] have become attractive for mixed digital-analog applications. Traditionally, resistor and/or capacitor matrices can be used to provide tuning to analog circuits. However, they require relatively large area which typically limits the tuning accuracy to five bits or 3% of the nominal values. The proposed technique uses digitally controlled current amplifiers (DCCAs) which comprise the current division network (CDN) [15] to provide digital tuning of DCCA gains. The CDN is inherently linear (i.e. insensitive to second order effects and valid in all MOS operating regions). Moreover, the CDN can be digitally trimmed up to 10 bits accuracy without component spreading [16]. The gains of the DCCA is utilized to provide precise frequency and/or gain characteristics that can be tuned over a wide range. Polysilicon resistors and capacitors are used to realize the filter time constants, which results in highly linear filters. In mixed analog/digital systems, the digital tuning feature of the proposed approach allows direct interfacing with the digital signal processing (DSP) part. DSP, available in most modern systems, is utilized to adapt the filter parameters with minimum additional hardware. The DSP is utilized to program the filter to operate at different bandwidths and/or different gain settings. A good example of the proposed technique is the design of an analog baseband chain for multi-standard wireless receivers [17]. In addition, digital automatic frequency tuning scheme such as that described in [18] can be employed to compensate for both components and temperature variations. The DSP tuning scheme avoids the feedthrough problems associated with the real time master-slave tuning approach which limits system dynamic ranges. A conceptual block diagram of digital automatic tuning is depicted in Fig. 1. Digital tuning feature eliminates the use of auxiliary digital to analog converters from the DSP to the analog filters resulting in simplified, flexible and low power system design solutions.

The following section discusses the design and implementation of the building blocks. Section 3 presents some basic applications such as amplifiers, integrators, and simulated active inductances. Several new digitally programmable filters are presented in Sect. 4 where a systematic design procedure to convert well-known active-RC circuits to their DCCA-RC counterparts is described. The development of fully differential architectures of the proposed approach is discussed in Sect. 5.
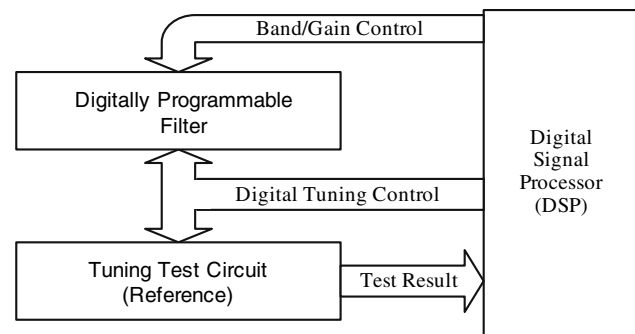
Fig. 1 Digitally programmable mixed signal system

2 Monolithic CMOS integration

A current follower (CF) is a two terminal device which transfers current signal from a low impedance input terminal to a high impedance output terminal. The DCCA is basically a CF with programmable gain that can be controlled digitally. The DCCA can be described by the following matrix equation:

$$\begin{bmatrix} I_z \\ V_x \end{bmatrix} = \begin{bmatrix} 0 & \pm\alpha \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_x \end{bmatrix}, \tag{1}$$

where α represents the current gain of the DCCA and the signs denote the positive (both currents are going in) and negative (one current is going in and the other is out) DCCA. The proposed DCCA with two outputs is shown in Fig. 2. When the CDN is replaced by a short circuit, the DCCA reduces to a unity gain CF. Its operation can be explained as follows. Transistors M1 and M2 provide the required virtual ground needed at the input port X. This is achieved by forcing equal currents in both transistors. Hence, their source potentials will be equal since they share the same gate, provided they operate in saturation region. Since the transconductance of a MOS transistor is small compared to a bipolar transistor, an internal feedback (M6) is incorporated to achieve low input impedance at the X terminal. The feedback reduces the input impedance by the amount of feedback yielding:

$$r_x \approx \frac{1}{g_{m2}(1 + g_{m6}(r_{ds2}//r_{ds5}))} \tag{2}$$

where g_m and r_{ds} are the transconductance and the output resistance of the MOSFET, respectively. Furthermore, the feedback reduces the distortion but sacrifices some of the bandwidth. The input current I_x, which is forced by the constant currents of M2 and M12 to flow into M6, is conveyed to the output port Z_p by current copying transistor M7. Cross-coupled current mirrors are used to change the polarity of the current and pass it to port Z_n.

The operation of the CDN is similar to that of the R-2R ladder and was explained in [17]. The proper operation of the CDN requires the input node to be current driven while
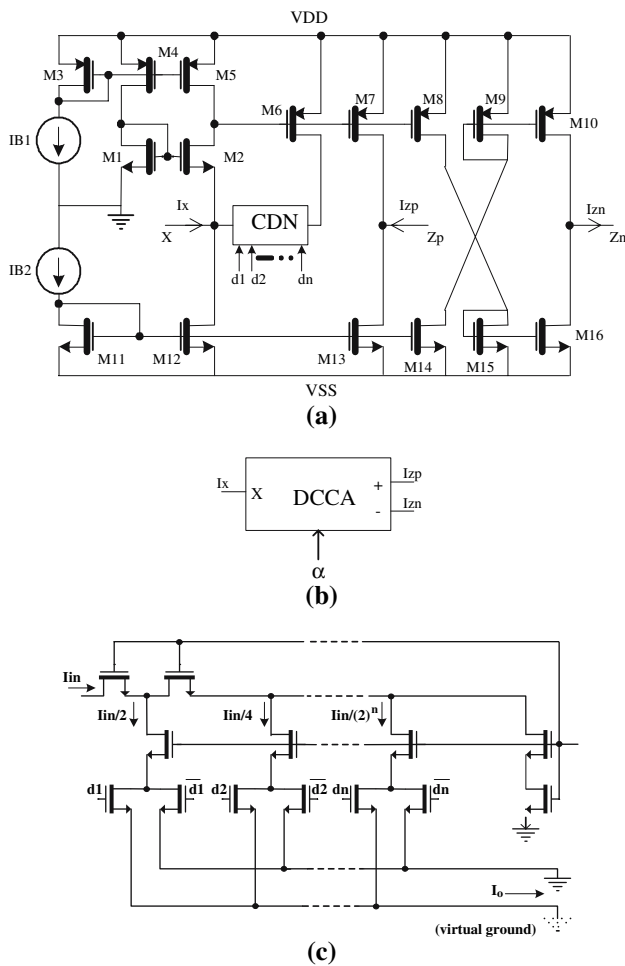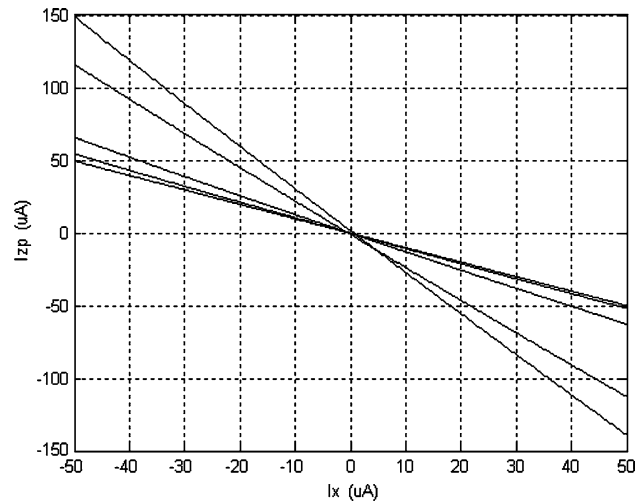
Fig. 2 Compound digitally controlled current amplifier (DCCA): (**a**) CMOS implementation (**b**) Symbol (**c**) The current division network [16].

Fig. 3 Measured DC characteristics of the DCCA showing several gain settings

the output node to be virtually grounded. In the proposed DCCA, the CDN is driven by the drain current of M6 while its outputs I_o is connected to the virtual ground node X. The current at terminal X (I_x) is provided by the output current of the CDN (I_o) while the negative feedback loop adjusts the current amplifier output (I_z) to be equal to the CDN input (I_{in}). Therefore, the transfer current characteristic of the DCCA becomes:

$$I_Z = \alpha I_X \text{ with } \alpha = 1/\sum_{i=1}^{n} d_i 2^{-i} \tag{3}$$

where d_i is the ith digital bit and n is the size of control word.

The input port virtual ground property of the DCCA facilitates the addition of different signals. But low output impedance VBs are needed to allow the distribution of output signal to several subcircuits. Adoption of VBs along with DCCAs simplifies the design of various signal processing voltage and current-mode circuits. Folded-cascode op-amps, which enjoy high speed, are used to implement

the VBs. DCCAs using 6-bit CDNs and the VBs have been fabricated in a 0.5 μm N-well CMOS process. The operation of the proposed DCCA and VB were experimentally verified. Throughout the testing, the supply voltages were set to ±1.6 V and the currents of the DCCA and VB were 600 and 300 μA, respectively. Figure 3 shows the dc current transfer characteristics of the DCCA under several different gain settings. The measured −3 dB bandwidth is more than 40 MHz for the different gain setting. Similarly, the measured ac response of the VB shows a bandwidth exceeding 40 MHz. Measurement results are limited by the maximum frequency that can be measured using the available network analyzer. However, post layout simulation results show that the bandwidth of the DCCF is more than 140 MHz. Also, the ac response of the VB shows a bandwidth exceeding 90 MHz.

3 Basic functions

This section presents several basic analog building blocks based on the proposed technique such as digitally programmable amplifiers, integrators, and active simulated inductors. The four basic amplifier types are shown in Fig. 4. These amplifiers exhibit wide bandwidths at different gain settings. The DCCA of Fig. 4(a) is itself a digitally controlled current amplifier with gain of $A_i = \alpha$. The voltage amplifier shown in Fig. 4(b) has a gain of $A_v = \alpha R_2/R_1$. The gain of transconductance amplifier shown in Fig. 4(c) is $G_T = \alpha/R$ while the gain of the transresistance amplifier of Fig. 4(d) is given by $R_T = \alpha R$.

Figure 5 shows ac responses of the voltage amplifier of Fig. 4(b) with 0-to-6 dB gain varied in step of 1 dB. It can be seen that the amplifier exhibits almost constant bandwidth independent of the gain.
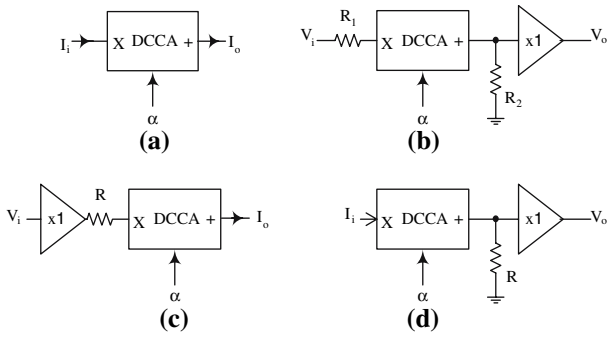
Fig. 4 The four different types of amplifiers: (**a**) current (**b**) voltage (**c**) transconductance (**d**) Transresistance
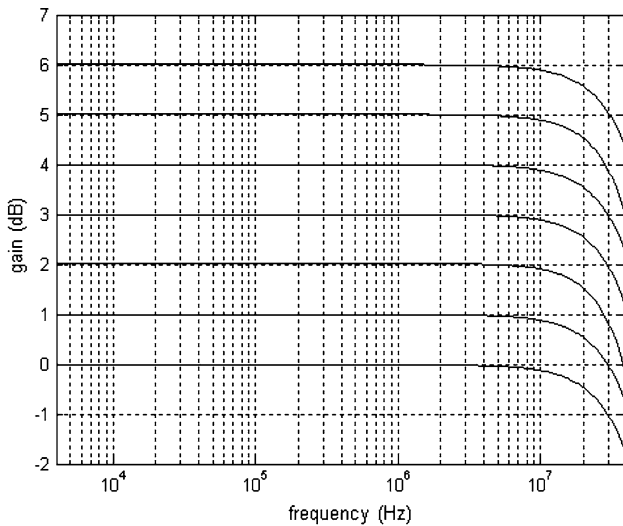
Fig. 5 Measured ac characteristics of the voltage amplifier of Fig. 4(b) showing several gain settings

Digitally programmable ideal and lossy integrators are shown in Fig. 6. The transfer function of the ideal integrator of Fig. 6(a) is given by:

$$\frac{V_o}{V_i} = -\frac{1}{sCR/\alpha}. \tag{4}$$

There are two realizations for the lossy integrator Fig. 6(b, c) with the following transfer functions, respectively:

$$\frac{V_o}{V_i} = -\frac{\alpha R_2/R_1}{1 + sCR_2}, \tag{5}$$

$$\frac{V_o}{V_i} = -\frac{R_2/R_1}{1 + sCR_2/\alpha}. \tag{6}$$

Although the first employs grounded resistors its time constant is not programmable. On the other hand, the second realization exhibits programmable time constant. A weighted summer circuit utilizing the virtual ground property of the DCCA is shown in Fig. 7. The output voltage is expressed as:
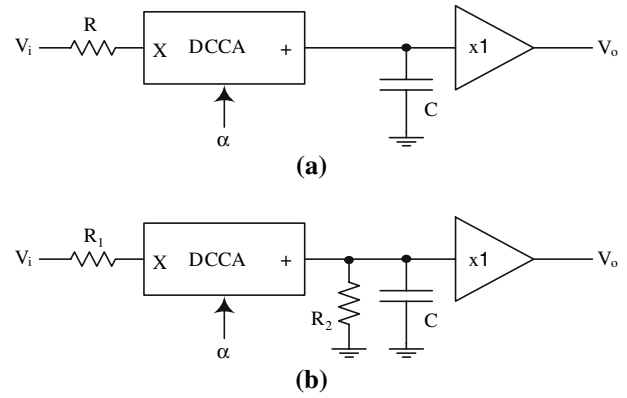
Fig. 6 Integrators: (**a**) ideal (**b**) lossy with grounded elements (**c**) lossy with programmable time constant
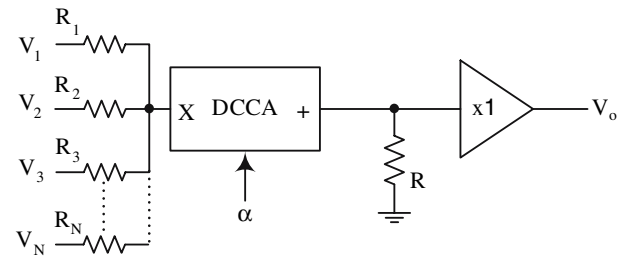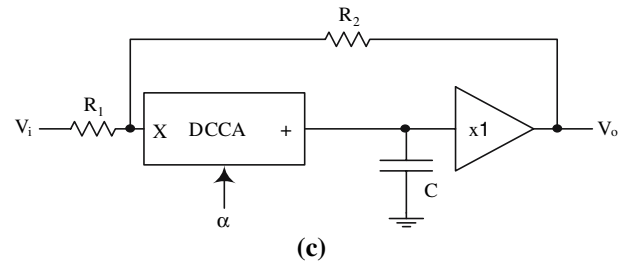

Fig. 7 Weighted summer

$$V_o = -\alpha R \sum_{i=1}^{N} \frac{V_i}{R_i}. \tag{7}$$

A digitally programmable negative impedance converter (NIC) is shown in Fig. 8. It is straightforward to show that the circuit input impedance is given by:

$$Z_i = -\frac{Z}{\alpha}. \tag{8}$$

When Z is a resistor (R), a negative resistor ($-R/\alpha$) is obtained. Actively simulated inductors can be used in several applications such as active filters, oscillator designs and cancellation of parasitic inductances. Various topologies of active inductors based on op-amps, nullors, current-feedback amplifiers and current conveyors can be found in the literature. However, such active-RC realizations rely on the inaccurate RC time constant to determine the inductance value. Using the proposed technique a digitally programmable active inductor can be implemented. The inductor is obtained from the basic circuit of Fig. 9(a)
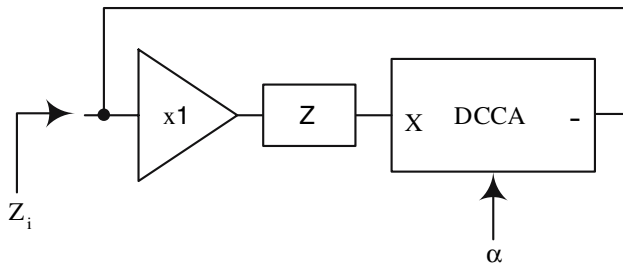
Fig. 8 Negative impedance converter (NIC)

consisting of a voltage mode integrator with infinite input impedance followed by voltage to current converter with its output fed-back to the input node. The proposed circuit of the lossless inductor is shown in Fig. 9(b). It can be shown that its input impedance is given by:

$$Z_i = \frac{sC_1R_1R_2}{\alpha_1\alpha_2}. \tag{9}$$

Obviously, the circuit simulates a lossless inductor with an inductance $L = C_1R_1R_2/(\alpha_1\alpha_2)$ Clearly, the inductance can be tuned digitally via α_1 and/or α_2. On the other hand, a negative lossless inductor can be obtained easily by changing the polarity of one of the DCCA. A lossy inductor with series resistance is shown in Fig. 9(c). The impedance of the circuit can be expressed as:
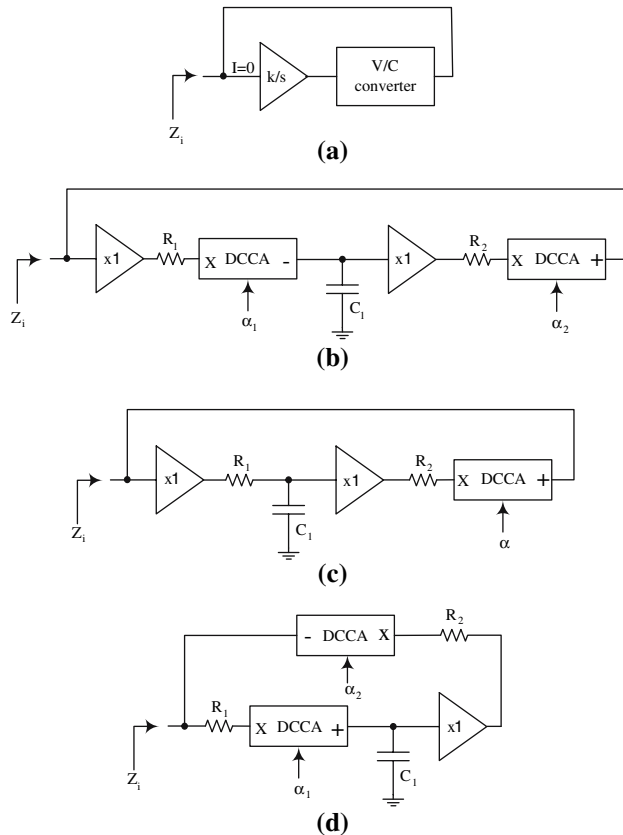
Fig. 9 Simulated inductors: (**a**) general circuit for lossless inductor (**b**) lossless L (**c**) series L-R (**d**) parallel L-R

$$Z_i = \frac{sC_1R_1R_2}{\alpha} + \frac{R_2}{\alpha}. \tag{10}$$

The circuit simulates a lossy inductor with $L = C_1R_1R_2/\alpha$ which can be digitally programmed via α. Similarly, by changing the polarity of the DCCA a negative inductor in series with a negative resistor can be obtained. A parallel lossy inductance circuit is shown in Fig. 9(d). Routine analysis shows that the input impedance is given by:

$$Z_i = R_1 // \frac{sC_1R_1R_2}{\alpha_1\alpha_2}. \tag{11}$$

4 Digitally programmable filters

Two systematic approaches of designing second-order digitally programmable active filters based on the proposed technique are presented. First, biquads filters obtained by substituting the inductor L in a LCR resonator with a circuit with inductive input impedance are provided. Second, filters obtained from their two-integrator loop active-RC counterparts are considered.

4.1 Simulated active inductance based filters

Class of active filters can be obtained using active simulated inductors. This approach has the advantage of realizing inherently very low sensitivity high-order networks directly. Also, the theory and design of passive RLC filter is well-developed with tables and design manuals that can be utilized for direct synthesis. It will be demonstrated that the proposed inductor of Fig. 9(b) exhibits several attractive features when used in filter designs. First, it can be used to provide both voltage and current-mode functions. Second, when it is used to design a bandpass filter an additional lowpass function is automatically provided. A second-order voltage mode LCR bandpass filter is shown in Fig. 10(a). It can be shown that by replacing the passive inductor by the proposed simulated inductor, as shown in Fig. 10(b), the circuit provides both bandpass and lowpass responses given by:
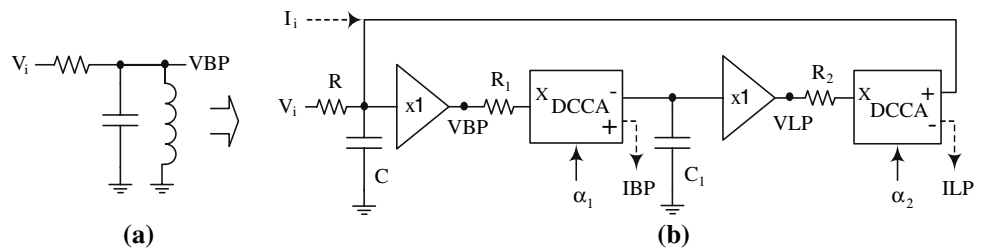
$$\frac{V_{BP}}{V_i} = \frac{s/(CR)}{s^2 + s/(CR) + \alpha_1\alpha_2/(CC_1R_1R_2)}, \tag{12}$$

$$\frac{V_{LP}}{V_i} = \frac{\alpha_1/(CC_1RR_1)}{s^2 + s/(CR) + \alpha_1\alpha_2/(CC_1R_1R_2)}. \tag{13}$$

It is worth mentioning that usually the lowpass biquad requires the simulation of a floating inductor, which is more difficult to design. It can be shown that the pole frequency (ω_o), bandwidth (ω_o/Q_o), and the quality factor (Q_o) are given by: $\omega_o = 1/\sqrt{LC} = \sqrt{\alpha_1\alpha_2/(CC_1R_1R_2)}$, $\omega_o/Q_o = 1/(CR)$ and $Q_o = R\sqrt{\alpha_1\alpha_2C/(C_1R_1R_2)}$. Clearly,

Fig. 10 Voltage and current-mode bandpass filter (a) LCR circuit (b) simulated circuit

(a)   **(b)**

center frequency can be tuned digitally using α_1 and/or α_2 without disturbing the bandwidth. Moreover, current mode bandpass and lowpass function can be realized using the same circuit by introducing an additional output current terminal to each of the DCCA and applying current input signal instead of the input voltage. The current transfer functions are given by:

$$\frac{I_{BP}}{I_i} = -\frac{s\alpha_1/(CR_1)}{s^2 + s/(CR) + \alpha_1\alpha_2/(CC_1R_1R_2)}, \quad (14)$$

$$\frac{I_{LP}}{I_i} = \frac{\alpha_1\alpha_2/(CC_1RR_1)}{s^2 + s/(CR) + \alpha_1\alpha_2/(CC_1R_1R_2)} \quad (15)$$

Figure 11 shows the bandpass magnitude responses of the voltage-mode filter while Fig. 12 shows the response of the current-mode lowpass filter where the corner frequencies are varied digitally by controlling both α_1 and α_2, simultaneously. The bandpass filter is tuned from approximately 200 kHz to 600 kHz whereas the tuning range of the lowpass filter corner frequency is from 500 kHz to 5 MHz.

A highpass biquad can be obtained using the passive LCR circuit of Fig. 13(a). Using the proposed parallel L-R inductor, the highpass filter of Fig. 13(b) is developed. Also, the circuit provides an additional bandpass function. The transfer functions are given by:

$$\frac{V_{HP}}{V_i} = \frac{s^2}{s^2 + s/(CR_1) + \alpha_1\alpha_2/(CC_1R_1R_2)}, \quad (16)$$

$$\frac{V_{BP}}{V_i} = -\frac{s\alpha_1/(C_1R_1)}{s^2 + s/(CR) + \alpha_1\alpha_2/(CC_1R_1R_2)}. \quad (17)$$

The filter parameters are given by:$\omega_o = \sqrt{\alpha_1\alpha_2/(CC_1R_1R_2)}$, $\omega_o/Q_o = 1/(CR_1)$ and $Q_o = \sqrt{\alpha_1\alpha_2 CR_1/(C_1R_2)}$. Clearly ω_o, can be tuned without changing ω_o/Q_o via programming α_1 and/or α_2. However, the highpass filter output is not associated with a low impedance. Hence, an additional VB may be required to provide that output. Figure 14 shows the response of the highpass filter. The corner frequency is tuned from 20 kHz to 60 kHz. In summary, it can be seen that inductance simulation based circuits result in independent control of pole frequency without disturbing the bandwidth. However, they cannot be used in applications requiring the tuning of ω_o without varying Q_o. The following subsection develops filters enjoying independent control of ω_o without disturbing Q_o.
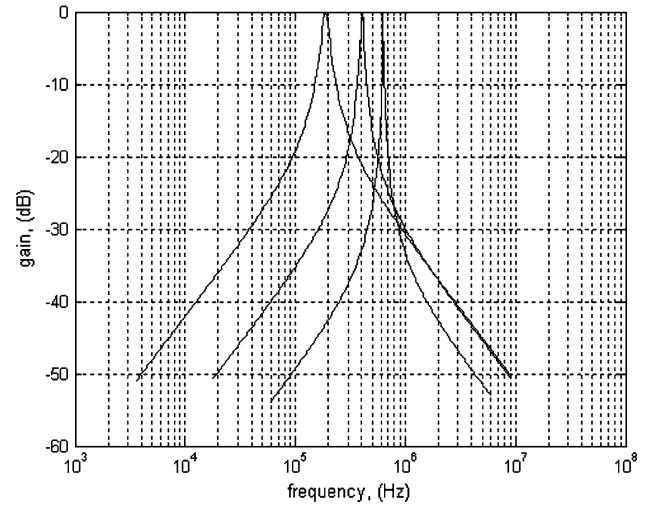
Fig. 11 Measured bandpass response of the voltage-mode filter of Fig. 10 showing ω_o tuning
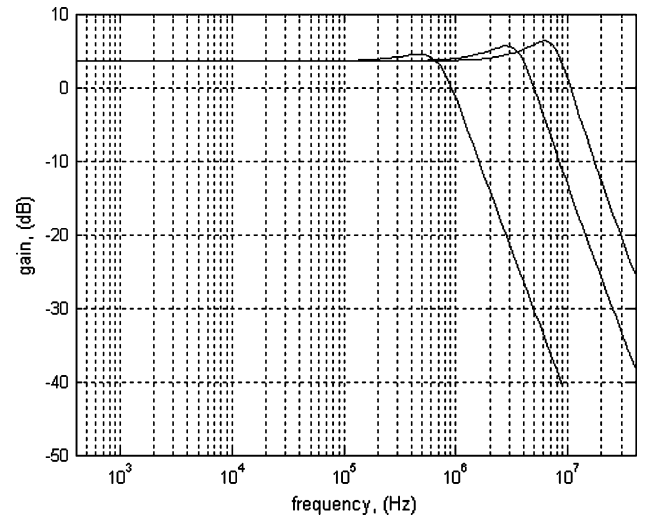
Fig. 12 Measured lowpass response of the current-mode filter of Fig. 10 showing ω_o tuning

4.2 Two-integrator loop based filters

Several well-developed active-RC circuits can be converted easily to their DCCA-RC counterparts by using the basic elements presented in Sect. 2. This results in the development of filters exhibiting independent control of ω_o without disturbing their Q_o. For example, the op-amp based
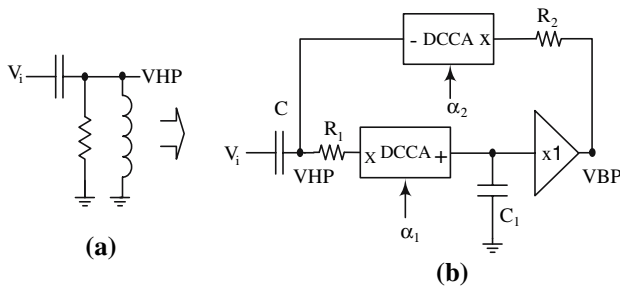
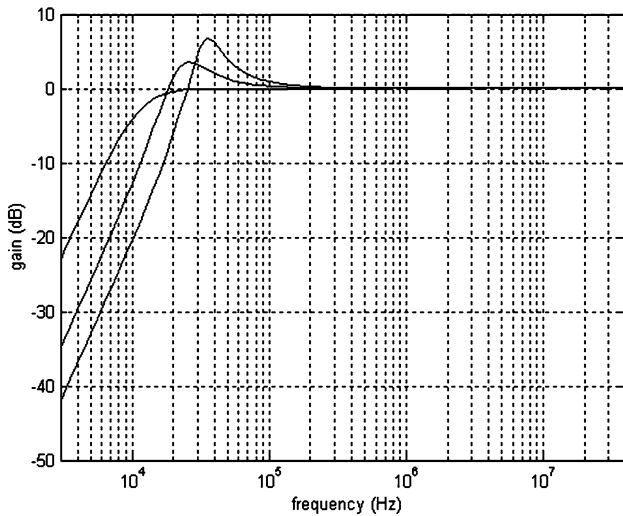**Fig. 13** Highpass filter: (**a**) LCR circuit (**b**) simulated circuit

Fig. 14 Measured response of the highpass filter of Fig. 17 showing ω_o tuning

resonator filter shown in Fig. 15(a) consists of a lossy integrator, a lossless integrator and an inverter connected in a loop. Two corresponding DCCA-RC based circuits are developed using the two different lossy integrators as shown in Fig. 15(b, c). Note that the inverter function is embedded in the second DCCA. The transfer function of the bandpass and lowpass outputs of the circuit of Fig. 15(b) are given by:

$$\frac{V_{BP}}{V_i} = -\frac{s\alpha_1/(C_1 R_4)}{s^2 + s/(C_1 R_1) + \alpha_1\alpha_2/(C_1 C_2 R_2 R_3)}, \qquad (18)$$

$$\frac{V_{LP}}{V_i} = -\frac{\alpha_1\alpha_2/(C_1 C_2 R_2 R_4)}{s^2 + s/(C_1 R_1) + \alpha_1\alpha_2/(C_1 C_2 R_2 R_3)}. \qquad (19)$$

The filter parameters are expressed as: $\omega_o = \sqrt{\alpha_1\alpha_2/(C_1 C_2 R_2 R_3)}$, $\omega_o/Q_o = 1/(C_1 R_1)$ and $Q_o = R_1\sqrt{\alpha_1\alpha_2 C_1/(C_2 R_2 R_3)}$. Therefore, the corner frequency cannot be controlled without disturbing quality factor. On the other hand, the second filter of Fig. 15(c) has the same transfer functions except the second term in the denominator is multiplied by α_1 to become $s\alpha_1/(C_1 R_1)$. Therefore, the different filter parameters become: $\omega_o = \sqrt{\alpha_1\alpha_2/(C_1 C_2 R_2 R_3)}$, $\omega_o/Q_o = \alpha_1/(C_1 R_1)$ and $Q_o =$
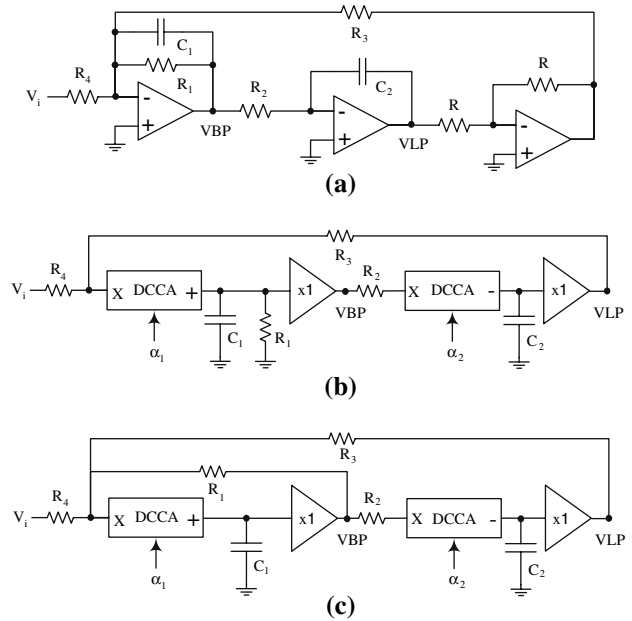

Fig. 15 Resonator filter: (**a**) based on op-amps, (**b**) & (**c**) based on the DCCA and VB
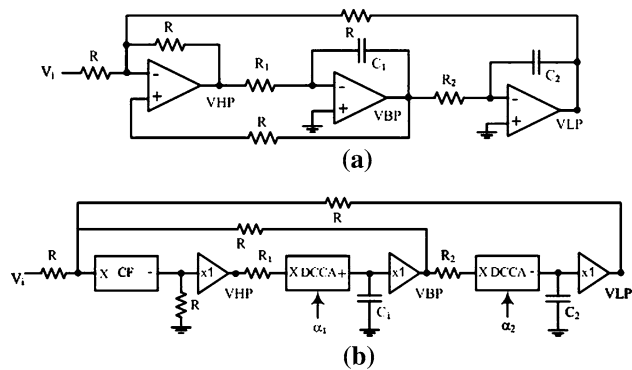

Fig. 16 State variable filter (**a**) based on op-amps (**b**) based on the DCCA and VB

$R_1\sqrt{\alpha_2 C_1/(\alpha_1 C_2 R_2 R_3)}$. Hence, it can be seen that ω_o can be varied digitally without changing Q_o by tuning α_1 and α_2, simultaneously.

The state-variable filter or the universal filter, which provides highpass, bandpass, and lowpass functions, realized by op-amps is shown in Fig. 16(a). It is composed of two lossless integrators and a summer circuit. The DCCA-RC based state variable is shown in Fig. 16(b). Note that the function of the summer is implemented by exploiting the virtual ground and the different current polarity of the DCCA. The transfer functions of the filters are similar to those of the original filter except with the replacement of R_1 and R_2 by R_1/α_1 and R_2/α_2, respectively. This yields the following transfer functions:
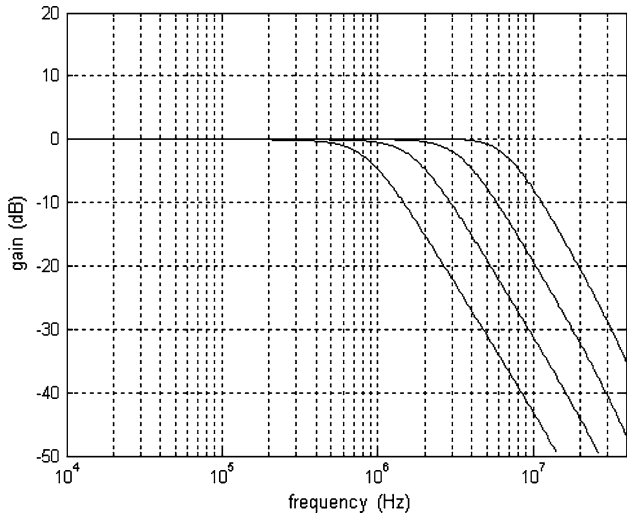
Fig. 17 Measured response of the lowpass filter of Fig. 16(b)

$$\frac{V_{HP}}{V_i} = \frac{s^2}{s^2 + s\alpha_1/(C_1R_1) + \alpha_1\alpha_2/(C_1C_2R_1R_2)}, \quad (20)$$

$$\frac{V_{BP}}{V_i} = -\frac{s\alpha_1/(C_1R_1)}{s^2 + s\alpha_1/(C_1R_1) + \alpha_1\alpha_2/(C_1C_2R_1R_2)}, \quad (21)$$

$$\frac{V_{LP}}{V_i} = -\frac{\alpha_1\alpha_2/(C_1C_2R_1R_2)}{s^2 + s\alpha_1/(C_1R_1) + \alpha_1\alpha_2/(C_1C_2R_1R_2)}. \quad (22)$$

Therefore, the parameter ω_o and Q_o are given by: $\omega_o = \sqrt{\alpha_1\alpha_2/(C_1C_2R_1R_2)}$ and $Q_o = \sqrt{\alpha_2C_1R_1/(\alpha_1C_2R_2)}$. Clearly, ω_o can be tuned digitally without disturbing Q_o by varying α_1 and α_2, simultaneously. Note that the DCCA-RC based filters employed grounded capacitors, which is recommended by integrated circuit technologies. The measured response of lowpass filter with variable ω_o is shown in Fig. 17. The corner frequency is tuned from 600 kHz to 5 MHz. The notch and the allpass filters can be obtained by properly adding the lowpass, bandpass and the highpass filters.
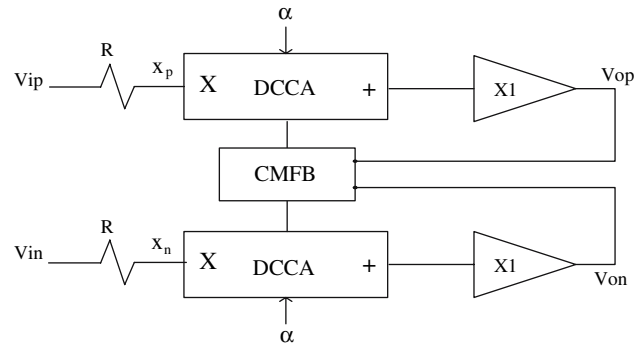

Fig. 18 CMOS realization of the fully differential DCCA-VB

5 Fully differential realizations

Fully differential operation is required by most of the modern high-performance integrated circuits. This is attributed to the facts that fully differential operation improves noise rejection, increases the dynamic range particularly at low supply levels and minimizes harmonic distortions. However, a fully differential topology requires the addition of common mode feedback (CMFB) circuitry to control common-mode output voltage and without it common-mode voltage is left to drift. There are several approaches to develop the fully differential architectures for the proposed circuits. One way is to develop fully differential realizations for both the DCCA and VB, which require modifications in their CMOS realizations. This method would require a separate CMFB circuit for each element. Alternatively, a single CMFB circuit can be employed to establish the common-mode voltage of both the DCCA and VB [17] and as shown in Fig. 18. This method is straightforward, easier to develop, and avoids the use of redundant CMFB circuits. Figure 19 shows the design of the fully differential architecture of the DCCA-VB including the CMFB circuit.
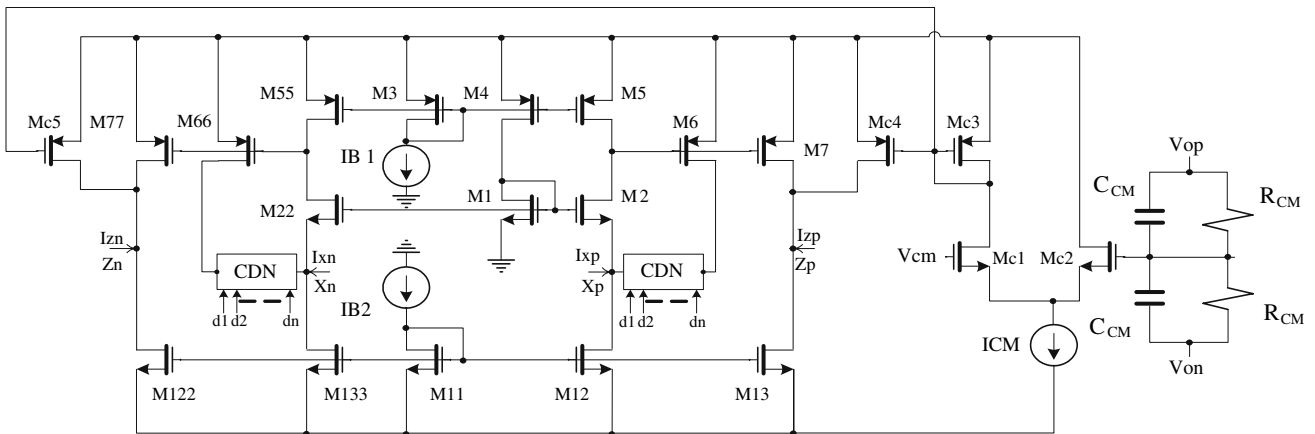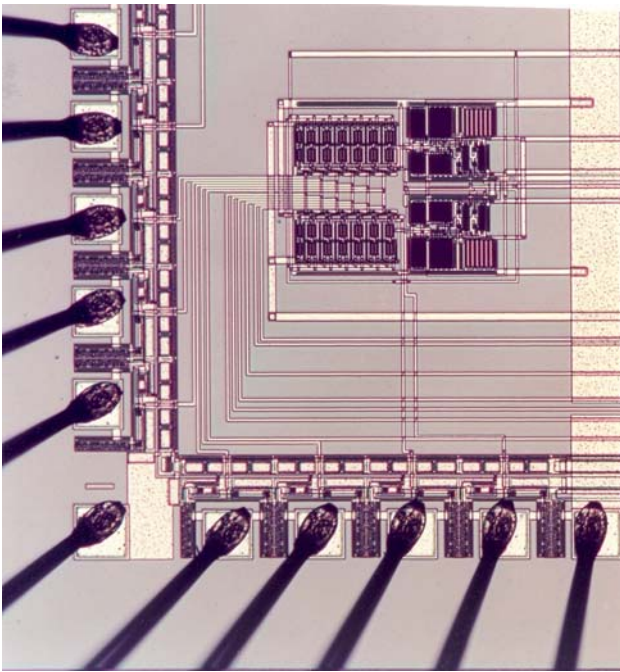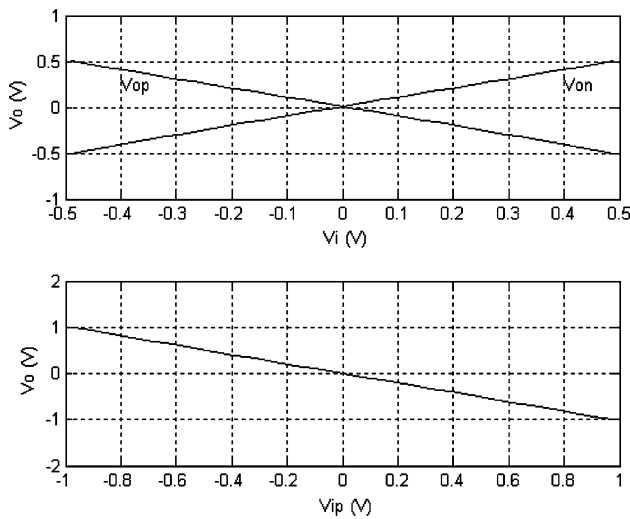

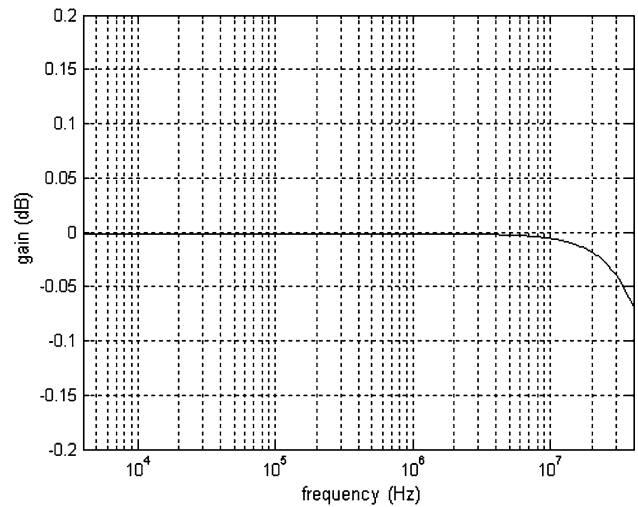**Fig. 19** Architecture for fully differential realization of the proposed DCCA-VB
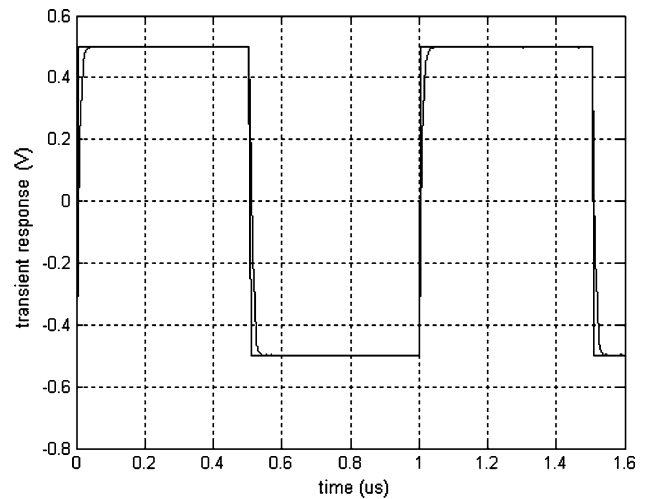
Fig. 20 Die-photo showing differential DCCA-VB

Fig. 21 Measured DC characteristics of DCCA-VB: single-ended and fully differential


Fig. 22 Measured ac characteristics of the fully differential DCCA-VB

Fig. 23 Measured transient characteristics of the fully differential DCCA-VB

Die photograph of the fully differential DCCA-VB element is shown in Fig. 20. It occupies an area of approximately 0.3x0.32 mm² in a standard 0.5 μm N-well CMOS technology. The inputs of the CMFB circuit are coming from the low impedance outputs of the VBs. This simplifies the design of the input stage of the CMFB circuit to two resistors (R_{cm}) and two capacitors (C_{cm}).

The operation of the CMFB circuit was explained in [17]. The measured DC response of the fully differential DCCA-VB with the X's and Z's terminals loaded with 1 kΩ resistors is shown in Fig. 21 while the ac response is shown in Fig. 22. The transient response of a square-wave input of 1 V_{pp} and 1 MHz frequency is shown in Fig. 23. The 1% settling time is approximately 40 ns. The measured input referred noise of the fully differential DCCA-VB is 17.3 nV/$\sqrt{\text{Hz}}$. The nonlinearity of the circuit was determined using the two tones intermodulation test. The measured input third intercept point IIP3 is found to be 31.4 dBm.

Using this fully differential basic building block circuit, fully differential architectures of the proposed circuits can be implemented easily. For example, Fig. 24 shows the fully differential version of the universal filter of Fig. 16(b). The measured bandpass filter function is shown in Fig. 25 where the center frequency is tuned from 48 kHz to 500 kHz. The common mode rejection ratio (CMMR)
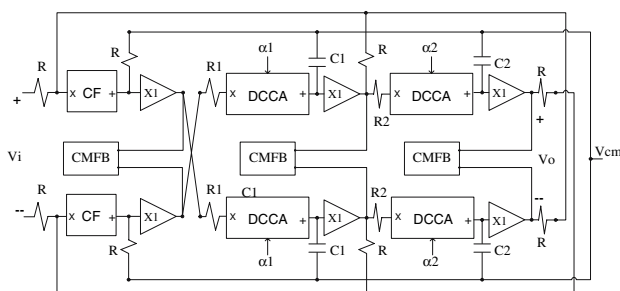
Fig. 24 Fully differential realization of the universal filter
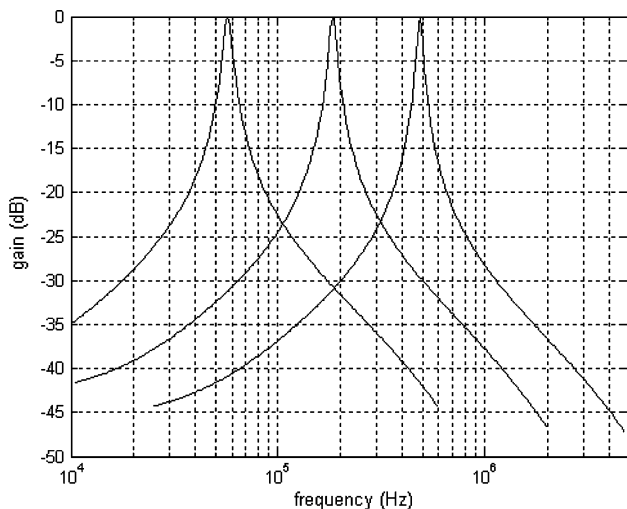
Fig. 25 Measured response of the bandpass filter of Fig. 24 showing center frequency tuning

and power supply rejection ratios (for both negative and positive supplies) were measured to be better than 45 and 40 dB, respectively.

6 Conclusions

A digitally programmable approach of designing analog and mixed signal CMOS integrated circuits is presented. The proposed technique based on digitally controlled current amplifier (DCCA) and unity gain voltage buffer achieves wide frequency operating range. Employing polysilicon resistors and capacitors, it exhibits high linearity. The DCCA is utilized to provide digital tuning of the design parameters of the proposed circuits. Basic building blocks such as amplifiers, integrators and inductors are developed. Systematic approaches of designing voltage and current-mode filters are described. Circuits based on the proposed technique achieve wide tuning ranges with high resolution without component spreading. The tuning resolution depends on the size of the CDN. With the experimental setup of 6-bit CDN, the gain and frequency characteristics of filters can be adjusted with 1.5%

accuracy. However, the resolution can be improved to better than 0.1% when using 10-bit CDN. Fully differential architecture of the proposed approach is developed. The DCCA and VB were fabricated in a standard 0.5 μm CMOS technology. All of the proposed techniques and circuits are experimentally verified.

Non-ideal analysis studying the frequency limitations can be performed to each circuit separately. In general, however, it can be observed that, for all of the proposed circuits, all internal nodes, except those of integrating capacitors, are either at virtual ground or low impedance (output terminal of VBs). Thus all parasitic poles and zeroes are expected to be at very high frequencies. The relatively low band response of the measured filter data is limited by the breadboard implementation of the various filters, in the presence of parasitic capacitances in the order of 20 pF. In integrated circuits, parasitics are much smaller; hence, operation with higher bandwidths can be demonstrated.

References

1. Durham, A., Redman-White, W., & Hughes, J. (1992). High-linearity continuous time filter in 5-V VLSI CMOS. *IEEE Journal of Solid-State Circuits, 27*, 1270–1276.
2. Roberts, G., & Sedra, A. (1988). All current-mode frequency selective circuits. *Electronics Letters, 25*, 183–194.
3. Ismail, M., Smith, S., & Beale, R. (1988). A new MOSFET-C universal filter structure for VLSI. *IEEE Journal of Solid-State Circuits, SC-23*, 183–194.
4. Toumazou, C., Lidgey, J., & Haigh, D. (1990). *Analogue IC design: The current mode approach.* London: Peter Peregrinus Ltd.
5. Wilson, B. (1990). Recent development in current conveyors and current mode circuits. *Proceedings of the Institute of Electrical Engineering pt G, 137*, 63–77.
6. Liu, S.-I., Chen, J.-J., & Hwang, Y.-S. (1995). New current mode biquad filters using current followers. *IEEE Transactions on Circuits and Systems, 42*, 380–383.
7. Gupta, S., & Senani, R. (2006). New voltage-mode/current-mode universal biquad filter using unity-gain cells. *International Journal of Electronics, 93*, 769–775.
8. Senani, R., & Gupta, S. (2006). New universal filter using only current followers as active elements. *International Journal of Electronics and Communication, 60*, 251–256.
9. Soliman, A. (1998). Equal-R, equal-C current mode Butterworth lowpass filters. *IEICE Transactions on Fundamentals, E81-A*, 340–342.
10. Weng, R.-M., Lai, J.-R., & Lee, M.-H. (2000). New universal biquad filters using only two unity-gain cells. *International Journal of Electronics, 87*, 57–61.
11. Rudell, J., Ou, J.-J., Cho, T., Chien, G., Brianti, F., Weldon, J., & Gray, P. (1997). A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone application. *IEEE Journal of Solid-State Circuits, SC-32*, 2071–2088.
12. Park, S., Kim, J., & Choi, S. (2005). Digitally controlled wide-band CMOS variable gain amplifier (Vol. 2, pp. 896–899). *Presented at the 7th International Conference on Advanced Communication Technology (ICACT).*

13. Mahmoud, S., Hashiesh, M., & Soliman, A. (2005) Low-voltage digitally controlled fully differential current conveyor. *IEEE Transactions on Circuits and Systems I-Regular Papers, 52*, 2055–2064.

14. Wang, C.-C., Lee, C.-L., Lin, L.-P., Tseng, Y.-L. (2005). Wideband 70 dB CMOS digital variable gain amplifier design for DVB-T receiver's AGC (Vol. 1, pp. 356–359). *Presented at Proceedings of International Symposium Circuits and Systems (ISCAS)*.

15. Bult, K., & Geelen, C. (1992). An inherently linear and compact MOST-only current division technique. *IEEE Journal of Solid-State Circuits, SC-27*, 1730–1735.

16. Hammershchmied, C., & Huang, Q. (1998). Design and implementation of an untrimmed MOSFT-only 10-bit A/D converter with −79 dB THD. *IEEE Journal of Solid-State Circuits, 33*, 1148–1157.

17. Alzaher, H., Elwan, H., & Ismail, M. (2002). A CMOS highly linear channel select filter for 3G multi-standard integrated wireless receivers. *IEEE Journal of Solid-State Circuits, 37*, 27–37.

18. Khorramabadi, H., Tarsia, M., & Woo, N. (1996). Baseband filters for IS-95 CDMA receiver applications featuring digital automatic frequency tuning (pp.172–173). *Presented at International Solid State Circuits Conference, San Francisco*.

Hussain Abdullah Alzaher was born in Qatif-Alawamya, Saudi Arabia, in 1972. He received the B.S. and M.S. Degrees (with honors) in Electrical Engineering from King Fahd University of Petroleum and Minerals (KFUPM), Dhahran, Saudi Arabia, in 1994 and 1997, respectively, and the Ph.D. Degree from The Ohio State University, Columbus, in 2001. Since 1994, he has been with KFUPM as a Faculty Member in the Electrical Engineering Department. His research interest includes applications of electronic circuit techniques for wireless communications: Multi-standard mobile phones, Bluetooth, WLAN and WiMAX. He is the author and co-author of more than 40 journal papers. Dr. Alzaher is the recipient of the 1994/1995 Prince Muhammed bin Fahd bin Abdulaziz Award for Excellence in Scientific Achievement. He is also the recipient of the 2003 Showman award for Young Arab Researchers, Engineering Science. Dr. Alzaher is a member of the Saudi Scientific Society for Electrical Engineering (SSSEE).