Design of a linearly assisted switcher for a supply modulated RF transmitter

Timo Rahkonen · Olli-Pekka Jokitalo

Abstract A broadband modulated power supply for envelope tracking or polar RF transmitters has been built. To study the design constraints, an efficient state-based simulation tool was developed. Based on the simulations, a prototype supply was built. It can deliver up to 1 W (6 V, 150 mA) to a resistive load of 30 ohms with spectral purity of ca. –45 dBc. The power efficiency using a QAM-signal is 49%.

Keywords Linearly assisted switcher · State model · Power efficiency

1 Introduction

The ratio between peak and average output power tends to be large in modern RF modulation formats, and this has two drawbacks. First, a linear and hence power inefficient RF power amplifier is needed to repeat the amplitude variations. Second, the amplitude distribution (shown with thick line in Fig. 1) is such that the peak amplitudes appear very seldom. This results in the fact that for most of the time the signal is small compared to compression level, which drastically reduces the average power efficiency.

One increasingly popular solution to the above problem is to modulate the power supply of the RF power amplifier so that the supply voltage tracks the signal amplitude. If the

T. Rahkonen (✉)
Electronics Laboratory, Department of Electrical Engineering and Infotech Oulu, University of Oulu, P. O. Box 90014, Oulu, Finland
e-mail: timor@ee.oulu.fi

O.-P. Jokitalo
Filtronic Comtek, Kempele, Finland

real-time modulation can be done with high efficiency, this greatly improves the overall efficiency of the transmitter.

The supply modulation can be implemented in two ways. In envelope tracking (ET) systems the RF power amplifier is linear, and the supply modulation does not need to be exactly precise, as the amplitude information is still contained in the input signal [1]. The other and more challenging way is to use a switch-mode RF power amplifier, that has a constant-amplitude, phase modulated input. Here all the amplitude information is in the modulated power supply, so that the supply modulation needs to be precise [2].

This paper presents the design method, implementation and measured results of a linearly assisted switch-mode supply modulator. It has been tested with signal bandwidths ranging from 100 kHz to 4 MHz both in a switched-mode polar transmitter and an ET transmitter employing a linear amplifier. The ET transmitter is a slightly easier application, as the supply voltage does not need to dip sharply to zero.

2 Structure of the modulated supply

A simplified block diagram of the implemented supply modulator is shown in Fig. 2. The structure has been reported in [3, 4] and it consists simply of a Buck down-converting switcher and a parallel broadband assisting amplifier that both absorbs the ripple current of the switcher and fills in the peak currents that are too rapid for the switcher. This replaces the functionality of the output filter capacitor usually seen in switchers, and allows broadband modulation.

The RF power amplifier appears as a resistive load for the supply, and it is modelled later as a series LR network.
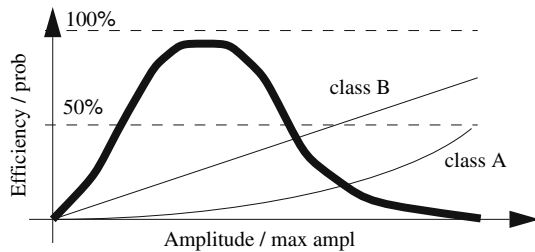
Fig. 1 Amplitude probability density function of a modulated signal and power efficiency of class A and B amplifiers, shown as functions of signal amplitude
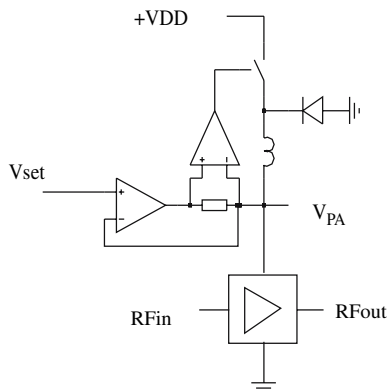

Fig. 2 Schematic of the linearly assisted, hysteretic-controlled switcher

The inductive part caused by the DC bias choke needs to be relatively small to allow broadband modulation. It is worth noting that the LC bias filtering is much weaker than in normal RF PA's, which complicates the PA design, too.

The control of the switcher is very simple: the switch is controlled by the polarity of the output current of the assisting amplifier. Hence, the operation is asynchronous, and the average switching frequency of the switcher is set by the value of the coil L and the inevitable loop delays caused by the comparator and opening and closing delays of the switch. This complicates the design as most switcher analysis methods assume synchronous operation of the switcher.

In this design, the ripple in the inductor current is mostly absorbed by the assisting amplifier. This sets stringent requirements for the closed loop output impedance R_{ocl} of the amplifier, as it needs to effectively short the ripple current. Assuming a –20 dB ratio between the average current and the ripple current (i.e., 10% ripple current) and aiming to –50 dBc spurious response, R_{ocl} needs to be 30 dB lower than the load resistance at all relevant frequencies. For example, a class E amplifier with 80% drain efficiency and 1 W output power at 6 V supply appears as a 29 ohm resistive load. The above reasoning means that the closed-loop output impedance of the amplifier needs to

be ca. 1 ohm up to 10 MHz, which calls e.g., for an opamp with 50 ohm open-loop output impedance and GBW of at least 500 MHz. In high-power transmitters the supply voltages are higher (up to 30–50 V), but the tendency is the same: very high loop bandwidth and low open-loop output impedance are needed to keep the closed-loop output impedance low.

3 Quick simulation technique

Simulation of switch-mode power supplies is in general slow due to the largely different time constants of the switched and continuous-time parts. Also the low-loss LC circuits are problematic for transient analysis, being another reason that requires the use a small time step. In a modulated supply the situation is even worse, as long signal sequences are needed to measure the quality and spectral purity of the generated output. Hence, to be able to study the design constraints and find the required peak amplifier currents, for example, a quick state-based simulator was developed.

To avoid the very small time steps needed to solve the response of a switching circuit, a Matlab-based simulator was built, based on the assumption that the system is a linear, time-varying circuit. The response of the linear circuit can be calculated without iteration or numerical integration at any given time point, which greatly reduces the burden. Now the state of the circuit needs to be calculated only at such time points when either the input signal or the state of the switcher changes. This makes the simulator essentially to operate at the sampling rate of the envelope signal and facilitates long enough data sequences to capture some statistical properties of the system.

The reader should note that this approach is fundamentally different from using a HDL or Simulink description of the circuit, as these typically result in traditional transient analysis. The essential feature of this modelling is that it does not require numerical integration or heavy oversampling of the signals.

The principle of the analysis is the following. A state model (see e.g., [5]) is built for both states (switch positions) of the circuit shown in Fig. 3. Five state variables were used: inductor current I_L, voltage V_o of the small filter capacitance C (that can be used to reduce the RF ripple in the supply voltage), current I_{LO} of the inductor in the RL series load presenting the amplifier, dominant pole in the assisting amplifier V_a, and one state for creating a first-order low-pass filter for the sampled-and-held input signal V_{in}. Adding more state variables to obtain a more complicated amplifier model, for example, is straightforward. The state equations for the period when the switch is on are of form (1), where R_{ds} is switch on-resistance, R_L
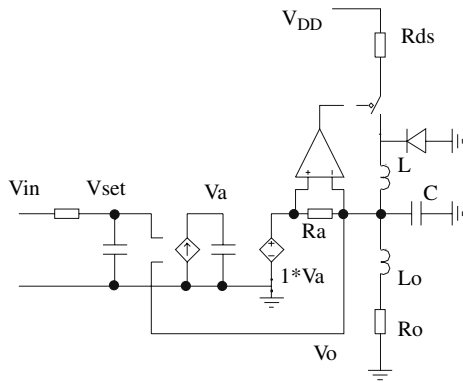
Fig. 3 Equivalent circuit of the simulated system

is the series resistance of inductor L, R_a lumps the opamp open-loop output impedance and a separate current measuring resistor, ω_t is opamp GBW and a is the corner frequency of the reconstruction filter.

behavior of the switching, for example. This was taken into account by introducing a transport delay t_d in switching (caused by the delay of the comparator and charging/discharging the gate capacitance of the switching FET), and the value of this was calibrated by comparing the calculated results to the results of short SPICE simulations, where manufacturer-provided simulation models were used for the opamp, comparator, schottky diode, and the FET switch. Similar simulations and later also measured results of the constructed prototype were used to calibrate the power dissipation estimates due to partial conduction, for example.

Altogether, the simulation is based on the following assumptions, also illustrated in Fig. 4:

- the input voltage V_{in} has a S/H response, so that it remains constant during a sample period
- the final state within the sample is calculated assuming linear settling given by eq. (3), using the previous final state as a new initial state $x(0)$

$$s\begin{bmatrix} I_L \\ V_O \\ I_{LO} \\ V_a \\ V_{set} \end{bmatrix} = \begin{bmatrix} -(R_L+R_{ds})/L & -1/L & 0 & 0 & 0 \\ 1/C & -1/R_aC & -1/C & 1/R_aC & 0 \\ 0 & 1/L_o & -R_o/L_o & 0 & 0 \\ 0 & -\omega_t & 0 & 0 & \omega_t \\ 0 & 0 & 0 & 0 & -a \end{bmatrix} \cdot \begin{bmatrix} I_L \\ V_O \\ I_{LO} \\ V_a \\ V_{set} \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & a \end{bmatrix} \cdot \begin{bmatrix} V_{DD} \\ V_{in} \end{bmatrix} \quad (1)$$

The transient response of the circuit is calculated as follows: using the normal state matrix notation in (2),

$$sX = A \cdot X + B \cdot U$$
$$Y = C \cdot X + D \cdot U \quad (2)$$

the forced response of the circuit can be calculated for any time point t by (3), where the latter form is true if the input vector U remains piece-wise constant during the calculation period

$$x(t) = \Phi(t) \cdot x(0) + \int_0^t \Phi(t-\tau) \cdot B \cdot u(\tau)d\tau$$
$$= \Phi(t) \cdot x(0) + A^{-1} \cdot (\Phi(t) - 1) \cdot B \cdot U \quad (3)$$

Here

$$\Phi(t) = \exp m(At) = I + At + \frac{A^2 t^2}{2!} + \dots \quad (4)$$

is the natural response of the circuit. Thus, one can use the final state of the previous sample as a new $x(0)$ and directly evaluate the next final state. However, the assumption of instantaneously switching linear circuit masks the detailed

- if the final state causes the comparator to trigger (i.e., the amplifier output current or V_a–V_o changes sign), the actual zero-crossing time t_z is searched by bisection. The comparison and switching is assumed to have a delay t_d, and the state model of the system is changed t_d seconds after the zero-crossing time t_z.

The main difference to a normal transient analysis is that here only one time point per sample is evaluated (plus additional 8-step binary search every time the error voltage changes time—this gives a timing resolution of 1/256 of the initial time step). The matrix exponentials are precalculated and tabulated so that all evaluations consist of
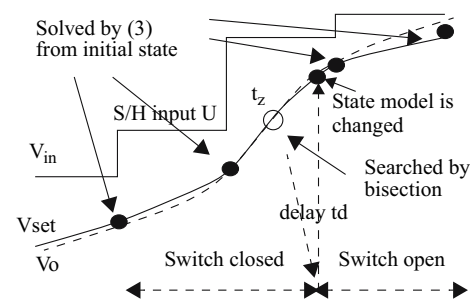

Fig. 4 Principle of the analysis

matrix multiplications only. This allows much faster simulation of long sequences with modulated data, and parametric sweeps to study the dimensioning constraints and dominant causes of losses. The main limitation is that the model is linear, and e.g., current limiting effects can not be (easily) included. Some coarse nonlinear effects can be implemented by using a different set of state matrices for different signal levels, for example.

An example of a transient simulation is shown in Fig. 5. Plot (a) shows input and output waveforms (a rectified QAM signal). Plot (b) shows the inductor and amplifier currents and the total load current. It is seen that the amplifier generates an opposite saw-tooth waveform to cancel the ripple in the inductor current. Note also, that in this simulation the switcher itself is rather agile, resulting in high ripple current and switching frequency.

The power dissipation and efficiency can be calculated. As an example, plot (c) shows the power dissipation in the output stage of the amplifier, and the average losses caused by charging and discharging the FET capacitance at the average switching frequency f_{avg}. Similar plots can be generated for switch and diode conduction losses, and after calibrating with real transient simulations, also the losses caused by partial conduction of the switch or charge
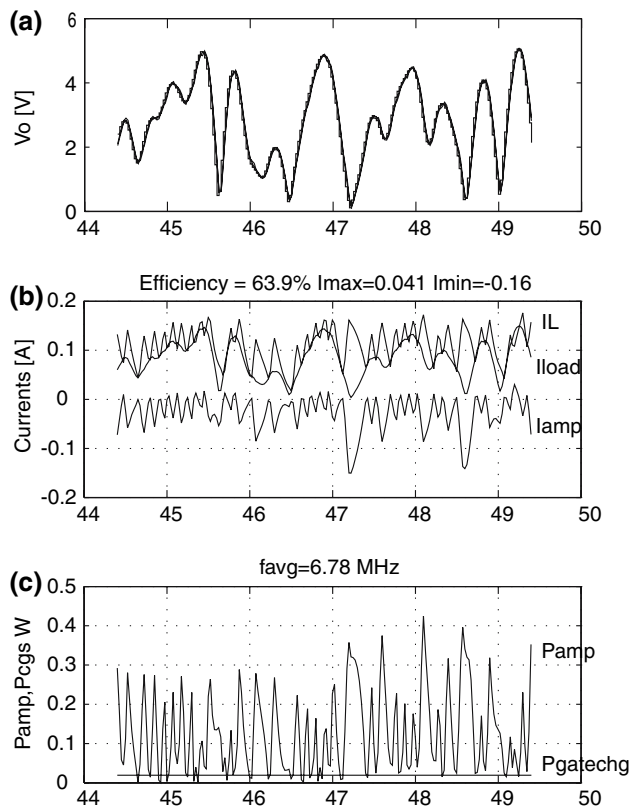
recovery can be included. This helps to find the dominant cause of losses, which in this case was the opamp and losses in the switch and diode.

4 Dimensioning constraints

The developed quick simulator was used to study the dimensioning trade-offs of the modulator, and several nested sweeps with long sequences of real QAM-modulated input data were performed. As an example, the effect of varying the amplifier GBW and inductance value are studied in Fig. 6, where GBW was swept from 10 MHz to 1 GHz (shown on the x-axis) and L on the y-axis. According to (a), the inductor value sets the switching frequency and hence affects switching-related losses. The input–output delay t_{dly} in (b) depends mostly on the amplifier GBW. The extracted value of t_{dly} is needed to match the propagation delay of the phase and amplitude paths in the polar transmitter, and also to calculate the error between input and output voltages, as the input needs to be delayed by t_{dly} before the error is calculated. The calculated output rms error shown in (c) is proportional to $1/(GBW*L)$, as increasing GBW reduces the amplifier output impedance and increasing L reduces the ripple current in the inductor. According to (e), the efficiency drops due to switching losses when the average switching frequency is increased beyond 4–5 MHz.

Altogether, this simulation suggests using rather large inductor value (i.e., a slow switcher) and a very broadband assisting amplifier. As shown in plot (d), this happens at the expense of larger peak output current of the amplifier: when the switcher is slow, the amplifier needs to provide large peak currents. The chosen L and GBW values (L = 6.8 µH and GBW = 900 MHz) for the prototype are shown by a black dot in the plots. The choice of rather high switching frequency helped to keep the peak output current low enough so that the output stage of a commercial broadband opamp is sufficient, and no external driver stage was needed.

5 Experimental results

An experimental circuit was built using discrete integrated circuits. The target system was a polar transmitter consisting of a digital data separator, the modulated supply, and a 0.5 W class E switch-mode power amplifier designed using a discrete CLY5 GaAs MESFET [6]. These were tested as a complete polar transmitter with various modulating signals, and the same supply modulator was also used to drive a linear amplifier in an ET experiment.

The complete implementation is shown in Fig. 7. National Semiconductor LMH6609 opamp had 900 MHz

Fig. 5 Example transient simulation of the system. (**a**) Output voltage, (**b**) inductor, amplifier and load currents, and (**c**) power dissipation of the switch driver and amplifier output stage
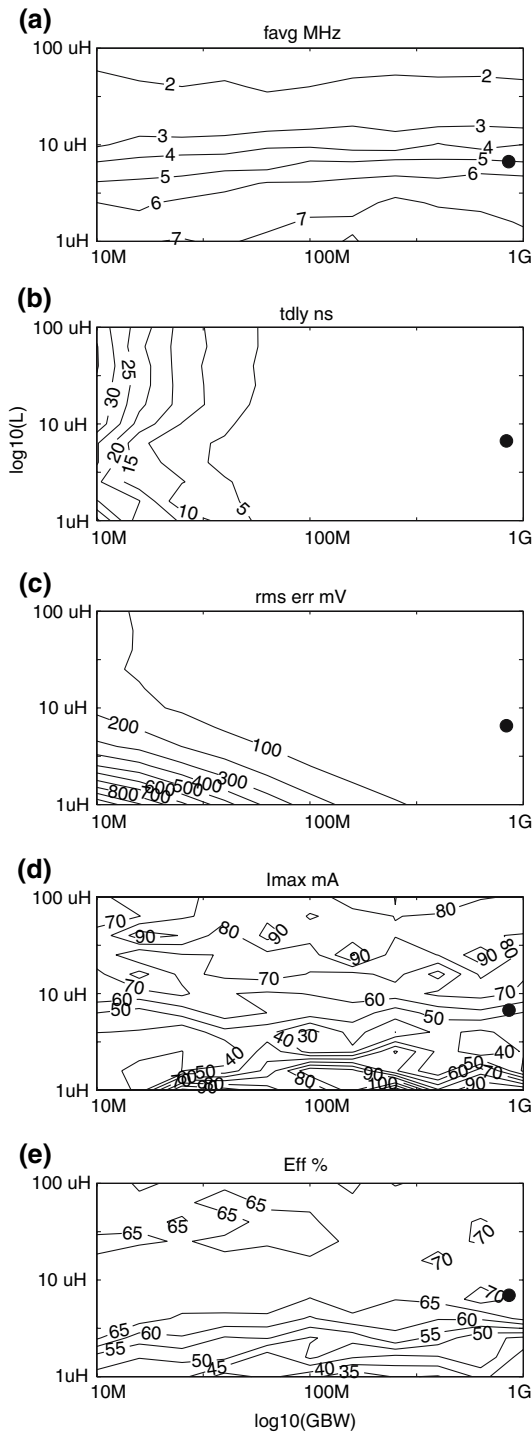
Fig. 6 Results of 2-D logarithmic GBW, L sweep. (a) average switching frequency, (b) input–output delay, (c) rms output error, (d) peak amp. current, and (e) power efficiency

GBW and sufficient 90 mA output current for assisting the switcher without an external driver. MAX961 high-speed comparator and a discrete three-transistor buffer were used to drive the switcher. Due to the 5 V maximum input voltage of the comparator, an attenuator network was needed in the input of the comparator.
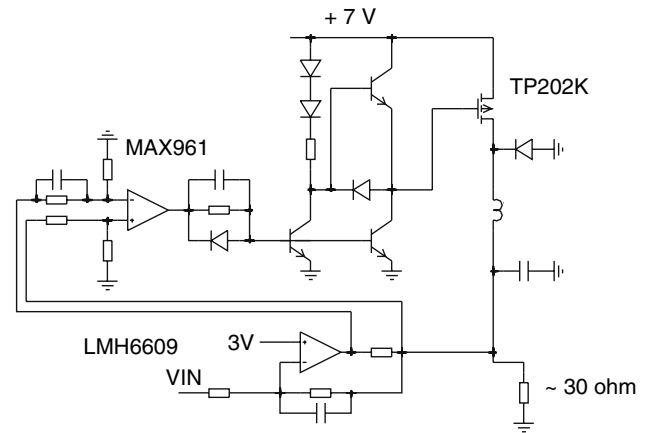

Fig. 7 Implemented modulated supply

The loop delay was dominated by the switch-off delay of the transistor, which (due to the relatively low discharge current through the load) was as long as 50 ns. The effect of this was partially compensated by slightly differentiating the input signal of the comparator. Also the speed of the level shifter was boosted by a slight differentiation.

The linearity of the modulator is challenging to measure. Single-tone distortion measurements cause the switching frequency to synchronize with the input signal, causing switching brum to appear as harmonic distortion. Hence, it is more realistic to use a broadband test signal that randomises the switching events.

The targeted RF signal had a bandwidth of 4 MHz, centered at 1 GHz. This gives a baseband bandwidth of 2 MHz, but the actual rectified envelope signal is much more broadband, due to the nonlinearity of the rectification. Hence, any nonlinear distortion and switching images are buried underneath the signal and can only be found by calculating the difference of the measured output and a fitted ideal input signal. This was done by measuring the input and output signals by an oscilloscope, compensating the input–output delay, and calculating the difference, as shown in Fig. 8.
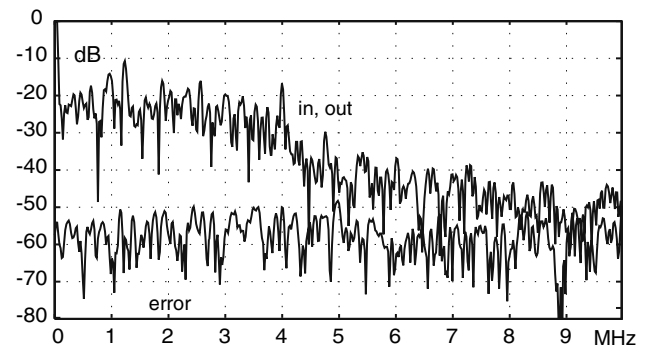

Fig. 8 Measured input, output, and error spectra of rectified envelope signal
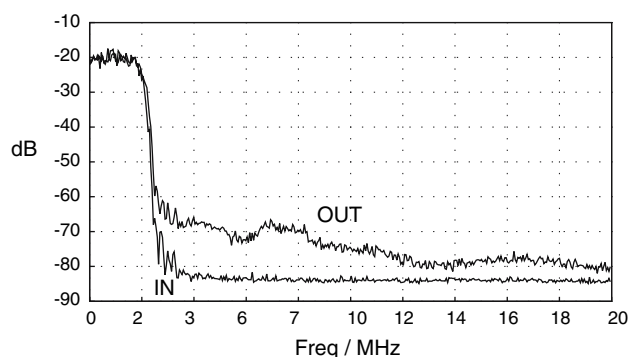
Fig. 9 Measured input and output spectra of a non-rectified QAM signal with proper DC offset

The vertical resolution of an oscilloscope is only modest, and also any errors in the estimated input–output delay affect the residual error. For test purposes, the modulator was also driven by a narrowband (non-rectified) root-raised cosine filtered QAM signal, and the input and output spectra were measured using a spectrum analyzer with sufficient dynamic range. Figure 9 shows the measured input and output spectra, revealing that the spectral purity of better than 45 dBc. The test also shows switching image is centered at the average switching frequency of 6 MHz.

6 Summary

The design principles of a supply modulator consisting of a Buck switcher and an assisting linear amplifier were shown. To speed up the simulation of modulated switch-mode supply modulators, a new state-based analysis technique was developed and used to search the design constraints of the modulator. The technique allows very quick simulation of long data sequences, so that e.g., spectral purity can be reliably estimated. It is believed that this technique can find other applications as well, for example modelling the behavior of reconstruction filters in baseband signal processing blocks.

The main limitations of the presented simulation technique are, that it assumes instantaneous switching and linear behaviour. To overcome the first one, lumped delay and switching losses were added, and the values of these were calibrated with short SPICE transient simulations.

One of the benefits of the technique is that it can calculate the response of highly resonating circuits without the numerical damping and frequency warping problems haunting numerical integration.

The system simulations clearly showed that the main limitation for high spectral purity is the rejection of the switcher output current ripple, and here it results in very

strict requirements of the output impedance of the assisting amplifier. The ripple current can be reduced by increasing the value of the switcher coil (i.e., slowing down the switcher), but this increases the required peak current from the amplifier. Another method to reduce the ripple is would be to use multi-level or multi-phase switcher, as shown e.g., in [7].

The implemented prototype was aimed for 1–2 W power level, and 0–6 V voltage level, only. Hence, the output current of a commercial opamp is sufficient, and no extra output stage was needed. Instead, at such a low power levels any dissipation overhead easily ruins the efficiency, and total efficiency with modulated signal stayed below 50%. The implemented class E power amplifier appeared as a 46 ohm load (instead of 30 ohms previously assumed), and the overall efficiency of a polar transmitter prototype was 36%. The efficiency of the Buck converter itself was only 72% due to high switching frequency and losses in the fly-back diode, but the majority of the losses were still caused by the assisting amplifier in this relatively low-power prototype.

Large loop delays in the switcher (especially when closing the switch) cause some phase lag between the amplifier and switcher currents, and this is one additional reason reducing the efficiency. Hence, it would be very beneficial to be able to reduce the loop delays. Additional improvement in efficiency can be achieved by replacing the fly-back Schottky diode with a FET.

References

1. Wang, F. et al. (2005). Design of wide-bandwidth envelope tracking power amplifiers for OFDM applications. *IEEE Transactions on Microwave theory and techniques, 53*(4), 1244–1255.
2. Diet, A. et al. (2004). EER architecture specifications for OFDM transmitter using class E amplifier. *IEEE Microwave and wireless components letters, 14*(8), 389–391.
3. Wang, F. et al. (2004). Envelope tracking power amplifier with pre-distortion linearization for WLAN 802.11 g. *In proceedings of IEEE MTT-S, 3,* 1543–1546.
4. Kimball, D. et al. Capacitorless DC-DC converter. US Pat Appl. US 2003/0137286 A1.
5. Reynaert, P. et al. (2003). A state-space behavioral model for CMOS class E power amplifiers. *IEEE Transactions on Computer-aided design of Intergrated Circuits and Systems, 22*(2), 132–138.
6. Hietakangas, S. et al. (2006). 1 GHz class E RF power amplifier for a polar transmitter. *In proceedings of 24th Norchip conference, Linköping, Sweden, 20–21,* 5–8.
7. Yousefzadeh, V. et al. (2006). Three-level buck converter for envelope tracking applications. *IEEE Transactions on Power Electronics, 21*(2), 549–552.

Timo Rahkonen was born in Jyväskylä, Finland, 1962. He received his Diploma Engineer, Licentiate and Doctor of Technology degrees in 1986, 1991 and 1994, respectively, in University of Oulu, Oulu, Finland. Currently he is a professor in circuit theory and circuit design in University of Oulu, Oulu, Finland.

Olli-Pekka Jokitalo designed and built the modulator prototype as his M.Sc thesis work at the University of Oulu, Finland. He is currently at Filtronic Comtec, Kempele, Finland.