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A polyphase filter based on CMOS inverters

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Abstract A new idea for generation of quadrature signals on chip is presented. The topology is based on a passive *RC* polyphase filter, where the resistive parts are made active by using inverters. The active filter combines quadrature generation, isolation, and gain without losing quadrature performance compared to a regular *RC* polyphase filter. The filter technique is demonstrated in a 10 GHz front-end application where a broadband VCO, having a tuning range of 1.44 GHz, drives an active polyphase filter to generate quadrature LO signals. According to simulations the quadrature phase error shows a typical tuned behavior and stays below 0.8° for the complete tuning range. Since the signal amplitude is high throughout the filter the noise is low, below 160 dBc/Hz at 10 MHz offset. The high amplitude also reduces the need for high gain tuned buffers, thereby enabling significant reductions in chip area.

Keywords Polyphase filter · Quadrature generation · CMOS

1 Introduction

The low-IF receiver is a good compromise between the classic heterodyne receiver and the homodyne receiver. The IF filters and amplifiers operate at low frequencies like in a homodyne structure, which is beneficial, but the image rejection can be troublesome. Since the image is located only two times the IF from the desired signal, it will pass the band-select filter unattenuated, putting very high demands on the image rejection by the receiver front-end. The image rejection ratio for a quadrature receiver can be expressed according to:

$$IRR \approx \left.\frac{4}{\varepsilon^2+\theta^2}\right|_{\text{Small } \varepsilon \text{ and } \theta} \quad (1)$$

where ε denotes the gain mismatch and θ the phase error between the I an Q branches. Large image rejection requires well matched receiver building blocks and accurate quadrature LO signals. Since switching mixers are typically used the phase accuracy is more important than the amplitude accuracy of the LO signals.

The most basic way to generate quadrature signals is to let resistors and capacitors form a symmetrical polyphase filter [1]. The main advantages of this structure are the simplicity (only passive components), high quadrature accuracy (good matching), and high frequency capabilities. However, the passive polyphase filter is not a power efficient solution. Power consuming active buffers are typically needed to compensate for the signal attenuation in the passive filter. The buffers are also needed to provide isolation between the mixer and the VCO. Strong signals in the mixer could otherwise disturb the sensitive VCO through pulling. Another common method for quadrature generation is to let a differential VCO work at twice the desired frequency and obtain quadrature by means of frequency division, which can be accomplished using a digital divide-by-two flip-flop. The main drawback using this technique is the large current consumption needed in order to achieve good phase noise performance. A quadrature VCO (QVCO) can gen-

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erate quadrature signals directly and it can be realized by coupling two differential LC VCOs to each other. The coupling forces the output phases to lock in quadrature, and the good phase noise performance of the LC oscillator can be preserved. In a standard quadrature receiver two mixers work in parallel, following the LNA. For low supply voltages it gives an advantage in terms of dynamic range to implement these mixers as quadrature passive mixers [2]. In order to minimize the on-resistance of the switches the LO voltage drive must be large, which can be accomplished by a tuned buffer. However, a quadrature LC-tuned buffer occupies a large chip area due to inductors [3] and together with the QVCO this solution is not very cost efficient. In this work an active polyphase filter is therefore considered instead, where the main idea is to combine isolation, gain, and small chip area. So far, active polyphase filters have been used in low frequency applications such as channel select filters, e.g. [4], but as demonstrated here the idea can be used for high frequency quadrature LO generation as well.

The paper is organized as follows. After recalling the regular RC-polyphase filter, Section 2 presents the active g_m-C structure and describes its behavior. Section 3 introduces the In-C topology, where the g_m-cell is implemented using a regular CMOS inverter, and finally Section 4 presents simulation results of a 10 GHz quadrature signal generator in 130 nm CMOS technology.

2 Analysis of ideal *RC* and g_m-*C* filters

The basic passive polyphase filter is shown in Fig. 1. The structure is symmetrical and the only building blocks are resistors and capacitors. To increase its frequency range a complete filter may consist of several links like the one depicted in Fig. 1 in cascade, where each link may have a different value of R and C [1]. The essential behavior of such a filter can, however, be found by investigating the structure of Fig. 1. A small phase-imbalance, θ, is introduced to the

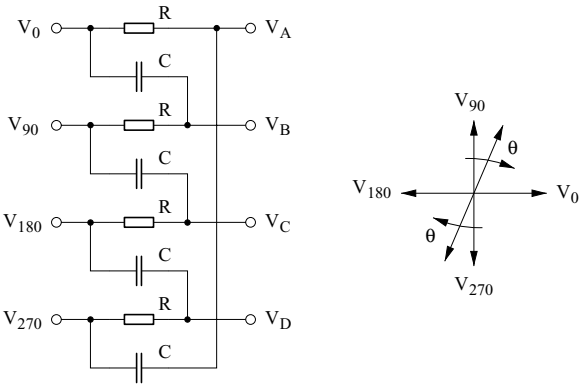

Fig. 1 A passive *RC* polyphase filter

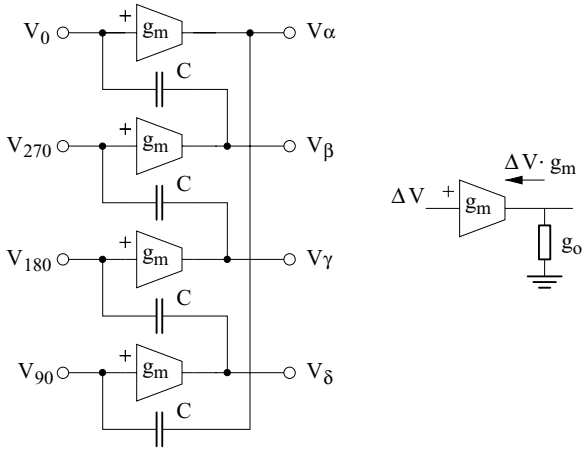

Fig. 2 The active g_mC polyphase filter

input signals. The phase difference between V_A and V_C (and between V_B and V_D) will still equal 180° thanks to the circuit symmetry. However, the phase difference between V_A and V_B will depend on both the circuit tuning and the angle θ. If V_0 is treated as the reference phase, the phases of V_A and V_B will be:

$$\begin{aligned} \angle V_{A,V_0=\text{ref}} &= \arctan\left(\frac{\cos(\theta)+1/(\omega RC)}{\sin(\theta)}\right) \\ \angle V_{B,V_0=\text{ref}} &= \arctan\left(\frac{-\sin(\theta)}{\cos(\theta)+\omega RC}\right) \end{aligned} \tag{2}$$

when the circuit is perfectly tuned, i.e. $\omega RC = 1$, the phase difference will be independent of θ and always equal to 90°.

If the resistors of the regular polyphase filter in Fig. 1 are replaced by transconductances, an active counterpart is found, see Fig. 2. This topology behaves in the same way as the regular structure if g_m equals $1/R$ and ideal source and load is assumed. However, the high input impedance of the transconductor reduces the loading of the preceding stage. The voltage gain of an unloaded single stage equals $\sqrt{2}$ for the *RC* structure and 2 for the g_mC structure. If a cascade of identical stages are used, the gain per stage of the passive filter drops to $1/\sqrt{2}$. For the active filter this calculation is more difficult, as illustrated in Fig. 3. For an arbitrary stage in a large cascaded structure it can be assumed that Z_{in} equals Z_L, which represents Z_{IN} of the following stage. By using nodal analysis we can derive the analytical expression for Z_{IN}. By inspection we get:

$$\begin{aligned} I_c + I_g + I_Z &= g_m V_{in} e^{-j\frac{\pi}{2}} \\ I_c &= \frac{V_{in}-V_L}{\left(\frac{1}{j\omega C}\right)} = \omega C e^{j\frac{\pi}{2}}(V_{in}+I_Z Z_L) \end{aligned} \tag{3}$$

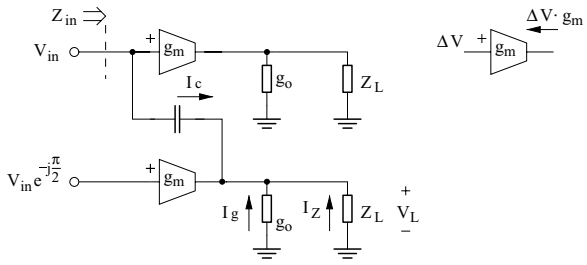

Fig. 3 Model of the active g_mC polyphase filter for calculating the stage gain

By using $I_g = -V_L g_o$ and setting the input impedance Z_{in} equal to load impedance Z_L we get the following expression for Z_L:

$$Z_L = Z_{in} = \frac{V_{in}}{I_c} = \frac{1 - j\omega C \cdot Z_L \left(j\frac{g_o}{\omega C} - 1\right)}{j\omega C(1 + Z_L(-jg_m + g_o))} \tag{4}$$

If a suitable software is used, Z_L can be solved analytically. It is assumed that the stage is tuned to ensure $g_m = \omega C$ which leads to the following analytical solution:

$$Z_L = Z_{in} = \frac{g_o \pm \sqrt{g_o^2 + 4g_m^2 + j4g_m g_o}}{2g_m^2 + 2jg_m g_o} \tag{5}$$

The stage-gain is now easily derived by inspection of Fig. 3.

$$\frac{|V_L|}{|V_{in}|} = \left|1 + j\frac{1}{\omega C \cdot Z_L}\right| = \left|1 + j\frac{1}{g_m Z_L}\right| \tag{6}$$

For an ideal inverter, having a zero output conductance, the load impedance becomes $1/g_m$ and the stage drops from 2 (the unloaded stage-gain) to $\sqrt{2}$. However, a real inverter implemented in CMOS has a non-negligible, signal dependent, g_o which stabilizes the output amplitude of the filter, but makes it difficult to predict the true gain for the whole active polyphase filter by hand. Instead the designer must rely on simulations, using extensive transistor models, in order to achieve the desired filter performance.

Compared to the passive filter in Fig. 1, the active design in Fig. 2 has the reverse phase order due to the inverter function of the transconductors. In order to analyze the quadrature behavior (the phases of V_α and V_β) of the active filter in Fig. 2, a simplified model can be used, see Fig. 4. To better model the behavior of an active transconductor, a phase difference ξ has been introduced between its output current and input voltage. As in Fig. 1, θ represents the input quadrature skew. The output signals V_α and V_β can be expressed

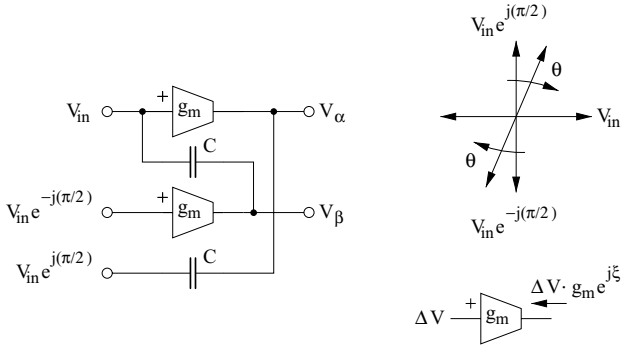

Fig. 4 A model of the g_mC structure, suitable for phase error analysis

as:

$$\begin{aligned} V_\alpha &= V_{in}e^{j(\pi/2-\theta)} - V_{in}g_m e^{j\xi}\frac{1}{j\omega C} \\ &= V_{in}e^{j\pi/2}\left(e^{-j\theta} + \frac{g_m}{\omega C}e^{j\xi}\right) = V_{in}e^{j\pi/2}\cdot Q_\alpha \end{aligned} \tag{7}$$

$$\begin{aligned} V_\beta &= V_{in} - V_{in}e^{-j(\pi/2+\theta)}g_m e^{j\xi}\frac{1}{j\omega C} \\ &= V_{in}\left(1 + \frac{g_m}{\omega C}e^{j(\xi-\theta)}\right) = V_{in}\cdot Q_\beta \end{aligned} \tag{8}$$

For a perfect quadrature output signal, Q_α and Q_β must be equal. In (9) the phases of Q_α and Q_β are examined and after some algebra it can be shown that the phases are identical when $\Gamma = 1$, e.g. when $g_m = \omega C$. This means that the transconductor phase shift ξ and input phase skew θ only affect the absolute phase of the outputs of a perfectly tuned filter.

$$\begin{aligned} \angle Q_{A,V_{in}=\text{ref}} &= \arctan\left(\frac{\Gamma\sin(\xi-\theta)}{1+\Gamma\cos(\xi-\theta)}\right) \\ \angle Q_{B,V_{in}=\text{ref}} &= \arctan\left(\frac{\Gamma\sin(\xi)-\sin(\theta)}{\cos(\theta)+\Gamma\cos(\xi)}\right) \\ \Gamma &= g_m/(\omega C) \end{aligned} \tag{9}$$

3 Inverter-*C* filters

When the transconductor is implemented using a CMOS inverter, depicted in Fig. 5, two major effects must be considered. First, the transconductance will be signal dependent, and thereby time variant. Second, the output conductance, assumed to be zero in the ideal model, will also show a signal dependence. These effects prevent the use of a regular small

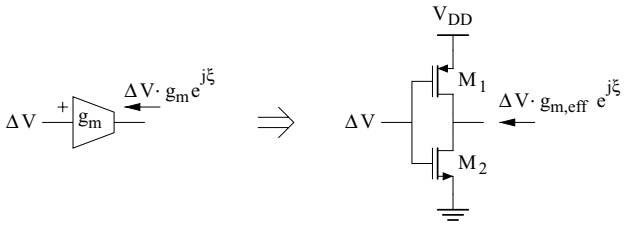

Fig. 5 CMOS inverter implementation. The effective g_m is called $g_{m,\text{eff}}$, and as before ξ indicates the phases difference between the output current and input voltage

signal analysis to understand the filter behavior. In order to analyze the active filter, implemented with CMOS inverters, an effective transconductance (g_m) can be used. By making a periodic steady state (or transient) analysis, the fundamental output current amplitude and the voltage amplitude can be found. From that an effective g_m for the fundamental frequency can be calculated. It is important that the inverter is simulated with the same load and at the same signal level as in the polyphase filter for $g_{m,\text{eff}}$ to be accurate. Since the effective g_m, called $g_{m,\text{eff}}$ from now on, takes all parasitic effects of the inverter into account it can be used to analyze the active filter.

To verify the effective transconductance approach, the active inverter based polyphase filter, called In*C* filter, has been simulated at a low frequency (1 MHz). Both $g_{m,\text{eff}}$ and the output current phase of the inverters can be found by simulation. The quadrature phase error can then be calculated using (7, 8). As can be seen in Fig. 2, the filter is symmetrical and all transconductors are assumed to behave exactly the same. However, when a phase skew (θ) of the input signal is present the inverters must be treated as two pairs, having different $g_{m,\text{eff}}$ and ξ. In Fig. 6 the phase error is depicted for both the passive *RC* implementation and the In*C* structure implemented in a 0.35 μm CMOS process. The input phase skew is $\theta = 2^\circ$ and both filters are tuned to 1 MHz. As can be seen, the two different filter implementations show about the same performance. Also the estimated phase error of the In*C* filter is plotted. The estimation is based on (9) with simulated values of $g_{m,\text{eff}}$ and ξ.

Using the same technique on the passive *RC* filter the effective transconductances of the resistors can be expressed according to (10). As for the In*C* filter, the four resistors can be treated as two pairs, having different effective transconductances. When the filter is tuned and there is no input phase skew ($\theta = 0$), the transconductances all become equal to ωC, which is expected.

$$g_{m1,\text{eff}} = \sqrt{\frac{2(1+\sin(\theta))(\omega C)^2}{1+(\omega RC)^2}}$$
$$g_{m2,\text{eff}} = \sqrt{\frac{2(1-\sin(\theta))(\omega C)^2}{1+(\omega RC)^2}} \tag{10}$$

Figure 7 shows $g_{m,\text{eff}}$ for both an *RC* filter and an In*C* filter as function of frequency. Both filters are tuned to 1 MHz. The behavior of $g_{m,\text{eff}}$ is very similar for the two filters and the static difference is due to the phase shift ξ of the CMOS inverters. The difference between the two $g_{m,\text{eff}}$—pairs is proportional to the input phase skew θ. Since the effective g_m of the inverter can easily be changed by scaling the width of the transistors, the filter can be fine tuned to the correct operating frequency. In Fig. 7 the ideal g_m that would produce perfect quadrature signals at all frequencies is indicated. The ideal g_m is proportional to the frequency. Figure 8 shows a

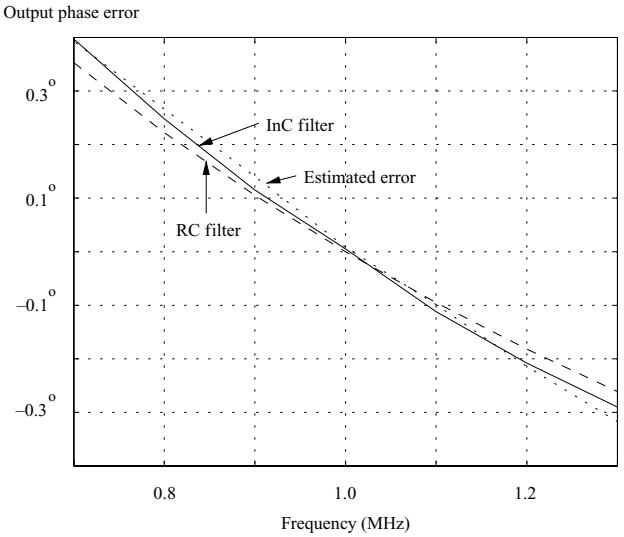

Fig. 6 Simulated phase error for both the *RC* filter and the In*C* filter. The input phase skew is 2°

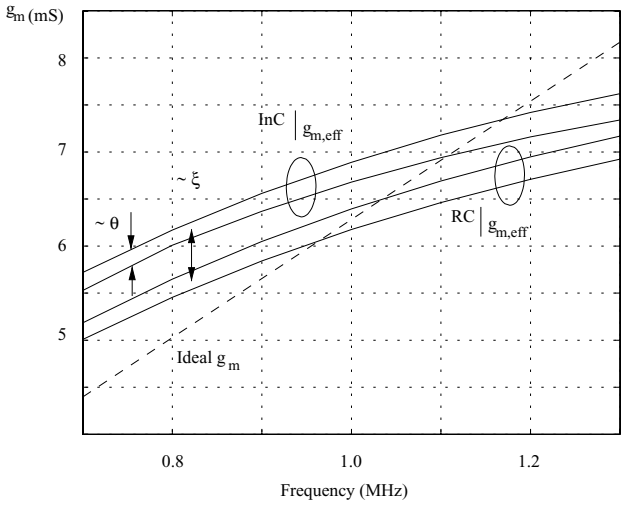

Fig. 7 Effective transconductances as function of frequency for tuned *RC* and In*C* filters (1 MHz). The input phase skew is 2°

Table 1 Summary of simulation results

Tuning range	9.14–10.58 GHz
VCO current (DC)	3.8 mA
Polyphase filter operating current (DC)	10.2 mA
Phase noise at 10 MHz offset	<-160 dBc/Hz (polyphase filter only)
Quadrature error (9.14–10.58 GHz)	$< 0.8^\circ$
Supply voltage	1.2 V
C_A	126 fF
C_B	188 fF
C_c	230 fF
C_{osc}	90 fF
L_{sym}	450 pH
C_L	Transistor gate: 87.2 $\times$ 0.13 μm^2
R_b	10 kΩ
Inverter NMOS transistor	$W = 8\ \mu$m, $L = 0.13\ \mu$m
Inverter PMOS transistor	$W = 16\ \mu$m, $L = 0.13\ \mu$m

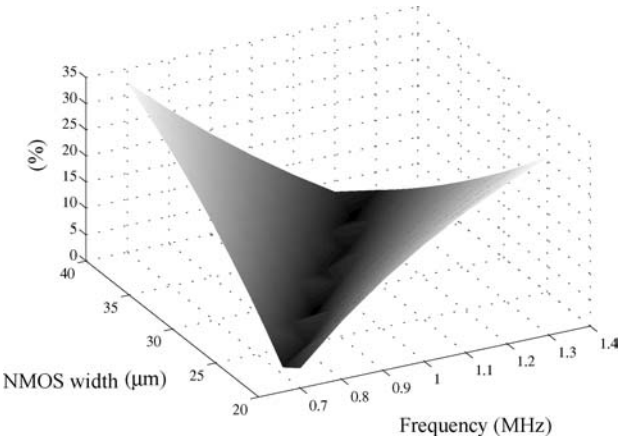

Fig. 8 The remaining quadrature error at the output of the In*C* filter implementation. The PMOS transistor width is set to 2.5 times the NMOS width

simulation of the remaining part of the quadrature error at the In*C* filter output as function of both transistor width and frequency. As can be seen, for a minimum output quadrature error the width should be scaled linearly with frequency. This is expected since the ideal g_m is proportional to the frequency, and the g_m of the inverters is proportional to the transistor width.

4 Simulation of 10 GHz quadrature signal generation in 130 nm CMOS

When used in practice, polyphase filters use cascaded stages in order to achieve larger bandwidth and less sensitivity to process variations. In this design example a 10 GHz quadrature LO signal is generated by a broadband differential VCO and a three stage active polyphase filter, implemented in a standard 0.13 μm CMOS process, see Fig. 9. The first In*C* link (A) generates a coarse quadrature signal, whereas the following In*C* link (B) reduces the quadrature error and makes the filter broadband. The output link is only an inverter

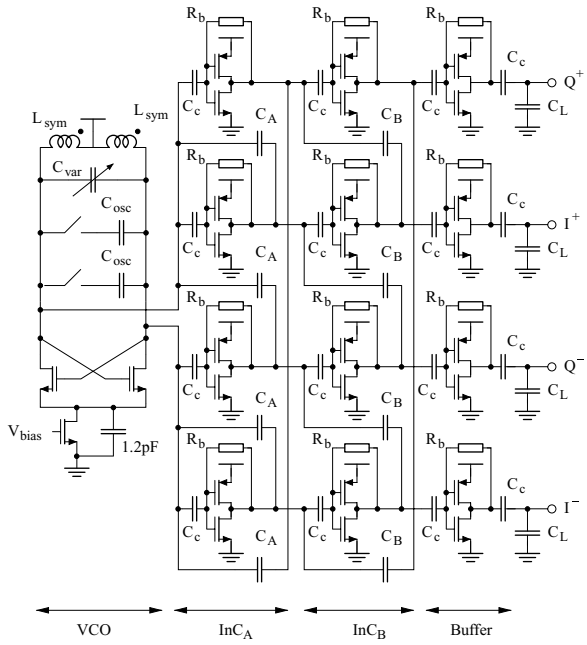

Fig. 9 Architecture of the quadrature LO signal generation. The DC feedback of the inverters, stabilizing the bias point, is included

buffer circuit to improve the VCO isolation. The buffer drives the gates of the transistors in a quadrature passive mixer in the front-end, and the capacitive load is represented by C_L in this example. The VCO is implemented as a differential negative resistance oscillator, using a symmetrical differential inductor and a small CMOS varactor for fine tuning. In order to achieve a broad tuning range two larger capacitors can be switched in and out of the resonance tank as described in [5]. A simulation of the quadrature generation is shown in Fig. 10, where the VCO output amplitude, the polyphase filter output amplitude, and the output quadrature phase error are depicted as functions of the VCO frequency. In order to get realistic results a quadrature passive mixer was used as a load. The tuning range of the VCO is 1.44 GHz, with a center frequency of 9.86 GHz. As expected, the output

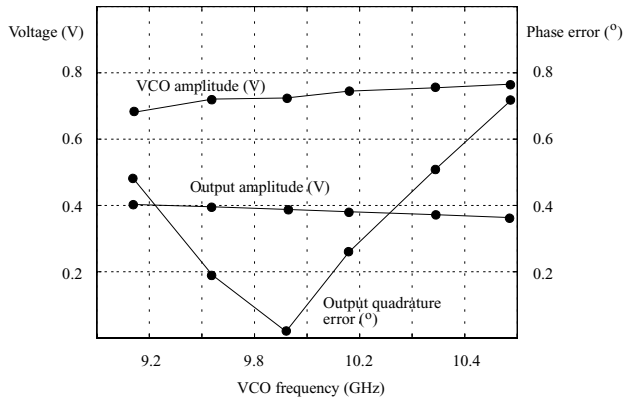

Fig. 10 Simulation of the single ended VCO amplitude, the output amplitude ($Q+$, $Q-$, $I+$, $I-$), and the output quadrature error

amplitude drops with frequency due to the capacitive load of the passive mixers, which adds complexity to the mixer design where there is already a significant trade off between switch transistor width and conversion gain. However, the amplitude drop is only 10% over the whole tuning range, making the conversion loss variation of the mixer small. The quadrature error shows a typical tuned behavior and stays below 0.8° for the complete VCO tuning range. In a filter with this many transistors it is important to investigate the far out phase noise performance, which is important to many radio transceivers. Thanks to the high signal amplitude throughout the filter the noise is low, below −160 dBc/Hz at 10 MHz offset.

5 Summary

In this paper an active polyphase filter architecture for generation of quadrature signals on chip has been presented. It has been shown how the regular *RC* polyphase filter structure can be modified, using inverters instead of resistors. Sufficient gain and isolation can thereby be achieved without additional tuned buffers. By using a differential VCO, without tuned buffers, significant chip area can be saved. Also, since there is no need for additional buffers, this compensates for the power dissipation of the active devices. The technique is exemplified by a simulated 130 nm CMOS 10 GHz design and the performance is summarized in Table 1.

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