Analog Integr Circ Sig Process (2007) 50:163–183
DOI 10.1007/s10470-006-9023-7

Novel input stages for current feedback operational amplifiers

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Received: 28 June 2006 / Accepted: 26 December 2006 / Published online: 30 January 2007
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Abstract This paper considers the trade-offs involved in the design of six new input stages intended to improve the performance of a current feedback operational amplifier (CFOA), over that possible using an established input circuit configuration, with respect to three major characteristics, viz, common mode rejection ratio (CMRR), offset voltage and slew-rate.

Keywords CFOA · CMRR · Bandwidth · Offset-voltage · Slew-rate

1 Introduction

The op-amp has evolved steadily over the years with improved designs from a number of the specialist manufacturers. The conventional op-amp is actually a voltage op-amp (VOA), so named because it has the distinctive characteristic of a high input impedance at both the inverting and non-inverting input terminals, and makes use of voltage feedback when used for linear signal processing applications.

Although attempts have been made to improve the performance of the basic VOA structure, the architecture of the VOA unfortunately has inherent limitations in respect of both the gain-bandwidth trade-off and slew-rate. Typically, the gain-bandwidth product is a constant and the slew-rate is limited to a maximum value determined by the input stage bias current. The slew-rate limitations of the VOA are overcome in a newer architecture op-amp, referred to as the current-feedback op-amp (CFOA) [1, 2], so-called because the feedback signal fed into the low input impedance inverting input terminal is current rather than voltage. Typically, slew-rate values for the CFOA range from 500 V/μs to 2,500 V/μs [3–5], whereas the slew-rates of VOAs are much lower, in the region of 1 V/μs to 500 V/μs. This is a direct result of the use of current as the feedback error signal. An advantage, related to the high slew-rate achieved in the CFOA, is that the bandwidth is almost independent of the closed-loop gain, unlike the VOA where the gain-bandwidth product is constant [5]. This gives the CFOA particular advantages in applications requiring variable closed-loop gains with constant bandwidth, such as in automatic gain control (AGC) systems [5, 6].

Although the idea of the CFOA existed some thirty years ago, it was market demand for video signal processing that stimulated interest in the development of a monolithic CFOA in 1987 by Elantec [7, 8]. A factor that held back the arrival of the CFOA was the lack of an advanced complementary bipolar technology, with PNP transistors providing electrical performances comparable with those of NPN types. The semiconductor technique that now enables this is dielectric isolation, which means that both PNP and NPN devices can be fabricated as vertical transistors, and hence offer similar performance characteristics [3, 7].

Unfortunately, the CFOA exhibits relatively poor DC precision, compared with that of the VOA. However, the nature of many high frequency applications is such that this precision may not be a problem with the result that the very high inherent slew-rate puts the CFOA in the spotlight [3].

The CFOA can offer considerable performance advantages when used to realise IF and RF applications [9]. Moreover, the CFOA is absolutely necessary to digital engineers who are involved in the design of high-speed analog-to-digital conversion systems, since these depend heavily on a sampling process in order not to obscure

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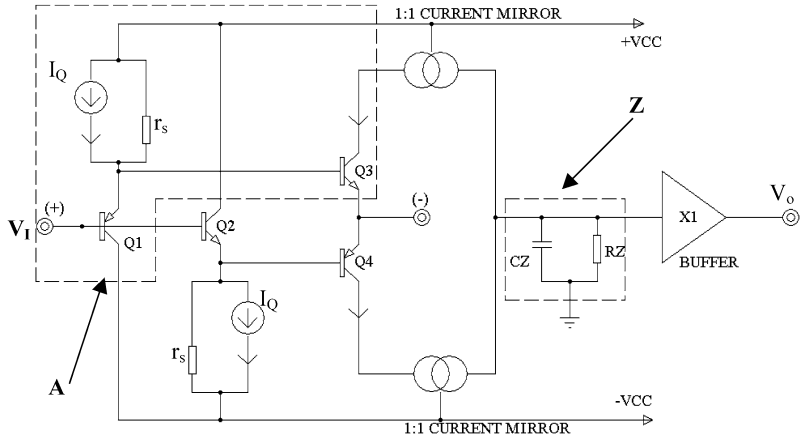


Fig. 1 Schematic of an established CFOA architecture

information [10, 11]. The CFOA delivers a high slew-rate and, as such, is the most suitable op-amp for this operation.

For video-systems engineers there are two important specifications to be considered, namely, (i) the differential gain (DG), and (ii), the differential phase (DP) [5]. DG and DP are two figures-of-merit of an op-amp that relate to the incremental change in closed-loop gain and phase resulting from a change in input and output, referenced to zero volts for a specific frequency. The DG and DP of most VOAs are not constant when varying DC offsets are added to a constant-frequency AC input signal [5]. This can cause problems when processing composite video signals, with picture distortion occurring if the DG and DP are too high. Thanks mainly to circuit topology, the typical CFOA exhibits a much better DG and DP performance than the typical VOA, thus making the CFOA an excellent amplifier for dealing with composite video signals [12, 13]. The other significant application areas for the CFOA are in high speed active-filter design, and line drivers [14].

Despite the many advantages of the CFOA over the VOAs, there exist certain limitations, one of which is the common-mode rejection ratio. The CMRR of CFOAs is generally quite poor, mainly because of the asymmetrical nature of the complementary-pair input stage, and the fact that input bias currents are unequal and uncorrelated. This paper is primarily concerned with circuit techniques for improving the CMRR [12, 14].

2 An established input architecture

For comparison purposes, the schematic circuit of an established CFOA architecture is shown in Fig. 1 [15].

For simplicity in a first-order analysis, the NPN and PNP transistors are assumed to have identical characteristics. Within the contour A, Q_1 together with its emitter load (bias current source I_Q with output resistance r_s) and Q_3 comprise an input 'half-circuit' and it is the half-circuit concept that is explored further in this paper. The other half-circuit, comprising Q_2 and its emitter load and Q_3, behaves in an identical, complementary, manner. Consider, first, the CMRR, ρ.

Figure 2, in which diode D_1 represents the base-emitter junction of Q_1, shows an equivalent circuit for A when a common-mode input signal, $v_{\rm cm}$, is applied. As far as the change, i, in the collector current of Q_3 is concerned, the circuit behaves like a 1:1 current mirror in which the effective rail supply is decreased in amount by $v_{\rm cm}$, so, i comprises two components, viz, $-(v_{\rm cm}/r_s)$ due to the current change in D_1 and $-(v_{\rm cm}/r_o)$ due to the change in collector emitter voltage across the common-emitter collector output resistance, r_o, of Q_3. Thus:

$$i = -v_{cm}\left(\frac{1}{r_s}+\frac{1}{r_o}\right) \tag{1}$$

This neglects the current change in the collector-base resistance, r_μ, of Q_3 but since $r_\mu \gg r_o$ [16], that is negligible.

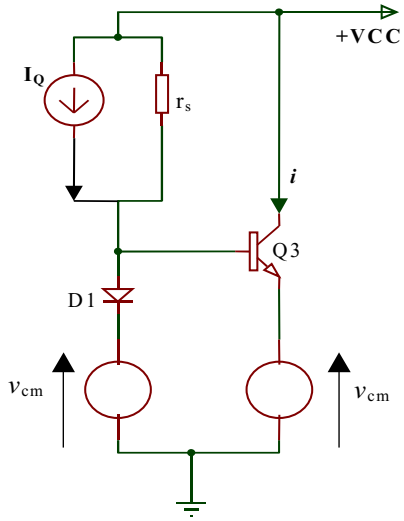


Fig. 2 Representation of section A, for common mode signal $v_{\rm cm}$

The common-mode current, i_{cm}, flowing in load impedance Z, in Fig. 1, after being transmitted via the 1:1 current mirrors CM1, CM2 is double that given in Eq. (1), because of the complementary action of Q_2, Q_4 Hence,

$$g_{Tc} = \left|\frac{i_{cm}}{v_{cm}}\right| = 2\left(\frac{1}{r_s} + \frac{1}{r_o}\right) \tag{2}$$

Figure 3 shows the equivalent circuit for A when a differential-mode signal, v_{dm}, is applied. Again, i has two major components, one due to change in base-emitter voltage ($\cong v_{dm}$), the other due to change in collector-emitter voltage of Q_3

$$i \cong v_{dm}\left(g_m + \frac{1}{r_o}\right) \tag{3}$$

In this equation g_m (the transconductance of Q_3) $= I_Q/V_T$, V_T ($=KT/q$) being the 'thermal voltage' (≈ 25 mV at room temperature). As with i_{cm}, i_{dm} is double that given by Eq. (3)

$$g_{Td} = \left|\frac{i_{dm}}{v_{dm}}\right| \approx 2\left(g_m + \frac{1}{r_o}\right) \approx 2g_m \tag{4}$$

The approximation is valid as $g_m \gg 1/r_o$ where, $r_o = V_A/I_Q$, V_A ($\gg V_T$) being the Early voltage. From Eqs. (2) and (4);

$$\rho = \frac{g_{Td}}{g_{Tc}} \approx \frac{g_m}{\left(\frac{1}{r_s} + \frac{1}{r_o}\right)} \tag{5}$$

For the special case $r_s = r_o$,

$$\rho \approx \frac{V_A}{2V_T} \tag{6}$$

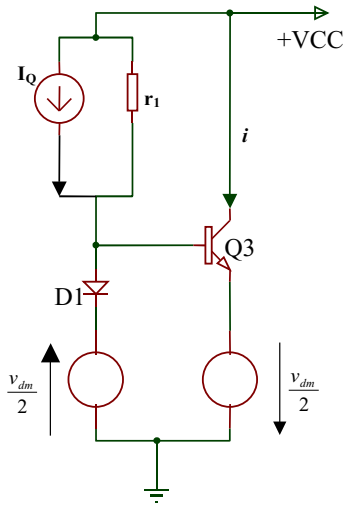


Fig. 3 Representation of section A, for differential-mode signal v_{dm}

This equation is applicable when I_Q is the output of a simple current mirror, as is meant to be the case for Fig. 1. Simulation tests show that doubling V_A doubles ρ [17].

Consider, next, the offset voltage, V_{os}. This is the voltage at the emitter of Q_3 when Fig. 1 is connected as a unity-gain follower (V_o connected to the inverting input) and V_I is set to zero. Ideally $V_{os} = 0$, but in reality V_{os} is finite (a few mV) because of mismatch in the V_{BE}s of Q_1, Q_3.

Finally, consider the slew-rate, SR. This, like V_{os}, is measured in the unity-gain configuration with a resistance (typically between 750 Ω and 2 kΩ for 15 V rail supplies) [18] connected between V_o and the inverting input, when a positive-going voltage step is applied at the non-inverting input. Transistors Q_1 and Q_4 in Fig. 1 tend to switch off and the SR is limited by the current, I_Q, available at the base of Q_3.

3 Improved half-circuits

In the replacement for A (of Fig. 1) in the circuits that follow, r_s is maximised by having I_Q supplied by a cascode source referenced to the rail supplies, and r_o, is made to appear larger by employing a bootstrapped cascode transistor Q_5.

The bootstrapping technique typifies the configuration. Type 1 circuits are exemplified in Figs. 4–6. In these the base of Q_5 is bootstrapped to the inverting input, which follows the non-inverting input in normal CFOA operation: a suggested name for this is 'reverse bootstrapping'. The output resistance at the collector of Q_5 is approximately equal to $\beta V_A/I_Q$ (β being the common emitter current gain of Q_5). This replaces r_o, in Eq. (5); consequently ρ increases by a factor β. The V_{os}, however, is poor in half-circuit B because of practical mismatch in the V_{BE} of Q_1 and Q_3. This is remedied in half-circuit C, in which Q_1 is now an NPN transistor, diode-strapped. In half-circuit D, the diode-strapped transistor of Fig. 5 functions as a normal transistor

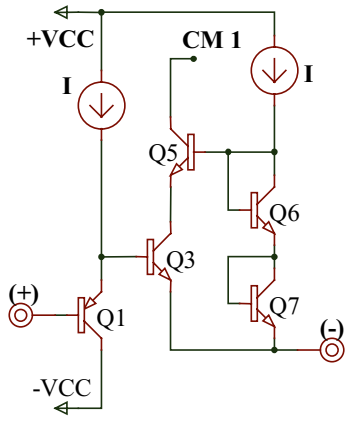


Fig. 4 Half-circuit B

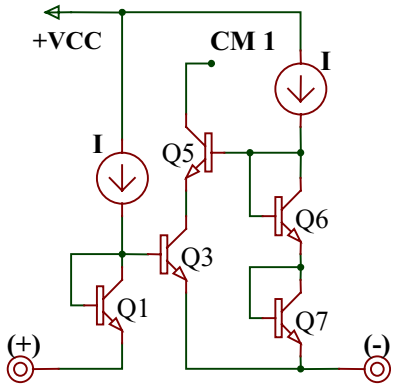


Fig. 5 Half-circuit C

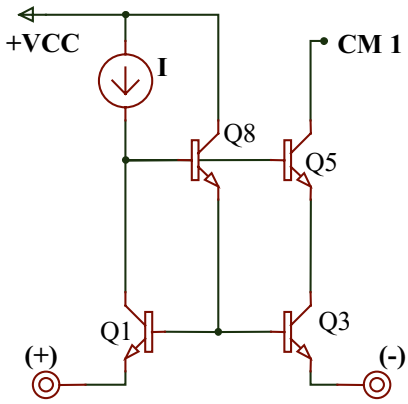


Fig. 8 Half-circuit F

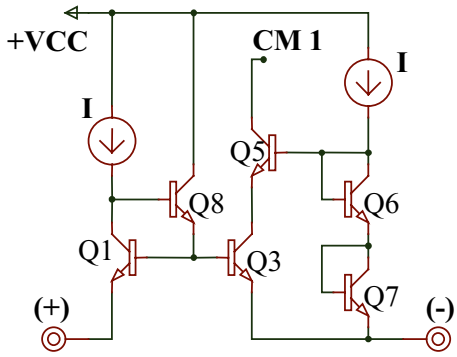


Fig. 6 Half-circuit D

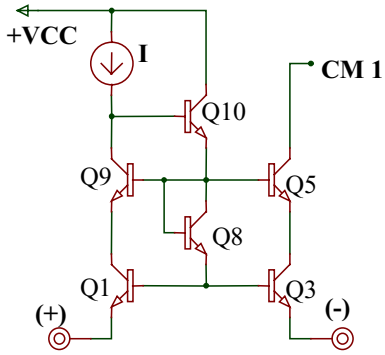


Fig. 9 Half-circuit G

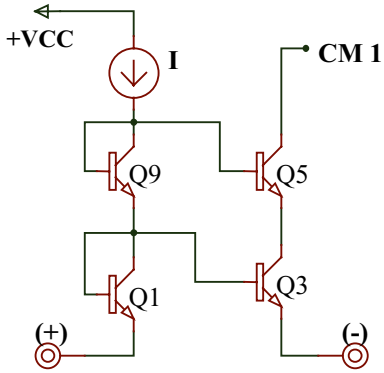


Fig. 7 Half-circuit E

and the emitter-follower Q_8 increases the SR by making more current available at the base of Q_3.

Type 2 circuits are-exemplified in Figs. 7–9, in which the base of Q_5 is driven from the non-inverting input ('forward-bootstrapping') Figs. 8, 9, like Fig. 7, employ emitter-followers to drive the base of Q_3 for increased SR. In Fig. 9, Q_1 and Q_3 both operate at the same V_{CB} (≈ 0), as well as the same collector current, to ensure a very low V_{os}. Note that, for a given I_Q, half-circuit A requires the minimum input d.c. bias current. In all the half-circuits, except A, the vertical stacking of transistors necessary to improve the performance parameters detracts from the dynamic output voltage swing of the CFOA because of V_{BE} summation.

We now consider the design of CFOAs that incorporate these six new input circuits. The performance of each new CFOA is compared with that of the basic one shown in Fig. 1. OrCAD PSpice was used to verify the operation and performance of the circuits. The technology used in the simulation was the complementary bipolar XFCB process of Analog Devices, Santa Clara, California.

In all the new designs, unless otherwise indicated, the main current biasing circuitry is the same as that used in Fig. 10. Furthermore, all simulation measurements refer to $I_Q = 0.2$ mA, $V_{CC} = \pm 5$ V, at room temperature (27°C).

4 Reverse bootstrapping

4.1 Performance with half-circuit B

In Fig. 10, the buffered current mirrors, $(Q_7 + Q_8 + Q_9 + Q_{17} + Q_{21})$ and $(Q_5 + Q_6 + Q_{10} + Q_{18} + Q_{26})$ are supplied

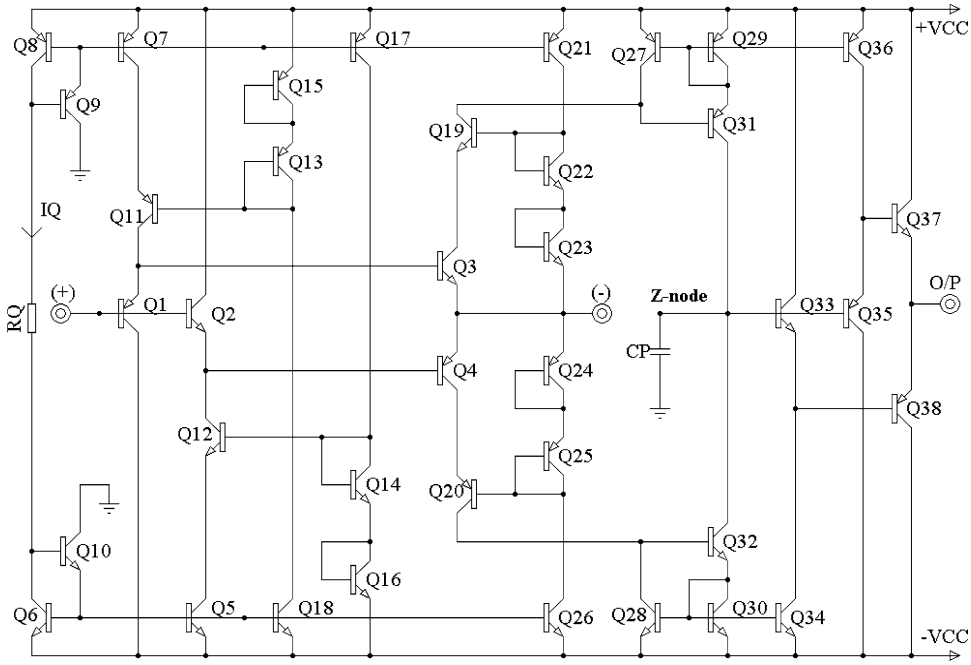


Fig. 10 A CFOA using half-circuit B

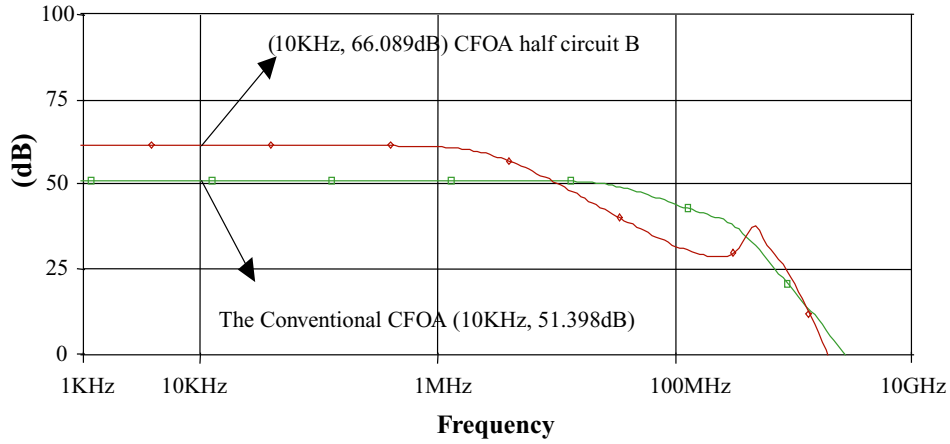


Fig. 11 CMRR ∼ Frequency

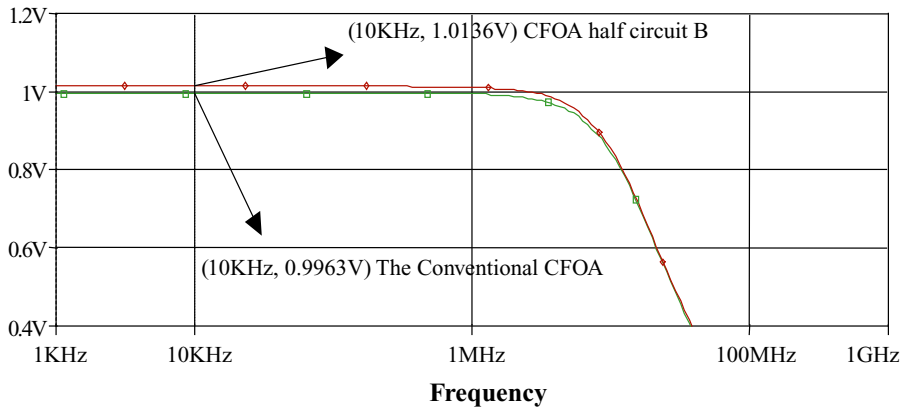


Fig. 12 AC gain accuracy ∼ Frequency

with a common input current, I_Q, via the resistor R_Q. Since the operation of the two buffered-mirrors is the same, only one is considered here, $(Q_7 + Q_8 + Q_5 + Q_{17} + Q_{21})$. The output from Q_7 supplies the cascode transistor Q_{11} with the emitter current for Q_1. The base bias voltage for Q_{11} is provided by the voltage drop across the series connected and diode-strapped transistors Q_{15}, Q_{13} the biasing current for which is supplied by an output of Q_{18} in the other buffered

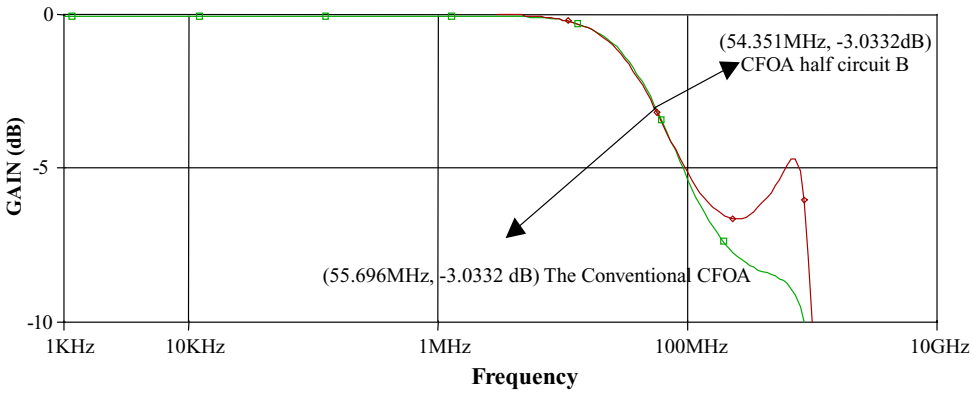


Fig. 13 Frequency responses for unity closed-loop gain

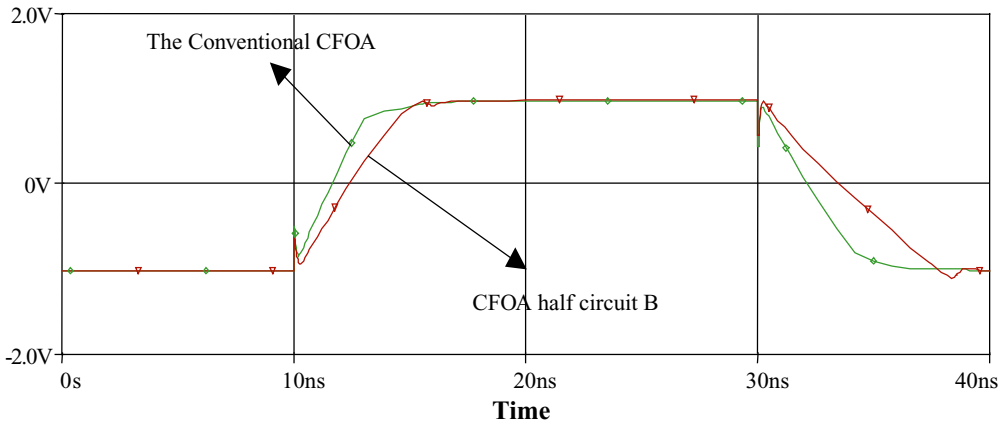


Fig. 14 Transient response

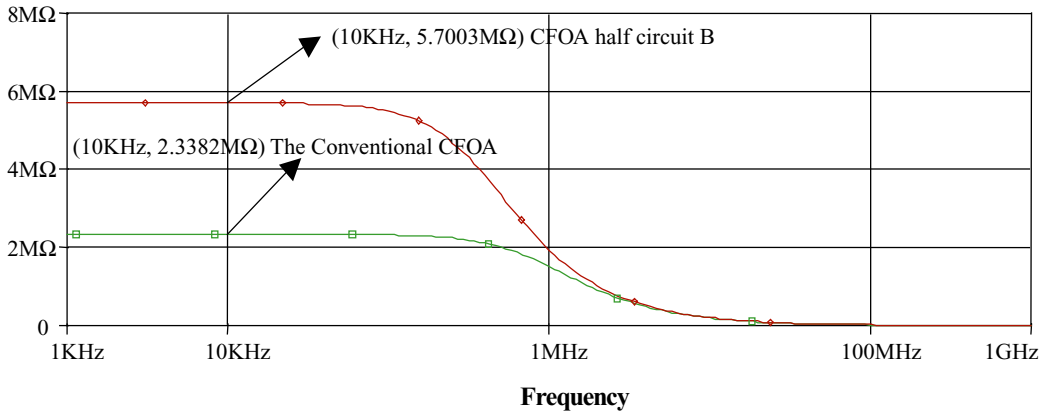


Fig. 15 Input impedance∼frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

current- mirror. The cascoding of Q_7 ensures greater constancy in the emitter current of Q_1 as the input voltage changes: it results in a better CMRR and less variation of incremental input resistance over the input voltage range. The output from Q_{17} supplies current for the bias circuitry of cascode transistor Q_{12} and the output from Q_{21} supplies biasing current for Q_{22}, Q_{23} connected to the base of cascode transistor Q_{19} in the reverse-bootstrapping scheme [19].

4.2 Performance with half-circuit C

The circuit diagram of a CFOA using half-circuit C is shown in Fig. 17, and should be compared with that using the half-circuit B, shown in Fig. 10. A significant difference between the two input circuits of the CFOAs is the use of NPN transistors for both Q_1 and Q_3, and the application of the input signal to the emitter of Q_1 rather than its base. Similarly,

Table 1 Characteristics of the conventional and the improved CFOA using half-circuit B

Parameter	Conventional CFOA [15]	CFOA using half circuit B (Fig. 10)
CMRR	51.4 dB	66.1 dB
Bandwidth	55.7 MHz	54.4 MHz
Inverting input resistance (at 0 V d.c. input)	68.7 Ω	87.2 Ω
Non-inverting buffer input resistance (at 0 V d.c. input)	2.3 MΩ	5.7 MΩ
AC gain error (Unity gain, Vin = 1 V pp)	3.7 mV	13.6 mV
Input offset voltage (at 0 V d.c. input)	±20.6 mV	±24.45 mV
Slew rates	SR+ = 569.6 (V/μs)	SR+ = 400.7 (V/μs)
	SR− = 454.2 V/μs	SR− = 245.3 V/μs
Input dynamic range	−3 V, +3 V	−2.6 V, +2.4 V

Discussion:

The CMRR in CFOA half-circuit B has been increased, to about 66.1 dB (in the conventional CFOA it is 51.4 dB). This increase justifies the earlier discussion. However, improvement in the CMRR has been achieved at the expense of a reduction in slew-rate performance and input dynamic range.

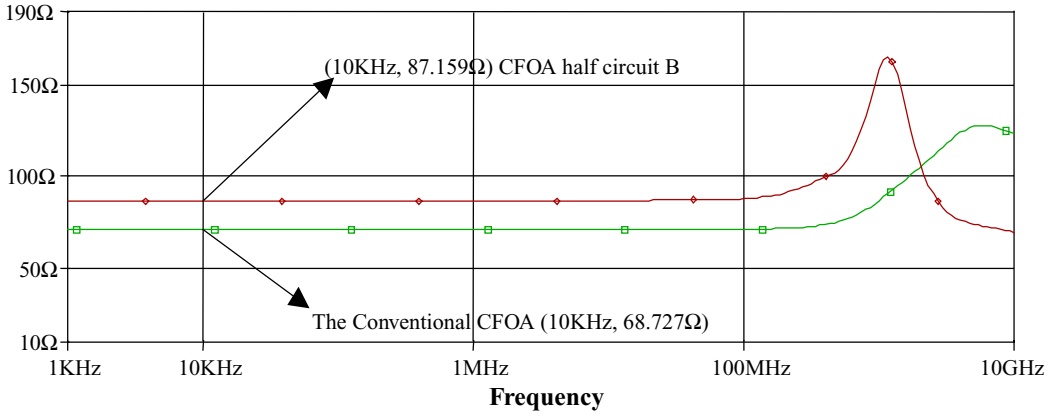


Fig. 16 Input impedances (inverting)∼Frequency

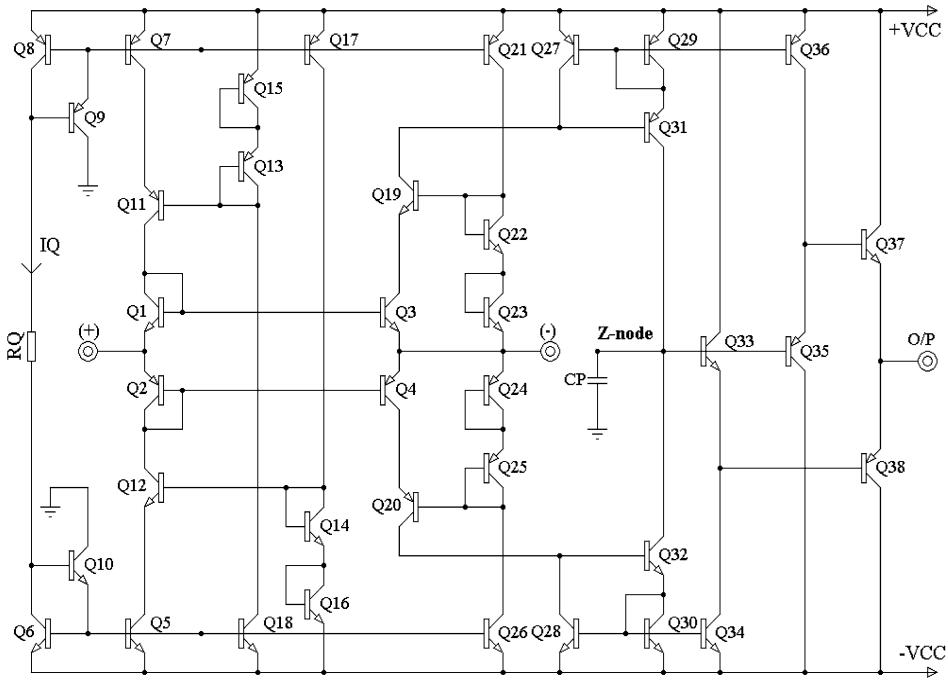


Fig. 17 A CFOA using half-circuit C

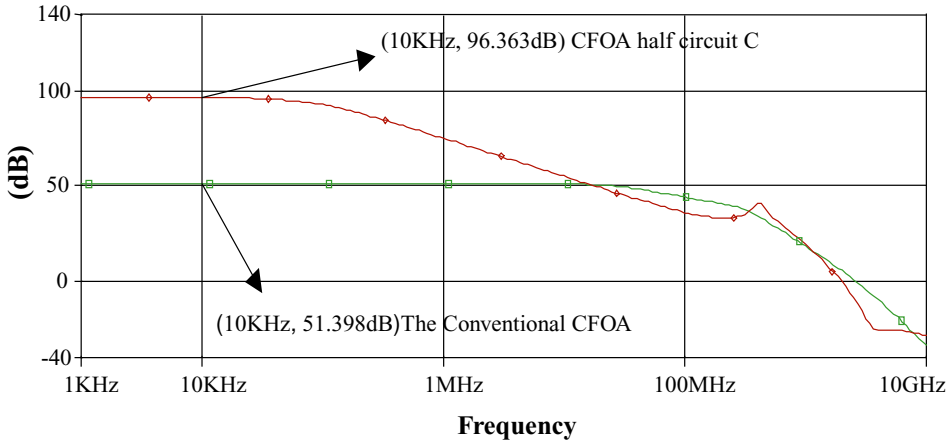


Fig. 18 CMRR ~ Frequency

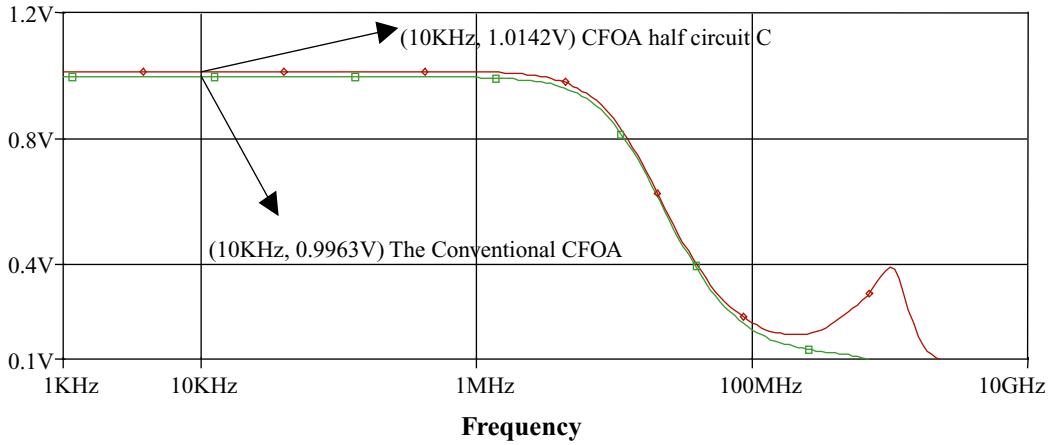


Fig. 19 AC gain accuracy ~ Frequency

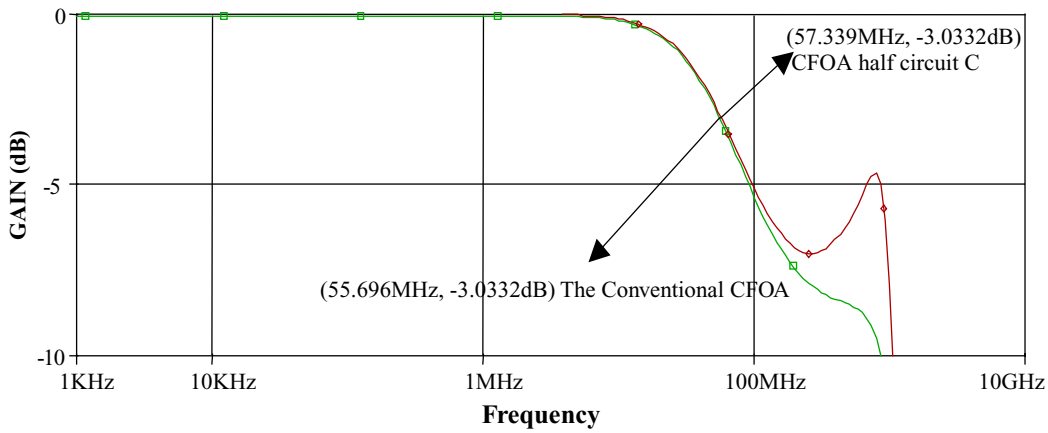


Fig. 20 Frequency responses for unity closed-loop gain

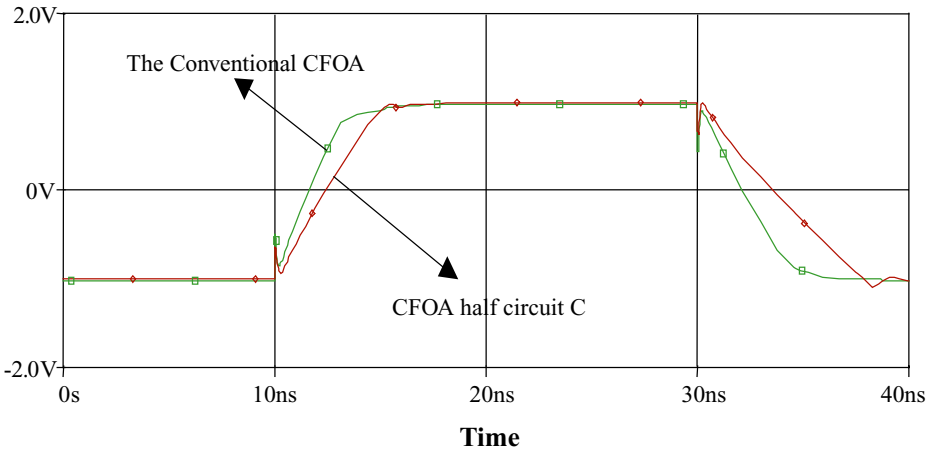


Fig. 21 Transient response

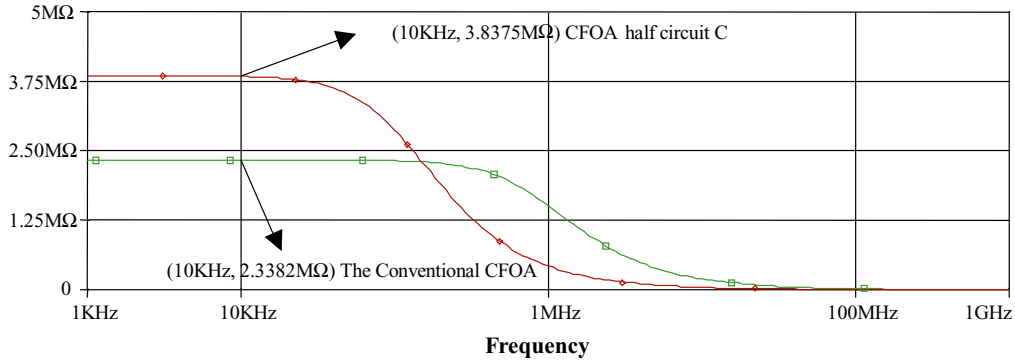


Fig. 22 Input impedance ∼ frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

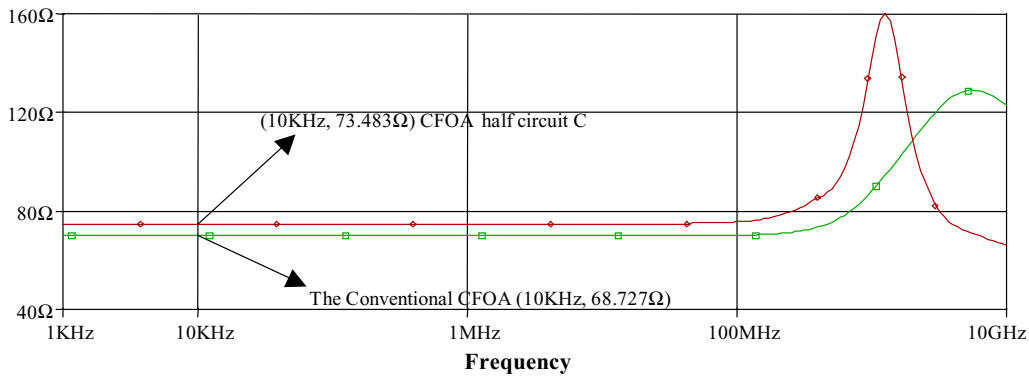


Fig. 23 Input impedance (inverting) ∼ Frequency

Q_2, Q_4 are both PNP transistors and the input applied to the emitter of Q_2 rather than its base. Furthermore, Q_1, Q_2 are now strapped to operate as diodes. From Fig. 17, it follows that the DC voltage difference from the (+) to (−) is first increased (decreased) by V_{BEQ1} (V_{BEQ2}), and then decreased (increased) by V_{BEQ3} (V_{BEQ4}) [20], thus,

$$V_{\mathrm{os}} = |V_{\mathrm{BEQ_1}} - V_{\mathrm{BEQ3}}| = |V_{\mathrm{EBQ2}} - V_{\mathrm{EBQ4}}| \tag{7}$$

Because the matching between the same-type transistors (NPN or PNP) is good, a better V_{OS} can be achieved.

4.3 Performance with half-circuit D

See Table 3.

5 Forward bootstrapping

5.1 Performance with half-circuit E

The biasing scheme is that used in previous designs, but the cascode transistors for Q_3, Q_4 do not, of course, require the same level of bias currents as are necessary for reverse bootstrapping.

Table 2 Characteristics of the conventional and the improved CFOA using half-circuit C

Parameter	Conventional CFOA [15]	CFOA using half circuit C (Fig. 17)
CMRR	51.4 dB	96.4 dB
Bandwidth	55.7 MHz	57.3 MHz
Inverting input resistance (at 0 V d.c. input)	68.7 Ω	73.5 Ω
Non-inverting buffer input resistance (at 0 V d.c. input)	2.3 MΩ	3.8 MΩ
AC gain error (Unity gain, Vin = 1 V pp)	3.7 mV	14.2 mV
Input offset voltage (at 0 V d.c. input)	±20.6 mV	±15.3 mV
Slew rates	SR+ = 569.6 V/μs	SR+ = 385.8 V/μs
	SR− = 454.2 V/μs	SR− = 252.9 V/μs
Input dynamic range	−3 V, +3 V	−2.4 V, +2.3 V

Discussion:

The problem of having to match NPN transistors Q_2, and Q_3, to PNP transistors Q_1, and Q_4 in Fig. 10 has been reduced by using, instead, the diode-connected transistors Q_1 (NPN), and Q_2 (PNP) In Fig. 17. Thus, the DC offset-voltage is significantly reduced in the CFOA using half-circuit C to ±15.3 mV from the larger ±24.45 mV, ±20.6 mV of the CFOA using half-circuit B, and the conventional CFOA, respectively. However, of greater importance is the dramatic increase in CMRR.

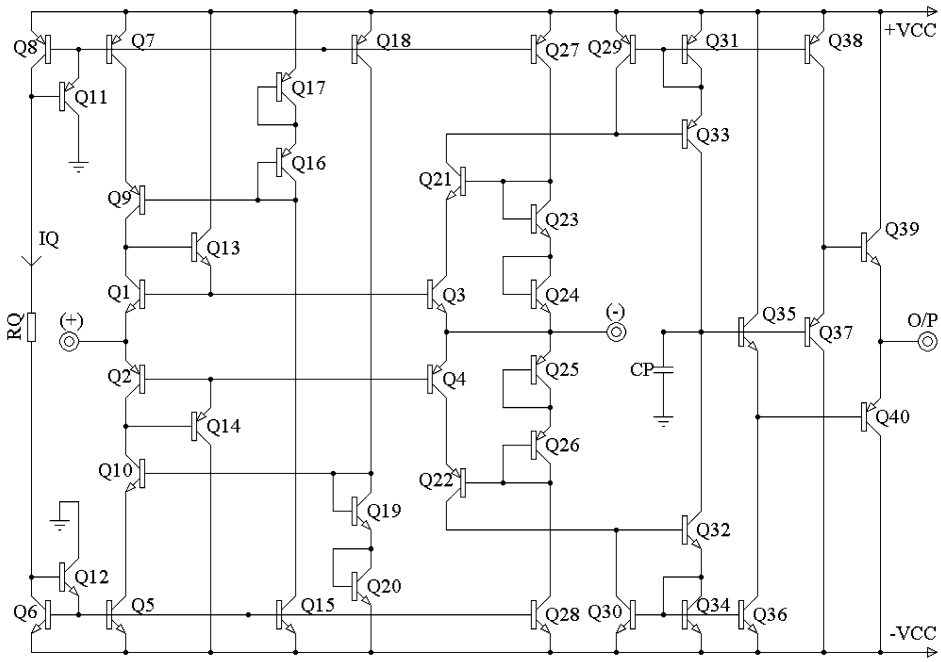


Fig. 24 A CFOA using half-circuit D

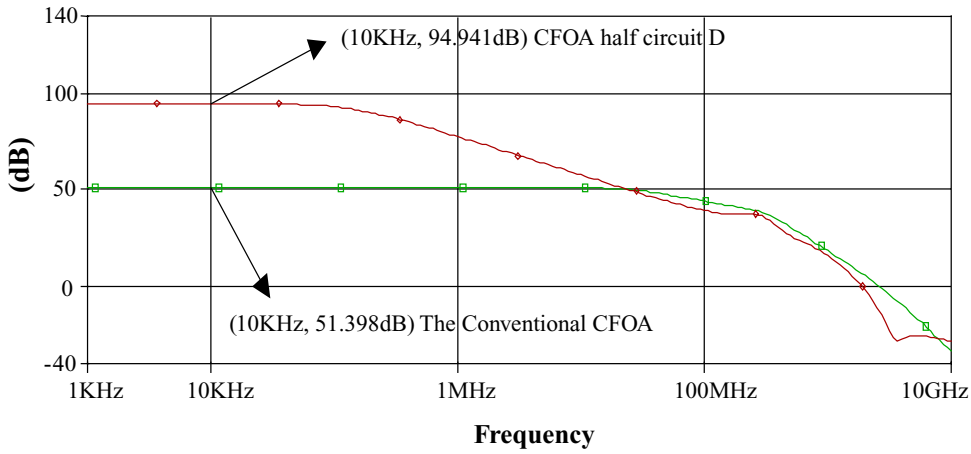


Fig. 25 CMRR ∼ Frequency

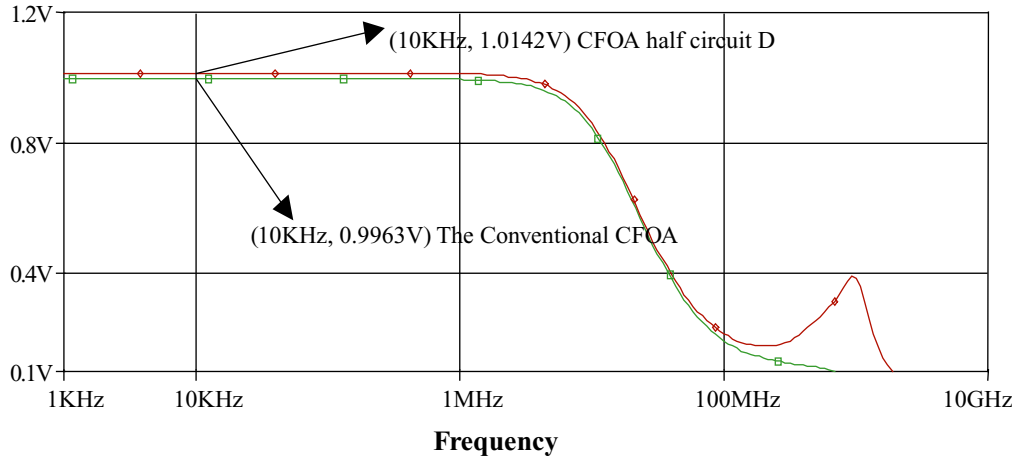


Fig. 26 AC gain accuracy ~ Frequency

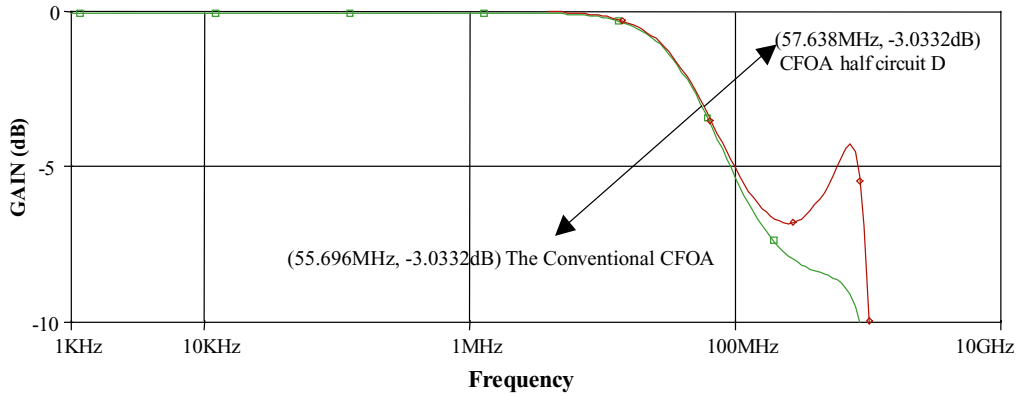


Fig. 27 Frequency responses for unity closed-loop gain

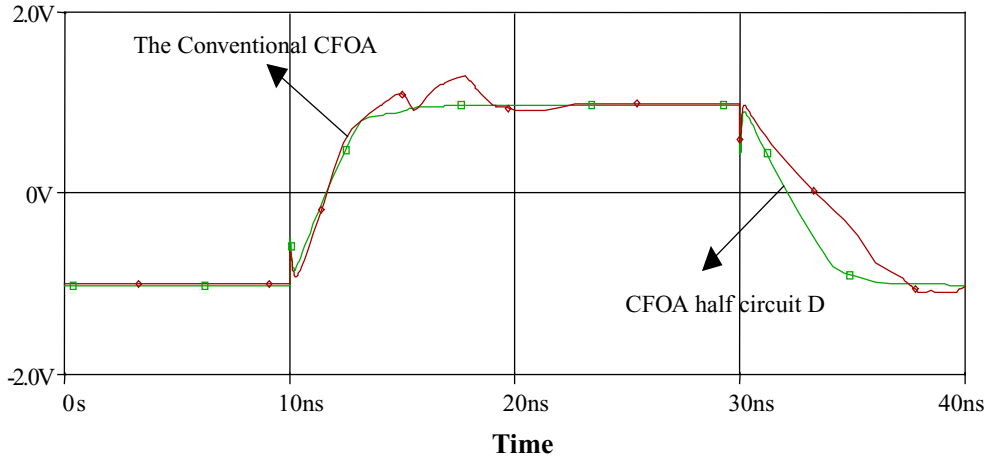


Fig. 28 Transient response

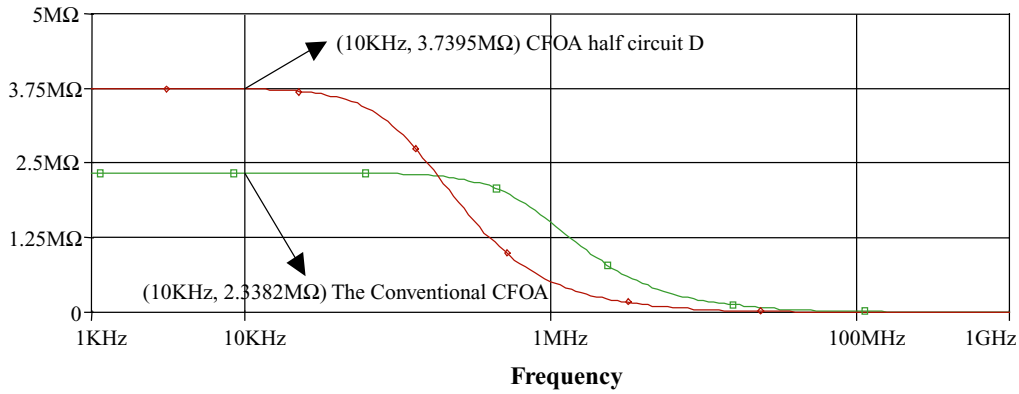
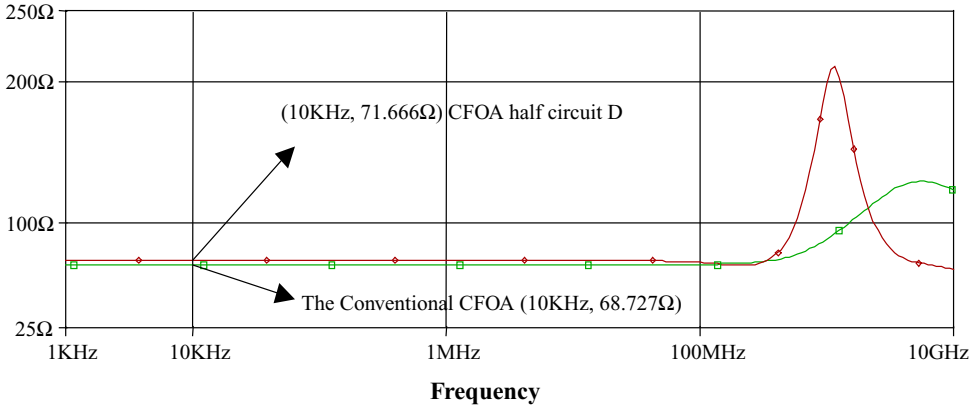


Fig. 29 Input impedance ~ frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

Fig. 30 Input impedance (inverting) ~ Frequency



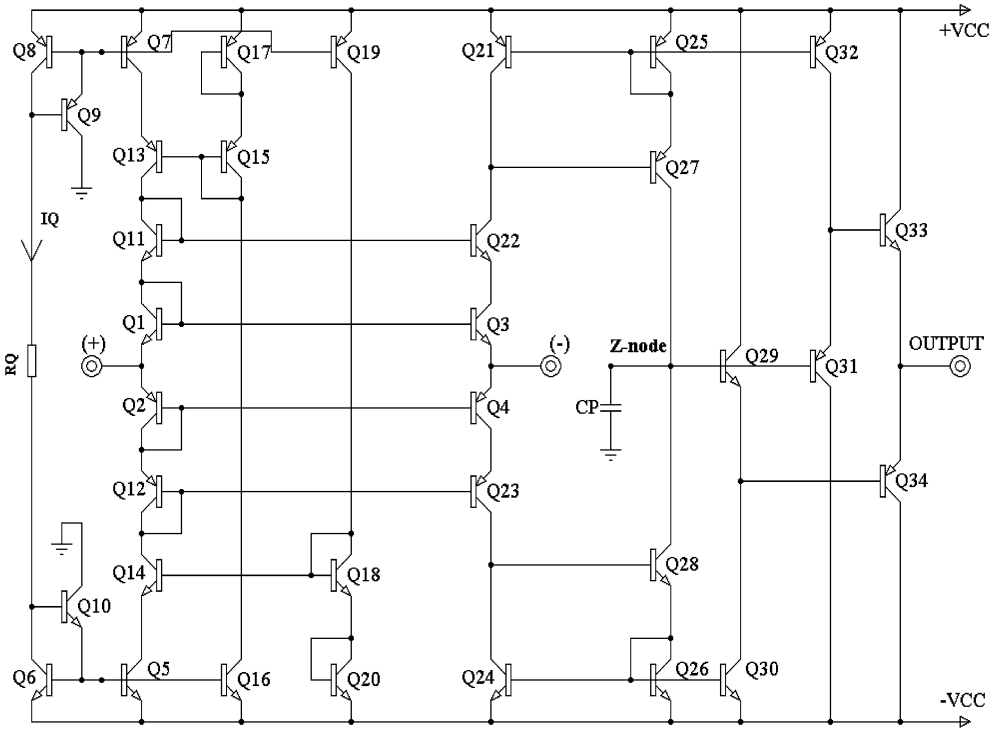


Fig. 31 A CFOA using half-circuit E

Table 3 Characteristics of the conventional and the improved CFOA using half-circuit D

Parameter	Conventional CFOA [15]	CFOA using half circuit D (Fig. 24)
CMRR	51.4 dB	95 dB
Bandwidth	55.7 MHz	57.6 MHz
Inverting input resistance (at 0 V d.c. input)	68.7 Ω	71.7 Ω
Non-inverting buffer input resistance (at 0 V d.c. input)	2.3 MΩ	3.7 MΩ
AC gain error (Unity gain, Vin = 1 V pp)	3.7 mV	14.2 mV
Input offset voltage (at 0 V d.c. input)	±20.6 mV	±11.5 mV
Slew rates	SR+ = 569.6 V/μs	SR+ = 750.3 V/μs
	SR− = 454.2 V/μs	SR− = 272.6 V/μs
Input dynamic range	−3 V, +3 V	−2.1 V, +2.1 V

Discussion:

A comparison of the entries in Table 3 with these in Table 2 justifies the inclusion of emitter-follower drive (via Q_{13}, Q_{14} in Fig. 17) to increase Slew Rate. For some unexplained reason, SR- only increases marginally. Apart from that, the parameters for half-circuits C and D are virtually the same, through input dynamic range for the CFOA using half-circuit D is reduced because of the added V_{BE} drop of Q_{13}.

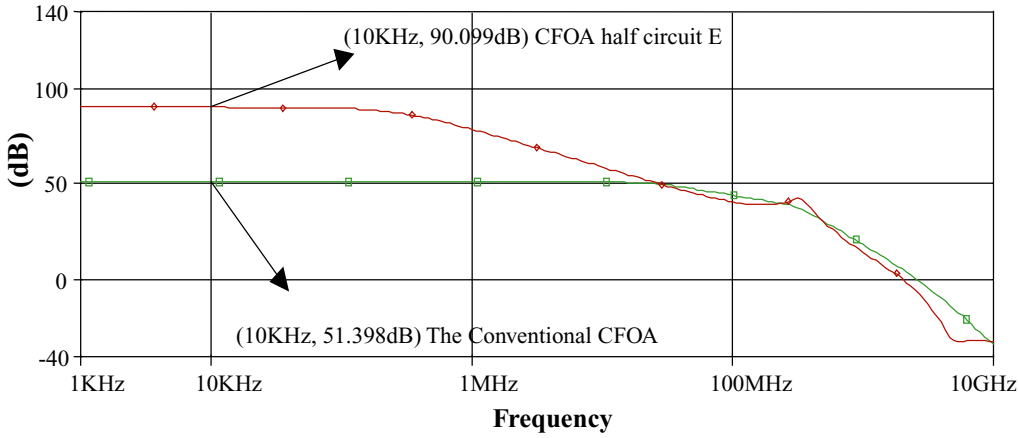


Fig. 32 CMRR ~ Frequency

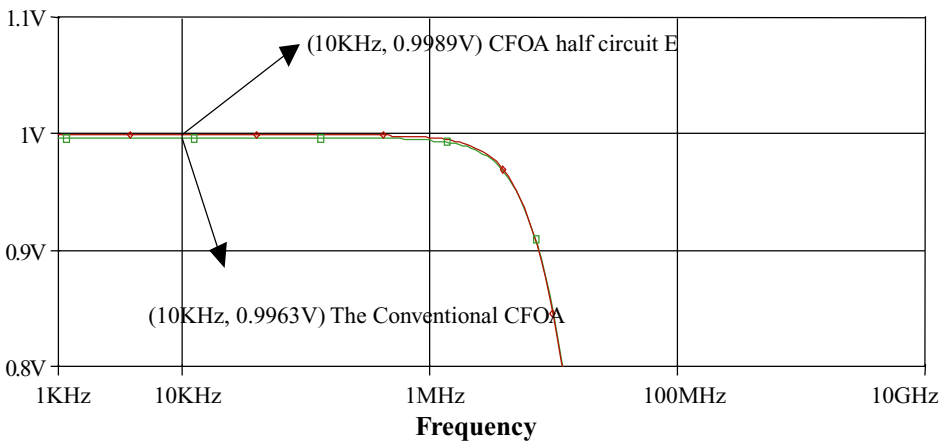


Fig. 33 AC gain accuracy ~ Frequency

5.2 Performance with half-circuit F

This differs from half-circuit E in that Q_{11}, Q_{12} now function as emitter-follower transistors rather than diodes

5.3 Performance with half-circuit G

The architecture in this is based on the design and use in a repeated pattern of a current-transfer cell.

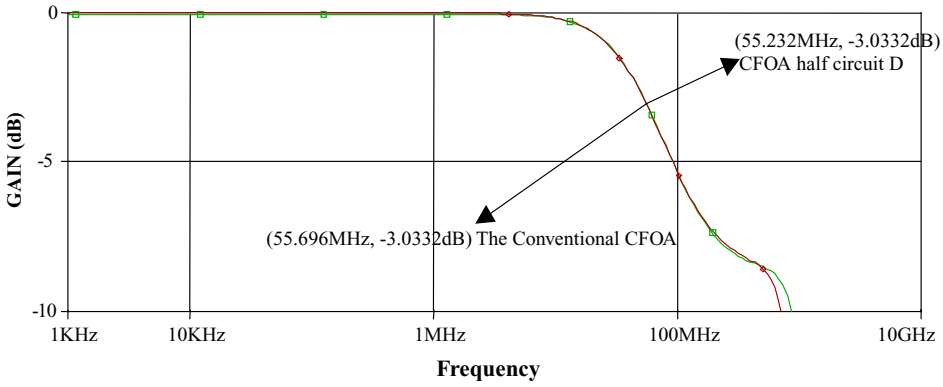


Fig. 34 Frequency responses for unity closed-loop gain

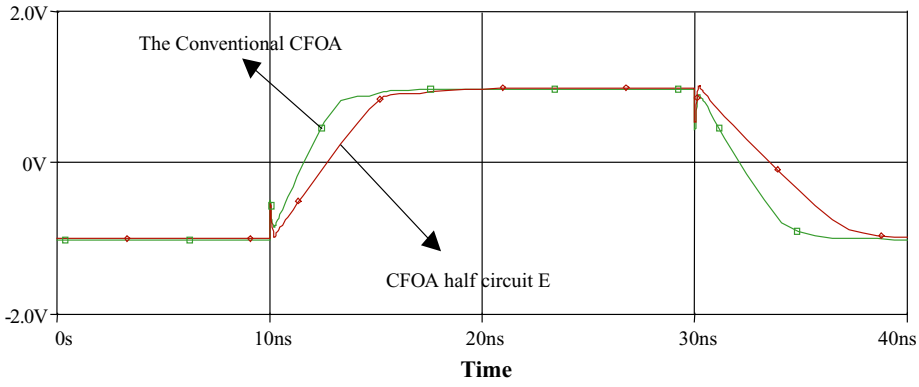


Fig. 35 Transient response

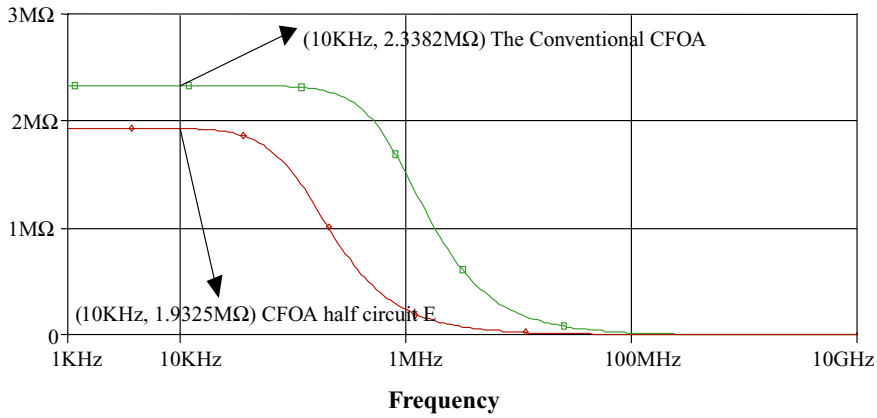


Fig. 36 Input impedance ~ frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

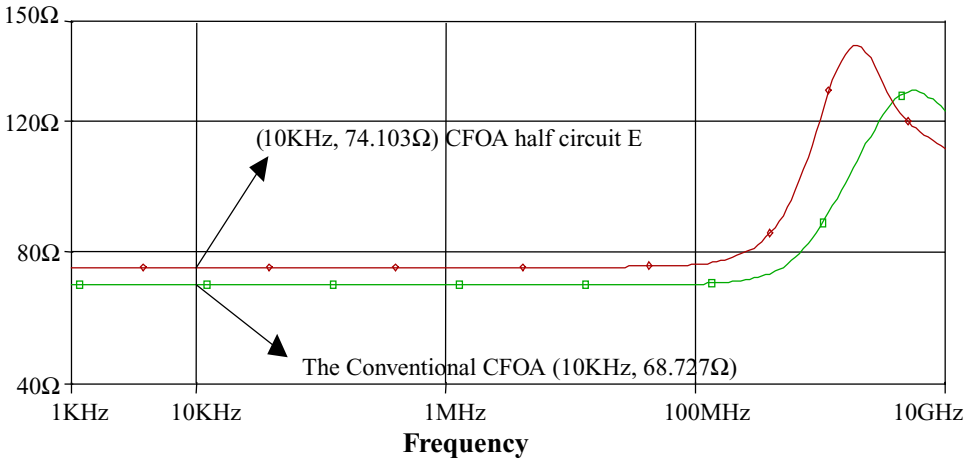


Fig. 37 Input impedance (inverting) ~ Frequency

Table 4 Characteristics of the conventional and the improved CFOA using half-circuit E

Parameter	Conventional CFOA [15]	CFOA using half circuit E (Fig. 31)
CMRR	51.4 dB	90.1 dB
Bandwidth	55.7 MHz	55.2 MHz
Inverting input resistance (at 0 V d.c. input)	68.7 Ω	74.1 Ω
Non-inverting buffer input resistance (at 0 V d.c. input)	2.3 MΩ	1.9 MΩ
AC gain error (Unity gain, Vin = 1 V pp)	3.7 mV	1.1 mV
Input offset voltage (at 0 V d.c. input)	±20.6 mV	±3.45 mV
Slew rates	SR+ = 569.6 V/μs	SR+ = 357.1 V/μs
	SR− = 454.2 V/μs	SR− = 282.5 V/μs
Input dynamic range	−3 V, +3 V	−2.4 V, +2.3 V

Discussion

The AC gain-error and the offset-voltage improvement in half-circuit E are mainly due to the close matching between the NPN transistors Q_1, Q_3, Q_{11}, Q_{22}, and between the PNP transistors Q_2, Q_4, Q_{12}, Q_{23}.

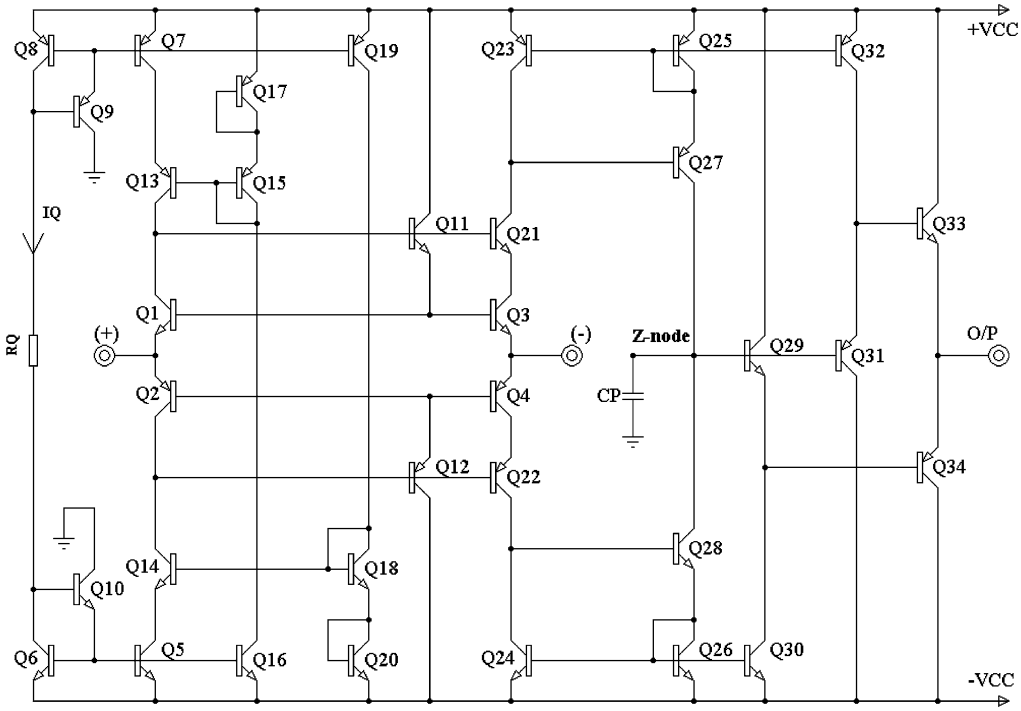


Fig. 38 A CFOA using half-circuit F

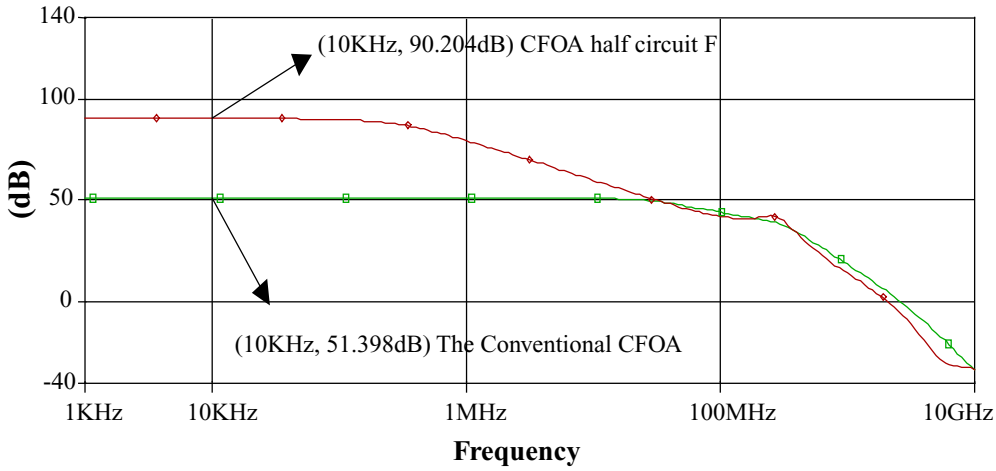


Fig. 39 CMRR ∼ Frequency

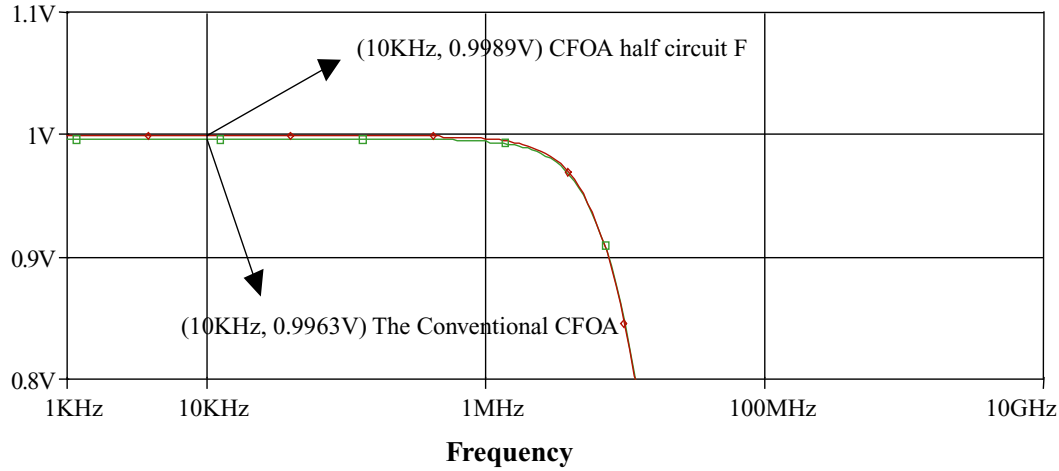


Fig. 40 AC gain accuracy ~ Frequency

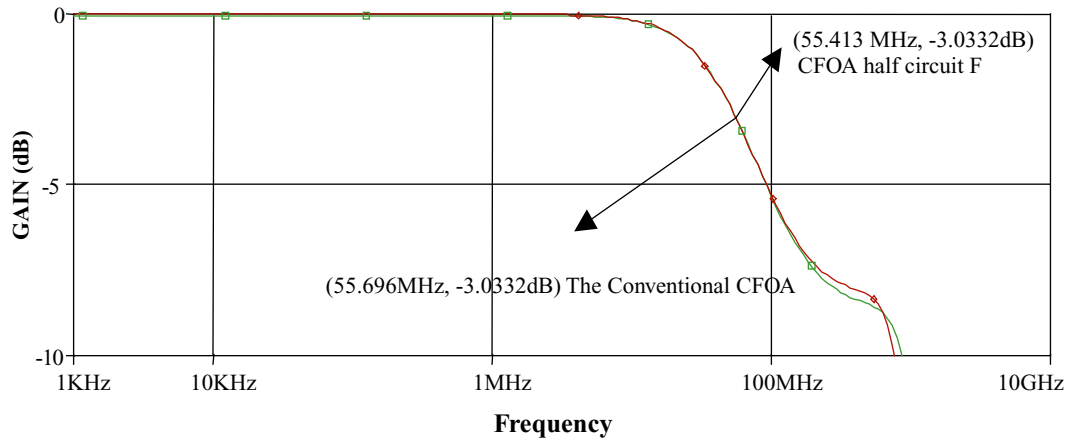


Fig. 41 Frequency responses for unity closed-loop gain

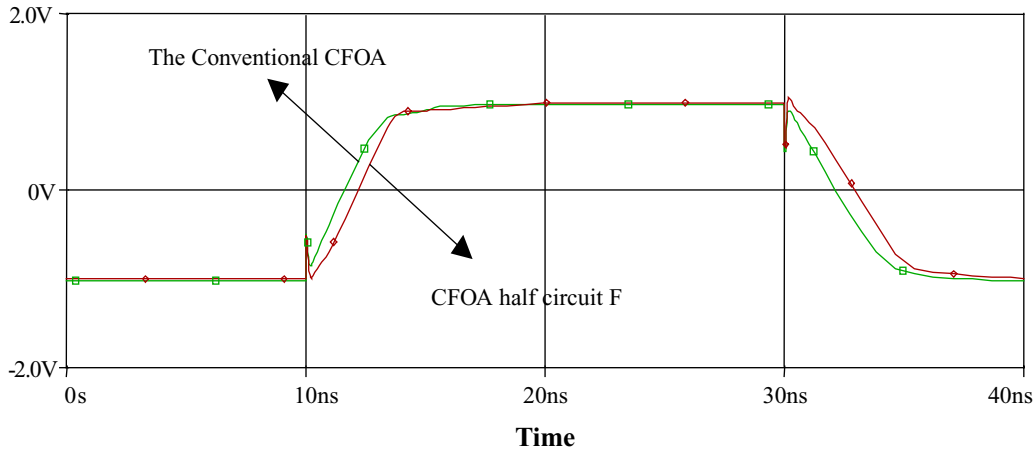


Fig. 42 Transient response

Table 5 Characteristics of the conventional and the improved CFOA using half-circuit F

Parameter	Conventional CFOA [15]	CFOA using half circuit *F* (Fig. 38)
CMRR	51.4 dB	90.2 dB
Bandwidth	55.7 MHz	55.4 MHz
Inverting input resistance (at 0 V d.c. input)	68.7 Ω	72.4 Ω
Non-inverting buffer input resistance (at 0 V d.c. input)	2.3 MΩ	1.9 MΩ
AC gain error (Unity gain, Vin = 1 V pp)	3.7 mV	1.1 mV
Input offset voltage (at 0 V d.c. input)	±20.6 mV	±2.95 mV
Slew rates	SR+ = 569.6 V/μs	SR+ = 564.8 V/μs
	SR− = 454.2 V/μs	SR− = 430.5 V/μs
Input dynamic range	−3, +3 V	−2.4, +2.3 V

Discussion:

Compared with half-circuit E, all that has improved is the slew rate which is attributed to the use of emitter-follower drive for the bases of Q_3, Q_4.

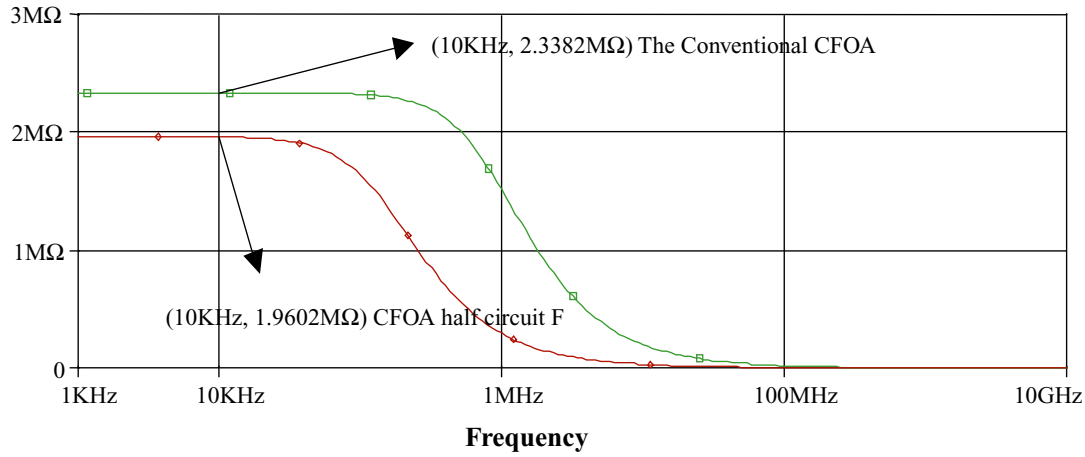


Fig. 43 Input impedance ~ frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

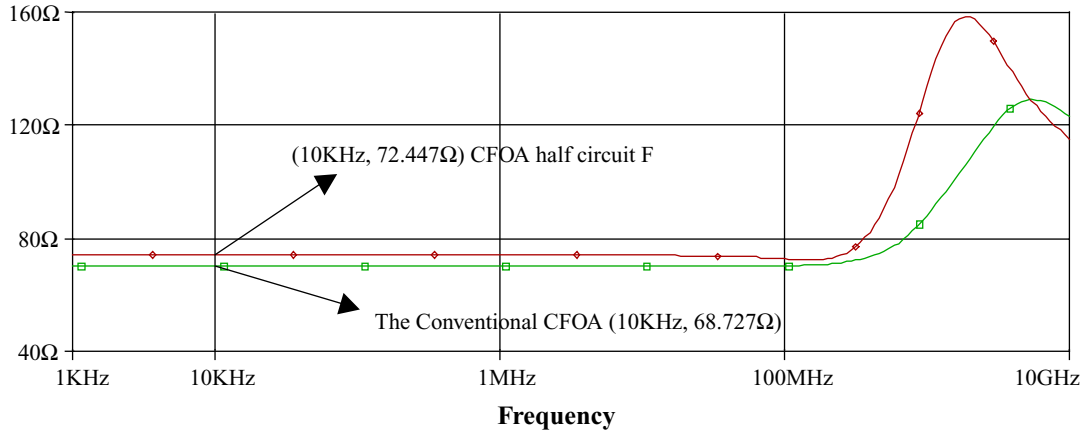


Fig. 44 Input impedance (inverting) ~ Frequency

The dotted contour, b, encloses a current-transfer cell (shown earlier, in Fig. 9) which is replicated three times, in NPN form, in the input stage. A similar PNP cell is also replicated three times in the design. The output stage of the CFOA is conventional. The mirror-symmetry of the input stage about an imaginary horizontal line joining the 'non-inverting', and 'inverting' inputs helps promote a low offset-voltage.

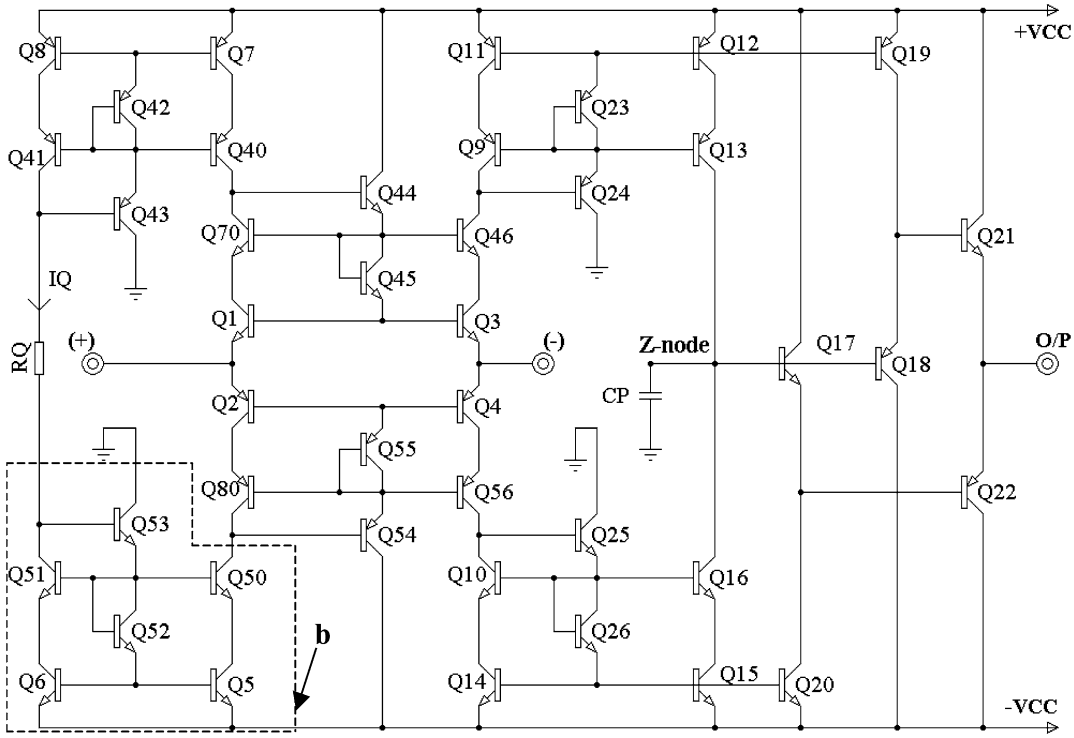


Fig. 45 A CFOA using half-circuit G

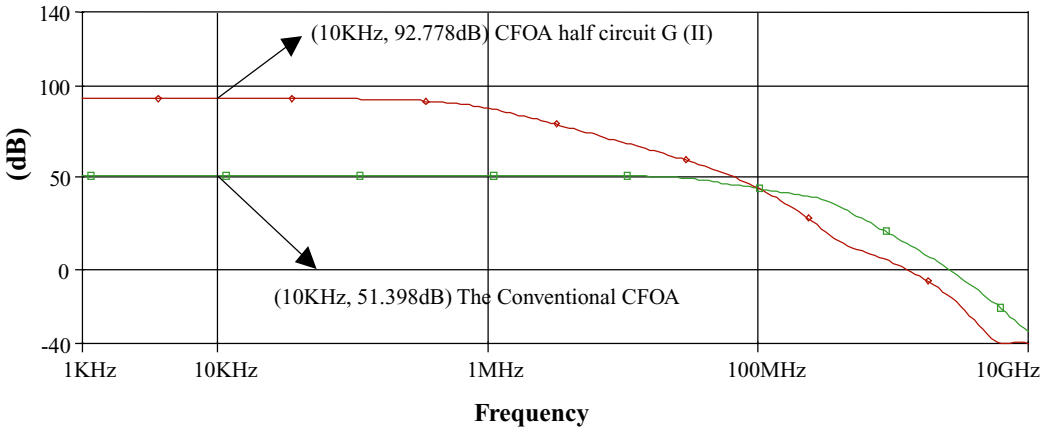
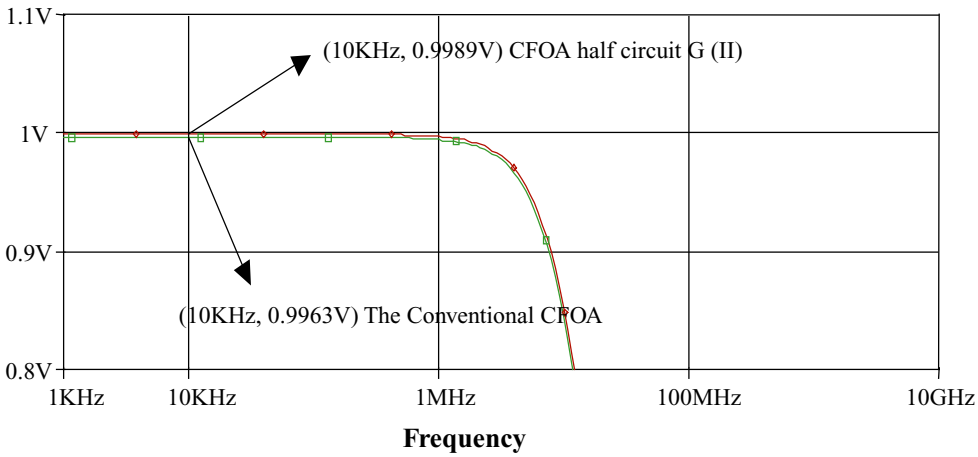


Fig. 46 CMRR ~ Frequency

Fig. 47 AC gain accuracy ~ Frequency



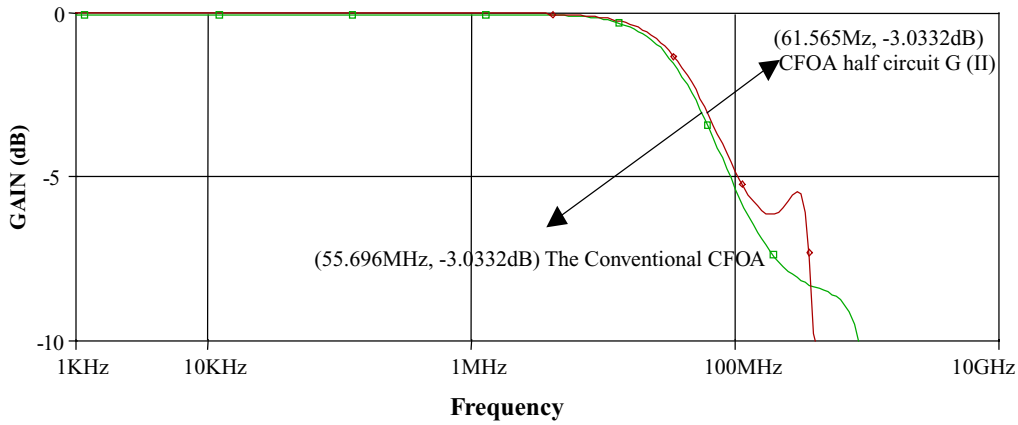


Fig. 48 Frequency responses for unity closed-loop gain

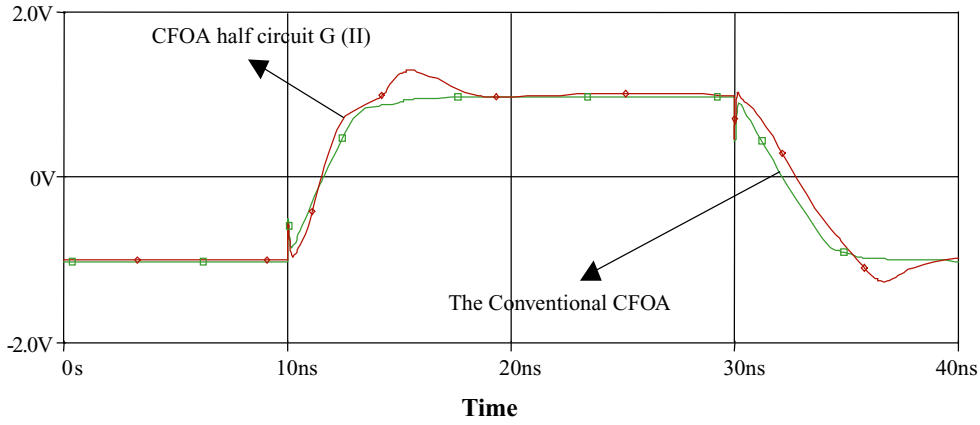


Fig. 49 Transient response

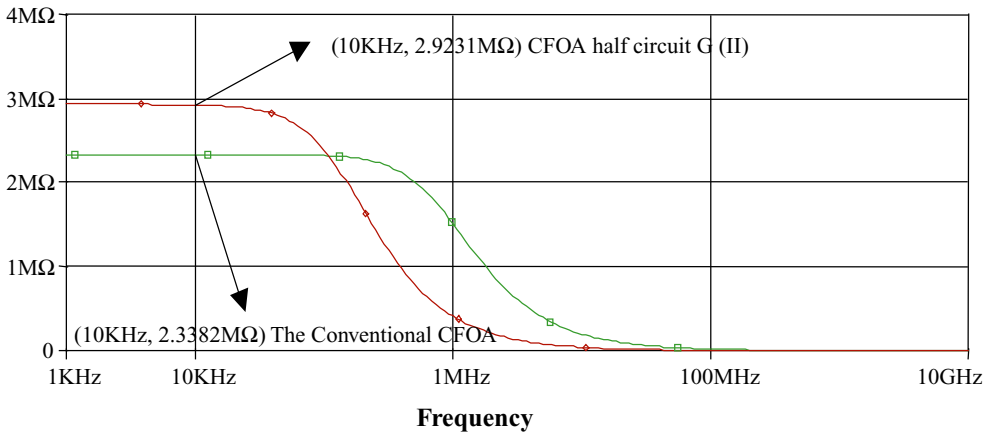


Fig. 50 Input impedance ∼ frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

6 Conclusions

This paper has presented some analysis and discussion that provides insight into a methodology for the design of input stages for high performance CFOAs. For the maximum output voltage swing the input stage of a well-established CFOA is the best option. For comparable slew-rate, but improved CMRR and reduced offset voltage, other choices are possible.

A number of new CFOAs with performances much better than that of the conventional CFOA have been introduced in this paper. A comparison of performance parameters

Table 6 Characteristics of the conventional and the improved CFOA using half-circuit G

Parameter	Conventional CFOA [15]	CFOA using half circuit G (Fig. 45) [21]
CMRR	51.4 dB	92.8 dB
Bandwidth	55.7 MHz	61.6 MHz
Inverting input resistance (at 0 V d.c. input)	68.7 Ω	62.9 Ω
Non-inverting buffer input resistance (at 0 V d.c. input)	2.3 MΩ	2.9 MΩ
AC gain error (Unity gain, Vin = 1 V pp)	3.7 mV	1.1 mV
Input offset voltage (at 0 V d.c. input)	±20.6 mV	±0.75 mV
Slew rates	SR+ = 569.6 V/μs	SR+ = 950.6 V/μs
	SR− = 454.2 V/μs	SR− = 459.4 V/μs
Input dynamic range	−3 V, +3 V	−2 V, +2 V

Discussion:

In the current-transfer cell, Q_5 and Q_6 both operate at the same V_{CB} (≈ 0), as well as the same collector current, and since the cell is repeated throughout the architecture of the CFOA it ensures a very low Vos.

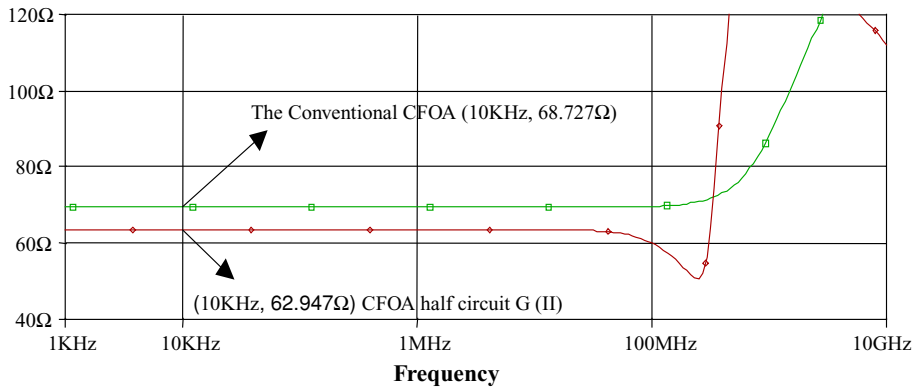


Fig. 51 Input impedance (inverting) ∼ Frequency

is summarised in Table 7. However, the price paid for these improvements is a reduced output voltage swing, because of vertical transistor stacking, for given rail supply voltages.

Table 7 Comparison of CFOA performance parameters

Parameter*	Best	→	→	→	→	Worst
CMRR	C	D	G	F	E	B
SR+	G	D	F	B	C	E
SR−	G	F	E	D	C	B
V_{OS}	G	F	E	D	C	B
$R_{IN(-)}$	G	D	F	C	E	B
$R_{IN(+)}$	B	C	D	G	F	E
BW	G	D	C	F	E	B
A.C Gain Error	G	E	F	B	D	C
Dynamic Input Range	B	C	E	F	D	G
Dissipation	E	F	B	C	D	G
Transistor Count	B 38	C 38	D 40	E 34	F 34	G 42

*A letter stands for half-circuit type.

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He is the author of over 60 publication and two undergraduate textbooks, 'Digital signal transmission: line circuit technology' (1987) and 'Introduction to Analogue Electronics' (1997).
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