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# Implementation of a chaotic oscillator by designing Chua's diode with CMOS CFOAs

**E. Tlelo-Cuautle · A. Gaona-Hernández · J. García-Delgado**

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**Abstract** The implementation of a chaotic oscillator which is based on Chua's circuit, is presented. Chua's diode is realized by using current feedback operational amplifiers (CFOAs). Furthermore, it is shown that a CMOS compatible CFOA can be designed by connecting two voltage followers sandwiched between two current mirrors. The proposed implementation is biased at $\pm 1.2$ V, and simulated by using SPICE and standard CMOS technology of 0.35 $\mu$m. Finally, simulation results are presented to show the sequence of chaotic behaviours for increasing values of the linear resistance.

**Keywords** Analog CAD · Chua's circuit · CFOA · CCII+ · Voltage follower · Current mirror · MOSFET

## Introduction

Chaos phenomenon has been studied extensively from three decades ago, in various areas of science such as biology, ecology, physics, optics, etc. [1]. In electronics, a very interesting and simplest autonomous third-order circuit which exhibits bifurcation and chaotic phenomena can be implemented as shown by Fig. 1, where the most important element is a nonlinear resistor called Chua's diode ($N_R$).

Chua's circuit is the only chaotic system which can be easily built, simulated, and tractable mathematically, such that its simplicity and robustness has made it the *circuit of choice* for generating chaotic signals for practical applications, namely: visual sensing, neural networks, nonlinear waves, music and secure communications [2].

As shown in [1], $N_R$ can be described by a piecewise-linear *I-V* characteristic consisting of two slopes whose limits are determined by two voltage-ranges to establish the breaking points to generate chaotic phenomenon [3–6]. On the other hand, $N_R$ has been implemented by using opamps [3], a CMOS IC design by using operational transconductance amplifiers (OTAs) was presented in [1], and a realization by using commercially available current feedback operational amplifiers (CFOAs) was given in [4, 5]. The last realization is better than the others because the performance of a CFOA does not depend on the gain-bandwidth tradeoff [7, 8]. Furthermore, this device can be implemented in standard CMOS IC technology by using voltage followers (VFs) [9, 10], and current mirrors (CMs). Most important is that VFs and CMs have the advantage of wider bandwidth compared to other more complex analog building blocks, so that VFs, CMs and also current followers (CFs), are good candidates to implement novel analog signal processing applications [11]. For instance, by superimposing or by connecting VFs with CFs and CMs, one gets directly the design of current conveyors [10], which are also quite useful to implement chaotic applications [12].

In this manner, a design-approach is introduced in this paper for a CMOS compatible CFOA circuit consisting of two VFs sandwiched between two CMs. Second, $N_R$ is implemented by using two CMOS CFOAs. Finally, simulation results by using SPICE and standard CMOS technology of 0.35 $\mu$m, are given to show the suitability to implement a chaotic oscillator, i.e. Chua's circuit.

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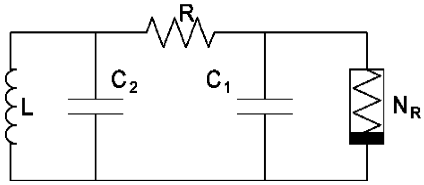


**Fig. 1** Chua's circuit

## Design of the CFOA

As already shown in [9, 10], by using the nullator property, and by manipulating nullators, norators and biases, all CMOS VF topologies can be generated, from which the best practical one can be further selected to accomplish a desired design-application. Henceforth, among all the possible CMOS VF implementations, the one shown by Fig. 2 can be used to design both current conveyors and the CFOA.

In Fig. 2, all biases $I$ can be synthesized by any kind of CM, so that several VF topologies can be generated. From this VF topology, the design of a positive second generation current conveyor (CCII+) can be obtained by synthesizing the biases I located at its output-port by simple cascode CMs, and by synthesizing the biases I located at its input-port by simple CMs. The CCII+ is embedded in Fig. 3, where labels $Y$ and $X$ are associated to the input and output ports of the $VF$, while $X$ and $Z$ are associated to the input and output ports of the CM. Afterwards, by connecting this CCII+ with a VF one gets the design of the CMOS CFOA given in Fig. 3. The VF between Z and W is taken from Fig. 2, where the biases I located in the output port has been eliminated, as described in [9].

As one can infer, at the behavioral level of abstraction the design-approach for the CFOA can be described by a circuit consisting of two VFs sandwiched between two CMs. Furthermore, at the transistor level of abstraction many CMOS CFOA realizations may arise by choosing other kinds of VF and CM topologies. Henceforth, the CMOS CFOA shown in Fig. 3 is used herein to design $N_R$. The sizing of this active device has been done by using standard CMOS technology of 0.35 $\mu$m, supplies of $\pm 1.2$ V, and $I_{ref} = 20$ $\mu$A. From [13], by setting $L = 1$ $\mu$m, the sizes of all $P$-channel MOSFETs are $W = 92$ $\mu$m, and all $N$-channel MOSFETs are $W = 85$ $\mu$m.

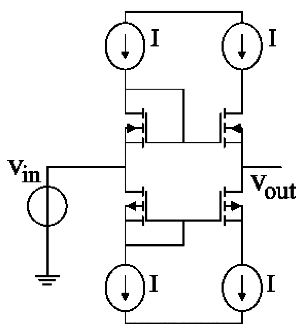


**Fig. 2** CMOS VF with ideal current biases

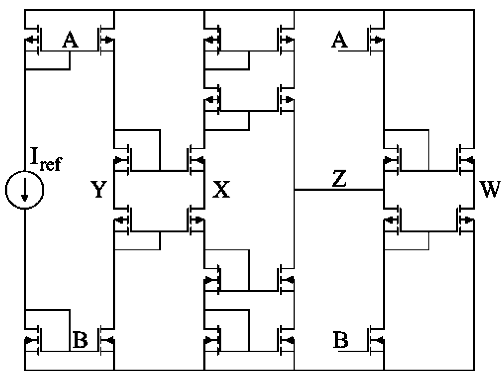


**Fig. 3** The CFOA consisting of two VFs sandwiched between two CMs

## Design of Chua's diode

By using the CMOS CFOA shown in Fig. 3, $N_R$ can be implemented as shown by Fig. 4. The simulation result by using SPICE is shown by Fig. 5, where it can be appreciated the piecewise-linear $I$-$V$ characteristic. The breaking points are located at $\pm 114$ mV, while the negative nonlinear behavior is performed between $\pm 400$ mV.

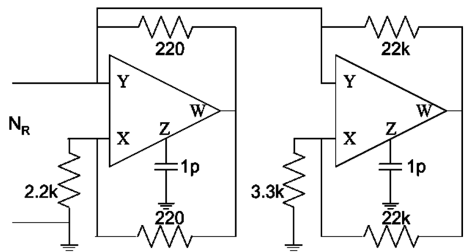


**Fig. 4** Design of $N_R$ by using the CFOA shown in Fig. 3

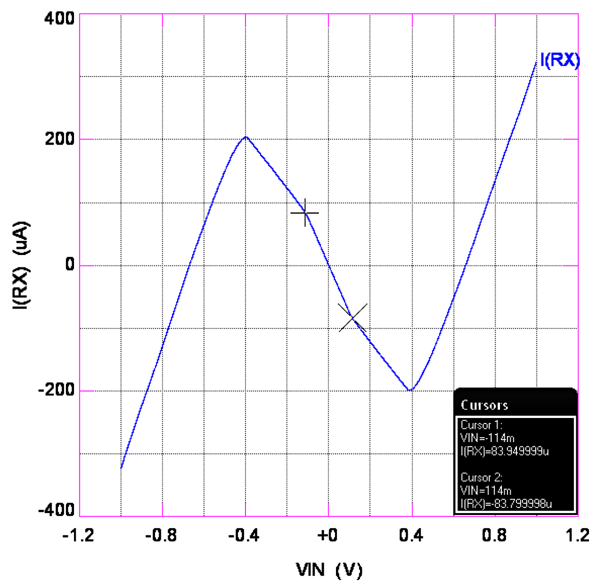


**Fig. 5** Simulation of the $I$-$V$ characteristic of $N_R$

**Simulation of the chaotic oscillator**

The $N_R$ shown in Fig. 4 can be used to implement the chaotic oscillator shown in Fig. 1. So that by setting $L = 1$ mH, $C_1 = 450$ pF, $C_2 = 1.5$ nF, by giving the initial conditions to the capacitors as $V_{C1} = 0.1$ V and $V_{C2} = 0$ V, and by selecting $V_{C1}$ and $V_{C2}$ as state variables to obtain $V_{C2}$ versus $V_{C1}$, a bifurcation sequence can be obtained by varying the value of the linear resistor $R$. For instance, a behavior presented near the large limit cycle is generated with $R = 1540$, as shown by Fig. 6, where $V(6)$ is associated to $V_{C2}$ and $V(1)$ to $V_{C1}$. It can be noted that the double scroll behavior is embedded in this Figure. By increasing $R$ to 1650, the double scroll attractor is generated as shown in Fig. 7. If $R = 1693$, a kind of Rössler-type attractor, or a local attractor is generated as shown by Fig. 8. When the value of R is above 1710, the $n$-period attractor is generated, but just when $R = 1746$, the 1 window 1-period attractor is generated, as shown by Fig. 9. Furthermore, by simulating the response in a state variable, a periodic signal can be appreciated as shown by Fig. 10, where the frequency is around 84 kHz. As a result, one can conclude on the suitability to use CMOS CFOAs to implement Chua's circuit. In the same manner, an analog designer can explore on other CFOA realizations by choosing other kinds of

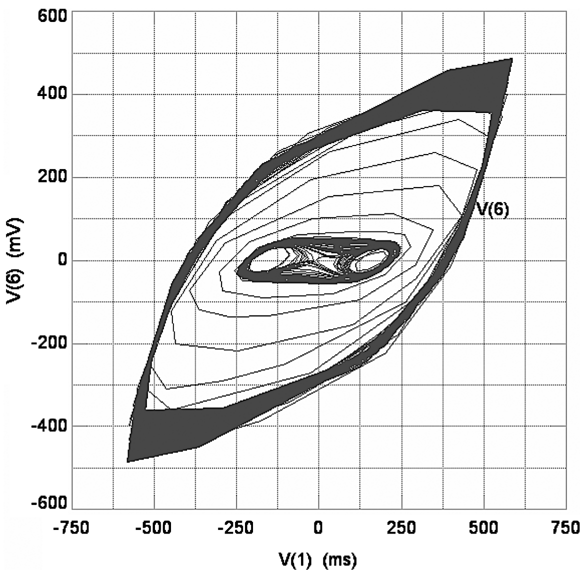


**Fig. 6** Behavior near the large limit cycle with $R = 1540$

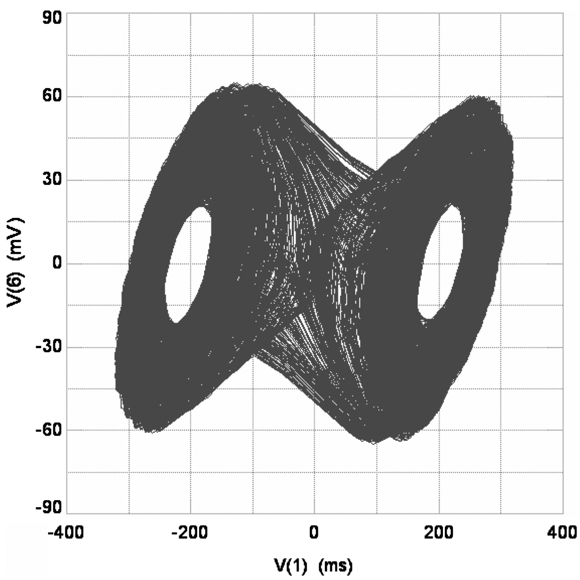


**Fig. 7** Generation of the double scroll attractor with $R = 1650$

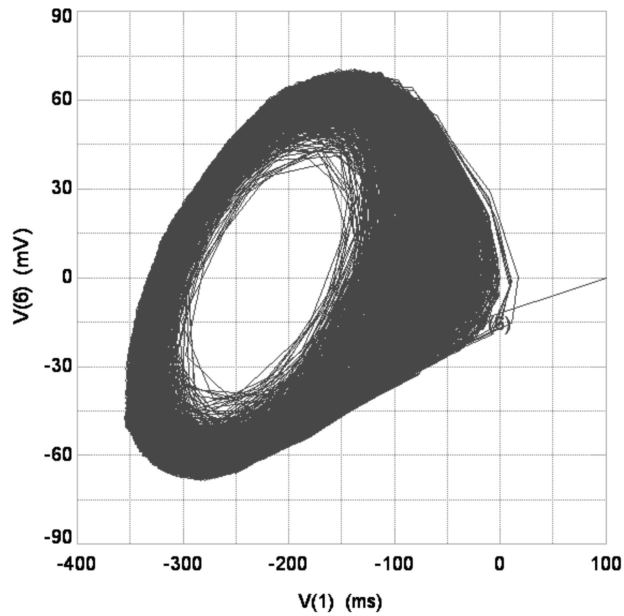


**Fig. 8** Generation of a local attractor with $R = 1693$

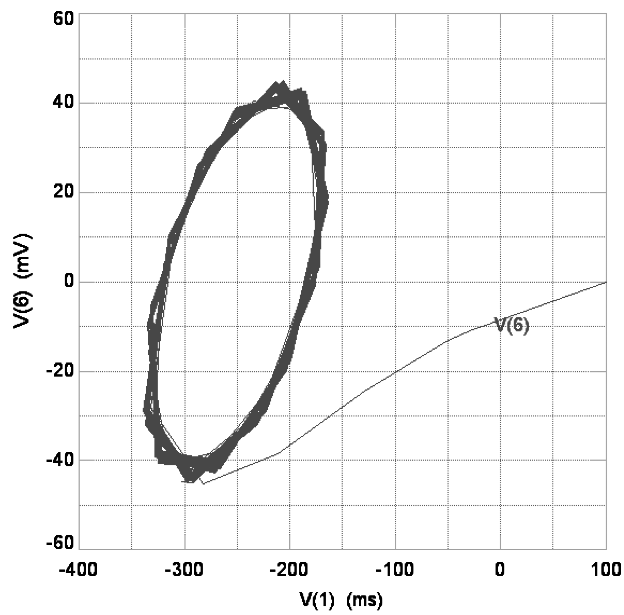


**Fig. 9** Generation of a 1-period attractor with $R = 1746$

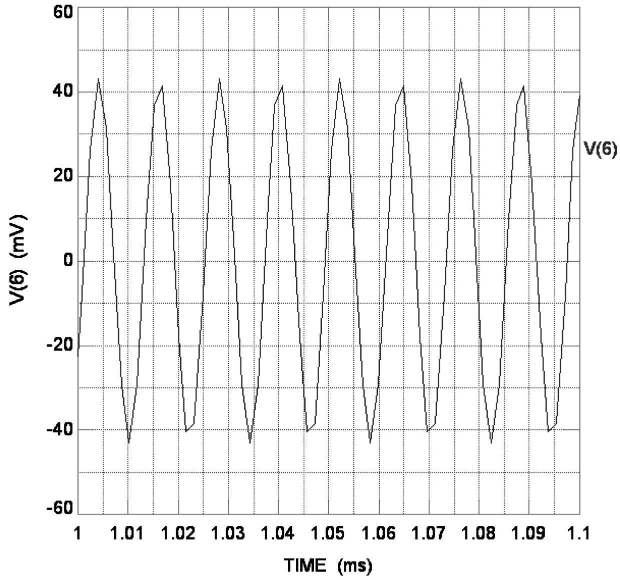


**Fig. 10** Periodic signal in $C_2$ when the 1-period attractor is generated

VFs and CMs to connect two VFs sandwiched between two CMs.

## Conclusion

It has been shown that at the behavioural level of abstraction, the design of a CMOS CFOA can be generated by a circuit consisting of two VFs sandwiched by two CMs. In this manner, at the transistor level of abstraction, an analog designer can explore on all CMOS compatible CFOA circuit realizations by choosing other kinds of VF and CM topologies. For instance, it was shown that the proposed CFOA design is suitable to implement $N_R$.

By using SPICE and standard CMOS technology of 0.35 $\mu$m, the proposed design for $N_R$ generates the piecewise-linear *I-V* characteristic, which is required to implement Chua's circuit. In this manner, from SPICE simulations results one can conclude on the suitability of the proposed design to generate bifurcation and chaotic behaviours by increasing the value of the linear resistance.

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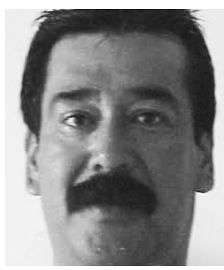

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