Analog Integrated Circuits and Signal Processing, 45, 61–69, 2005 c 2005 Springer Science + Business Media, Inc. Manufactured in The Netherlands.

Current-Division-Based Digital Frequency Tuning for Active RC Filters

KONG-PANG PUN,¹ CHIU-SING CHOY,¹ CHEONG-FAT CHAN¹ AND JOSE´ EPIFANIO DA FRANCA ˆ ²

1Department of Electronic Engineering, Chinese University of Hong Kong, Shatin, Hong Kong 2Chipidea Microelectronics S.A., TagusPark—Edificio Innovacao IV, Sala 733, 2780 920, Porto Salvo, Portugal ˜ E-mail: kppun@ee.cuhk.edu.hk

Received August 14, 2003; Revised July 2, 2004; Accepted August 30, 2004

Abstract. This manuscript presents a novel digital frequency tuning technique for integrated active RC filters. Unlike the traditional tuning approach of varying the values of the capacitors or resistors, the proposed technique achieves the tuning by varying the currents that flow through the resistors or capacitors. In this manuscript, the current varying is achieved by using a digital-controlled MOSFET-only current division network. This new tuning technique features digital tuning, compact size, and wide tuning range as well as high linearity as demonstrated by transistor-level circuit simulations.

Key Words: digital frequency tuning, active RC filter, current division

1. Introduction

The active RC filter provides highest linearity performance compared with other types of integrated continuous-time filters, such as MOSFET-C and *gm*-C filters. A basic property of active RC filters is that frequency tuning is required because their filter coefficients are determined by the product of resistor and capacitor values, which can vary as much as $\pm 50\%$ in integrated circuits. The traditional tuning technique for active RC filters is to use programmable capacitor (or resistor) arrays [1–4]. Figure 1 shows a first order lowpass active RC filter employing this tuning technique.

An alternative tuning approach is to control the current i_x that flows from the resistors (Fig. 1), such that only a portion, say, $\alpha(0 < \alpha \leq 1)$, of i_x is diverted to the integrating capacitor *C*. The effect of this *current division* is equivalent to the scaling of the capacitor *C* by $\frac{1}{\alpha}$. Therefore, tuning of the filter coefficients can be accomplished. This concept was first applied in *R-MOSFET-C filter* [5], where the above mentioned current division is performed by a MOSFET differential pair. In R-MOSFET-C filter, tuning is controlled by the analog gate voltage across the MOSFET differential pair.

In this manuscript, we propose to use a digitally programmable current division network (CDN) [6, 7] to implement the above mentioned concept of current division and thus the frequency tuning of the active RC filter. For automatic tuning, the method proposed in [3] can be used.

Compared with the tuning approach in the R-MOSFET-C filter, the proposed tuning method features digital tuning. In this method, tuning is controlled by a digital code, which can be stored in memory. Therefore, the tuning process needs to be done only during the power-up mode. Once the control code is obtained, the tuning circuit can be turned off to save power. Another advantage of the digital tuning is the higher immunity of the tuning circuit to noises.

Compared with the traditional tuning approach of using programmable capacitor/resistor arrays, the proposed technique has the advantages of compact size and wide tuning range. The latter property makes it suitable in the baseband channel selection application in multi-mode wireless receivers [8]. Meanwhile, the proposed technique also retains the high linearity performance of the active-RC filter. Furthermore, with a properly designed CDN the proposed technique can be used to reduce the chip area of filters with low characteristic frequency, where large RC values are required otherwise.

The remaining parts of this manuscript is arranged as follows. Section 2 presents the principle of the

Fig. 1. First order lowpass active RC filter with a programmable capacitor array.

proposed tuning method, describes the current division circuit, and discusses non-ideal characteristics. Section 3 presents the transistor-level simulation results. Section 4 concludes the manuscript.

2. The Proposed Tuning Technique

We will start introducing the proposed tuning technique by using a first order filter as an example. A general first-order continuous-time filter has the s-domain transfer function $H(s)$ in the following form:

$$
H(s) = \frac{k_1 s + k_0}{s + \omega_0}.
$$
 (1)

It can be of lowpass, highpass or allpass type depending on the coefficients. Figure 2 shows a signal flow graph (SFG) of this transfer function.

The active RC circuit of the general first order filter employing the proposed tuning technique is depicted in Fig. 3(a). A CDN is added in the circuit. It is connected to all the resistors in one end, and to the virtual ground of the op-amp in the other end. The CDN is used to control the currents that flow from the resistors R_1 and R_2 to the integrating capacitor C_A . The CDN is digitally programmable. The relation between its output current (right hand side) and input current is described by the

Fig. 2. Signal flow graph of a general first order filter.

following expression:

$$
I_{\text{out}} = \alpha I_{\text{in}}, \quad \alpha = \sum_{i=1}^{n} b_i 2^{-i} \tag{2}
$$

where b_i is the *i*th digital bit and *n* is the length of the control word.

Suppose the input resistance of the CDN is zero for the moment. Under this assumption, the voltage drop across the CDN is zero and node *x* of Fig. 3(a) behaves like a virtual ground. We can thus obtain an SFG of the circuit as shown in Fig. 3(b). The internal signal of the SFG represents the current i_c that flows to the capacitor *CA*. By equating the SFGs of Figs. 3(b) and 2, we obtain the correspondence between the filter coefficients and component values as follows:

$$
k_0 = \frac{\alpha}{R_1 C_A}
$$
, $k_1 = \frac{C_1}{C_A}$, and $\omega_0 = \frac{\alpha}{R_2 C_A}$. (3)

From the above expressions, we observe that the characteristic frequency ω_0 of the filter depends on the value of α . On the other hand, the passband gain (which equals k_1 in the highpass case and k_0/ω_0 in the lowpass case) does not depend on the value of α . Therefore, frequency tuning can be achieved without affecting the passband gain by varying the value of α .

Since the maximum value of α is 1, ω_0 can only be tuned downward. Under the process variation, the minimum full-scale value of ω_0 must not be less than the desired value of ω_0 . For example, if the process has a $\pm 50\%$ variation and the desired value of ω_0 is 2 MHz, then the nominal full-scale value of ω_0 must be at least 4 MHz. In other words, the RC values are designed according to $\omega_0 = 4$ MHz. In contrast, in the traditional tuning approach, the full-scale values of the capacitor arrays must be designed according to the lower bound of ω_0 , i.e., 1 MHz \times (1–50%) = 1 MHz in this example. A higher value of ω_0 results in a smaller area. Therefore, filters employing the proposed technique will be more compact than those employing traditional tuning technique. (Also, the CDN is very compact as it will be explained in Section 2.1).

Besides the frequency tuning, the proposed technique has another application. For an RC filter that has low characteristic frequency, large chip area is normally required due to the large values of RC products. The chip area can be reduced by the following approach. First, the filter is designed with a higher characteristic frequency to obtain smaller values of R and C. Then by using a CDN with a fixed (if tuning is not necessary)

Fig. 3. (a) Active RC circuit of the general first order filter with the proposed tuning technique. (b) Equivalent signal flow graph.

small value of α , the characteristic frequency can be lowered to the desired range.

2.1. CDN Circuit and the Loading Effect

The most important circuit component for realizing the proposed tuning concept is the current division network. In this manuscript, we have chosen the one proposed by Bull and Geelen [6] as depicted in Fig. 4. It is an R-2R like MOSFET-only ladder. All the transistors in the circuit are identical. The current flowing from the input side of the CDN is divided into two equal parts at each node of $1, 2, \ldots, n$. The accuracy of the current division depends only on the matching of transistors and can be very accurate. As indicated in the figure,

the binary-weighted currents in the vertical branches are diverted either to the ground or to the output (connected to virtual ground here) depending on a digital bit of the control word.

Since the number of transistors required by the CDN increases linearly with the size of the digital control word, the CDN is very compact even for a long control word.

The CDN has a characteristic resistance R_c looking from the input. The value of R_c is proportional to (L/W) ratio of the transistors, and is typically in the order of hundred Ohms or Kilo-ohms. At DC, all the capacitors behave as open-circuits. Current flowing through the CDN is zero. The node x (Fig. 3(a)) performs as a virtual ground. The filter's behaviour is not different from the one without CDN. At other

Fig. 4. (a) Symbol and (b) circuit of the current division network.

64 *Pun et al.*

Fig. 5. Loading effect.

frequencies the CDN will experience a voltage drop. Node *x* will no longer be at virtual ground, and thus the magnitudes of currents flowing from resistors to the CDN will be affected. This effect is referred to as *loading effect* [5].

Figure 5 illustrates the loading effect of a CDN connected to two resistors. Consider the input signal v_1 first. Due to the non-zero resistance of the CDN, the current signal i_x flowing to the CDN does not equal to $\frac{v_1}{R_1}$. Actually, it can be shown that

$$
i_x = \frac{v_1}{\beta R_1},\tag{4}
$$

where

$$
\beta = 1 + \frac{R_c}{R_1 // R_2}.\tag{5}
$$

The β is called as the *loading effect factor* in this manuscript. The value of β is the same for the other input branch. For *n* ($n > 2$) resistors, $\beta = (1 +$ $\frac{R_c}{R_1/|R_2|/.../|R_n}$. If $R_c \ll R_i$ for all *i*, then $\beta \approx 1$, which means the loading effect can be ignored.

Due to the loading effect, the SFG of Fig. 3(b) must be modified accordingly. From the above analysis, *R*¹ and R_2 in Fig. 3(b) should be replaced with βR_1 and βR_2 respectively. Therefore, the correspondence between the filter coefficients and component values must be modified as follows,

$$
k_0 = \frac{\alpha}{\beta R_1 C_A}
$$
, $k_1 = \frac{C_1}{C_A}$, and $\omega_0 = \frac{\alpha}{\beta R_2 C_A}$. (6)

To determine the component values based on (6) and (5) involves solving nonlinear equations. Instead, we can design the filter starting from (3), i.e., without considering the loading effect. Denote the values of *Ri*

obtained from (3) as R'_i , where $i = 1, 2$. From (3) and (6), we have

$$
\beta R_i = R'_i, \quad i = 1, 2. \tag{7}
$$

Substituting (7) into (5) and solving β in terms of R'_i , we obtain

$$
\beta = \left(1 - \frac{R_c}{R_1'/R_2'}\right)^{-1}.
$$
 (8)

In other words, to compensate the loading effect, the resistors must be scaled as follows,

$$
R_i = \left(1 - \frac{R_c}{R_1'//R_2'}\right) R_i', \quad i = 1, 2. \tag{9}
$$

The nonlinear I–V characteristics of the transistors of the CDN may affect the nonlinearity of the whole filter. However, the effect is insignificant due to the small voltage drop across the CDN, which results in small v_{DS} for all transistors in the CDN. Small v_{DS} leads to low distortion.

2.2. Second and Higher Order Filters

A filter of higher than two-order can be implemented by cascading first order and second order filter sections. A general continuous-time second order filter, or biquad, has the transfer function of the following form:

$$
H(s) = \frac{k_2 s^2 + k_1 s + k_0}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}.
$$
 (10)

It can be of lowpass, highpass, bandpass or allpass type depending on the coefficients. An SFG of the biquad is shown in Fig. 6.

Fig. 6. Signal flow graph of a general second order filter.

Fig. 7. (a) Proposed general second order filter. For simplicity, single-ended circuit is shown. The negative resistance −R₃ can be implemented in differential circuit. (b) Equivalent signal flow graph.

Figure 7 shows the active RC biquad circuit employing the proposed tuning technique and the equivalent SFG. Note that the loading effect has been included in the SFG. The loading effect factors β_A and β_B of the first and second CDN respectively are:

$$
\beta_A = 1 + \frac{R_c}{R_1 // R_4};\tag{11}
$$

$$
\beta_B = 1 + \frac{R_c}{R_2 / / R_3 / / R_5},\tag{12}
$$

where R_c is the characteristic resistance of the CDNs. β_A and β_B tends to one for $R_c \ll R_i$, $i = 1, 2, ..., 5$. By equating the SFGs of Figs. 6 and 7(b), we obtain the correspondence between the filter coefficients and component values as follows:

$$
k_2 = \frac{C_1}{C_B}, \ \ k_1 = \frac{\alpha}{\beta_B R_2 C_B}, \ \ k_0 = \frac{\alpha^2}{\beta_A \beta_B R_1 R_3 C_A C_B},
$$
\n(13)

$$
\omega_0 = \alpha \sqrt{\frac{1}{\beta_A \beta_B R_3 R_4 C_A C_B}}, \text{ and}
$$

$$
Q = \sqrt{\frac{\beta_B R_5^2}{\beta_A R_3 R_4} \frac{C_B}{C_A}}.
$$
 (14)

From the above expressions, it can be observed that the characteristic frequency ω_0 of the biquad is controlled by the digital code α . On the other hand, the Q factor of the biquad does not depend on α , but on the ratios of resistors and capacitors which can be sufficiently accurate. Thus *Q*-factor tuning is not and need not to be tuned. Moreover, the value of α does not affect the pass-band gain of the filer. For, example, if the biquad is configured as a lowpass filter, its DC gain k_0/ω_0^2 is independent of α .

To determine the values of *R* and *C*, we can first assume $\beta_A = \beta_B = 1$ (no loading effect). From expressions in (13) and (14), we can obtain a set of parameters *R* and *C*. Denote the values of *Ri* obtained under this assumption as R'_i , $i = 1, 2, ..., 5$. By the method presented in Section 2.1, we can obtain the values of *Ri*

66 *Pun et al.*

when the loading effect is considered:

$$
R_i = \begin{cases} \beta_A R'_i, & \text{for } i = 1, 4, \\ \beta_B R'_i, & \text{for } i = 2, 3, 5. \end{cases}
$$
 (15)

The loading effect factors β_A and β_B can be expressed in terms of R'_i as follows:

$$
\beta_A = \left(1 - \frac{R_c}{R_1'//R_4'}\right)^{-1};
$$
\n(16)

$$
\beta_B = \left(1 - \frac{R_c}{R_2'//R_3'//R_5'}\right)^{-1}.\tag{17}
$$

Last, since the non-linear distortion contributed by each CDN is related to the effective gate-source voltage of its transistors, it can be kept the same for all CDN by adopting a constant-current density approach, i.e., by sizing the W/L of the transistors of each CDN to be proportional to the input current of the CDN.

3. Simulation Results

In order to verify the proposed tuning technique, a 4th order Butterworth lowpass filter with a 5-bit CDN has been designed in a 0.35μ CMOS technology. The filter is implemented as a cascade of two biquads of the type shown in Fig. 7, with R_2 and C_1 removed. The targeted −3 dB frequency *f*[−]3 dB of the filter is 2 MHz. As the *f*[−]3 dB can only be tuned downward but not upward with the proposed tuning technique, the nominal value

of *f*−3 dB must be set higher than 2 MHz. To cover the ±50% variation of the *RC* product in the technology that we have used, the nominal value of $f_{-3 \text{ dB}}$ is set to 4 MHz.

The values of the components of the filter (cascade of two biquads) after scaling according to the loading effect are listed in Table 1. For both biquads, the resistance of the CDN connecting to OP1 is approximately $1.2 \text{ k}\Omega$, and the resistance of the CDN connecting to OP2 is approximately 2.3 k Ω .

Transistor-level circuit simulations have been conducted. The fully differential op-amps used in the design have 60 dB DC gain and 100 MHz gain-bandwidth product. For the CDNs, the minimum transistor length is used, and the transistor widths are ranged from 2 to 4μ (sized according to their current densities).

Figure 8 shows the simulated amplitude response of the filter at every control code. A wide tuning range of

Fig. 8. Simulated amplitude response of the 4th order filter with 5-bit CDN at every control code. The control code of each curve is indicated on the top of the graph.

Fig. 9. (a) $f_{-3 dB}$ versus the control code, (b) Tuning accuracy.

f[−]3 dB from 125 KHz to 4 MHz with a step size of 125 kHz is obtained. Figure 9(a) shows the $f_{-3 \text{ dB}}$ of the filter versus the control code. It can be observed that a monotonic tuning (which is very important if an automatic tuning algorithm is applied) is achieved. Ideally, the difference between the *f*[−]3 dB of two consecutive control codes is 125 kHz. To show the tuning accuracy,

we define

$$
Err(i)
$$

= $[f_{-3dB}(i) - f_{-3dB}(i - 1) - 1.25 \text{ kHz}]$

$$
/f_{-3dB}(i) \times 100, \text{ for } i = 1, 2, ..., 2^{n} - 1,
$$

(18)

Fig. 10. Simulated output spectrum for a two-tone test.

where $f_{-3 \text{ dB}}(i)$ is the −3 dB frequency of the filter at control code *i* (in decimal), and *n* is the number of bits of the control word. Figure 9(b) displays the above defined tuning error. From the figure, we find that the tuning error is within $\pm 4\%$ for most control codes (except the first code due to its small base of f _{−3 dB}). This tuning accuracy is comparable to the typical value ranged from ± 2 to $\pm 5\%$ obtainable in the traditional programmable capacitor/resistor array approach [4]. The tuning accuracy here is limited by the gain-bandwidth product of the op-amps, because it results in non-perfect virtual ground, which in turn affects the current division accuracy of the CDNs.

To examine the linearity performance of the proposed circuit, a two tone simulation has been conducted. First, the control code is set to "01111" for a *f*−3 dB near 2 MHz. Then two sinusoidal inputs at 2 and 1.9 MHz with amplitude of $2V_{pp}$ (differential) are applied to the filter. These two frequencies are chosen as they are near the edge of the passband of the filter, where the worst distortion will appear due to the smallest loop gain of the filter's feedback loop. The simulated output spectrum is shown in Fig. 10. The figure shows that the 3rd harmonic at 1.8 MHz is -75.8 dB to the fundamental one, which corresponds to a higher than 12-bit linearity.

4. Conclusions

A novel digital frequency tuning technique based on current division for active RC filter has been presented in this manuscript. The proposed technique features compact area, wide tuning range and easy to design. At the same time, the high linearity of the active-RC filter is maintained when the tuning technique is applied. The feasibility and the above mentioned properties of the proposed technique have been demonstrated by transistor-level circuit simulations.

Acknowledgment

The authors would like to thank the anonymous reviewers for their comments on the paper. This work was supported in part by Hong Kong Research Grant Council under Direct Grant project No. 2050269.

References

- 1. A. Durham, J. Hughes, and W. Redman-White, "Circuit architectures for high linearity monolithic continuous-time filtering." *IEEE Trans. Circuits and Systems*, pp. 651–657, Sept. 1992.
- 2. R. Shariatdoust, K. Nagaraj, J. Khoury, S. Daubert, and D. Fasen, "An integrating servo demodulator for hard disk drives." In *Proc. IEEE Custom Integrated Circuits Conference*, 1993, pp. 10.6.1– 10.6.5.
- 3. H. Khorramabadi, M.J. Tarsia, and N.S. Woo, "Baseband filters for IS-95 CDMA receiver applications featuring digital automatic frequency tuning." In *Digest of Technical Papers, IEEE Int. Solid-State Circuits Conference*, 1996, pp. 172–173.
- 4. J.M. Khoury, "Continuous-time filters." In *The Circuits and Filters Handbook*, W.K. Chen (Ed.), CRC Press and IEEE Press, 1999, pp. 58.1–58.32.
- 5. U.-K. Moon and B.-S. Song, "Design of a low-distortion 22-KHz fifth-order bessel filter." *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1254–1264, 1993.
- 6. K. Bult and G.J.G.M. Geelen, "An inherently linear and compact MOST-only current division technique." *IEEE J. Solid-State Circuits,* vol. 27, no. 12, pp. 1730–1735, 1992.
- 7. C.M. Hammerschmied and Q. Huang, "Design and implementation of an untrimmed MOSFET-Only 10-bit a/d converter with −79 dB THD." *IEEE J. Solid-State Circuits*, vol. 33, no. 8, pp. 1148–1157, 1998.
- 8. H.A. Alzaher, H.O. Elwan, and M. Ismail, "A CMOS highly linear channel-select filter for 3G multistandard integrated wireless receivers." *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 27–37, 2002.

Kong-pang Pun received his B.Eng. and M.Phil. in Electronic Engineering from the Chinese University of Hong Kong in 1995 and 1997 respectively, and Ph.D. in Electrical and Computer Engineering from the Institute Superior Técnico, Technical University of Lisbon, Portugal, in 2001. After his Ph.D. study, he joined the Department of Electronic Engineering, Chinese University of Hong Kong, where he is presently an Assistant Professor. Dr. Pun serves as a reviewer for several international journals. His research interest includes circuits for complex signal processing, continuous-time filters, sigma-delta modulators, and ultra low-voltage circuits.

Chiu-sing Choy received his B.Sc., M.Sc. and Ph.D. from the University of Manchester in 1983, 1984 and 1987 respectively, major in electrical and electronics engineering. From 1985, he spent a year in Ferranti Microelectronics, Oldham, U.K., assisting research in ASIC technology. In 1986, he joined Department of Electronic Engineering, The Chinese University of Hong Kong, where he is presently a Professor.

Dr. Choy is currently interested in low-power highspeed asynchronous designs, smart card technology and applications, digital transceiver for 3rd generation mobile communication, encryption and channel coding core designs.

Cheong F. Chan received his B.T. in electrical engineering with high honors from State University of New York at Binghamton in 1976. He received his M.S. and Ph.D. in electrical engineering from Lehigh University in 1979 and 1984, respectively. From 1985 to 1986, Dr. Chan was a post-doctoral fellow at the Sherman Fairchild Center of Lehigh University, where he developed a 3-micron CMOS self align gate technology. In 1986, he jointed Ametek as a research scientist working on silicon pressure sensors. In 1988, he jointed the VLSI department of AT&T Bell Labs. as a member of technical staff, where he was working on high speed memory design and giga bit network switches. Dr. Chan jointed the faculty at the Chinese University of Hong Kong in early 1993.

José E. da Franca graduated from Instituto Superior Técnico (IST) (Lisboa) in 1978, in 1985 obtained the Ph.D. at Imperial College of Science and Technology (London) and in 1992 obtained the degree of Agregado also from IST.

Dr. Franca is a Full Professor of the Department of Electrical and Computer Engineering of IST, where he was a member of its Executive Council from 1988 to 1991. He has had Visiting Professorship appointments with the University of Aveiro, the University of Macau, and the Chinese University of Hong Kong. In 1987 he founded the Integrated Circuits and System Group and later, in 1994, the IST Centre of Microsystems of which he is a Director. In March 1997 he co-founded and became the President of CHIPIDEA Microelectronics, the first Portuguese engineering company devoted to the design of advanced mixed-signal integrated circuit products.

Dr. Franca is a member of the Editorial Board of the Kluwer Journal on Analog Integrated Circuits and Signal Processing. He has served on the Board of Governors of the IEEE Circuits and Systems Society in the term 1997/99, and on the Executive Council of the European Circuits Society, in the term 1998/2001. Dr. Franca is a Fellow of the IEEE and has been awarded the Golden Jubilee Medal of the Circuits and Systems Society.