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SHORT COMMUNICATION

Fabrication of buried microfluidic channels with observation windows using femtosecond laser photoablation and parylene-C coating

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Abstract
We developed an advanced method for fabricating microfluidic structures comprising channels and inputs/outputs buried within a silicon wafer based on single level lithography. We etched trenches into a silicon substrate, covered these trenches with parylene-C, and selectively opened their bottoms using femtosecond laser photoablation, forming channels and inputs/outputs by isotropic etching of silicon by xenon difluoride vapors. We subsequently sealed the channels with a second parylene-C layer. Unlike in previously published works, this entire process is conducted at ambient temperature to allow for integration with complementary metal oxide semiconductor devices for smart readout electronics. We also demonstrated a method of chip cryo-cleaving with parylene presence that allows for monitoring of the process development. We also created an observation window for in situ visualization inside the opaque silicon substrate by forming a hole in the parylene layer at the silicon backside and with local silicon removal by xenon difluoride vapor etching. We verified the microfluidic chip performance by forming a segmented flow of a fluorescein solution in an oil stream. This proposed technique provides opportunities for forming simple microfluidic systems with buried channels at ambient temperature.

1 Introduction

Microfluidic technologies began to expand rapidly after Manz's group demonstrated a miniaturized chip that performed capillary electrophoresis (Harrison et al. 1992) and, later, a flow-through polymerase chain reaction system (Kopp et al. 1998). Those chips were made using technology based on a double glass substrate. Researchers used fabrication steps known from conventional microelectromechanical systems (MEMS) technology with the addition of deep glass etching with HF/HCl solution (Iliescu et al. 2005) using a Au/Cr mask and glass–glass bonding process (Iliescu et al. 2012). As these processes are rather complicated, there has been a lot of interest in creating microfluidic chips using a Si substrate instead of glass to create channels/chambers and then seal the glass cover with anodic bonding. This reliable bonding technique is known for its use in pressure sensors and other MEMS devices (Petersen 1982). The Si or glass patterning and subsequent bonding are relatively expensive, especially considering the need for a cleanroom facility and equipment. Scientists are, understandably, looking for simpler and cheaper methods to produce microfluidic devices to fulfill the required parameters (Faustino et al. 2016). Plastics such as polydimethylsiloxane (PDMS), acrylic, and polycarbonate have become popular materials for fabricating microfluidic devices. Computer numerical control is used for low-volume production, whereas microinjection molding, imprinting (Martynova et al. 1997), and hot embossing (Velten et al. 2010) are used for large-scale production (Becker and Gartner 2000). PDMS is especially popular as it allows for the rapid prototyping of microfluidic devices without requiring a great investment in cleanroom technology. The drawback of PDMS is its porosity and rather high cost, which prevent this material from being utilized for commercial microfluidic products. Nevertheless, PDMS has been successfully used in microfluidic applications such as

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label-free separation and sorting (Ramchandani and Heptulla 2012), barcoding and sequencing using droplet generation (Liu et al. 2013), particle channel diffusion (Xia et al. 2016), hydrodynamic stretching of single cells (Walsh et al. 2017), the investigation of bacteria physiology (Ilic et al. 2002; Iliescu et al. 2017), and in a quantitative study of antibiotic diffusion through lipid membranes (Huang et al. 2017).

Unfortunately, as with most other techniques making microfluidic devices, creating a channel with a circular cross-section that allows a well-defined liquid flow is rather challenging. There are also electrochemical microfluidic devices currently in large-scale production that are made from plastic and metal layers and utilize laser-based patterning (Ramchandani and Heptulla 2012). Microfluidic channels are also prepared by a femtosecond laser direct-writing method on glass, which requires post-annealing above 1000 °C (Liu et al. 2013). Femtosecond laser direct writing is also used to make non-buried channels in SiC substrates (Huang et al. 2017). Microfluidics with paper substrate (Xia et al. 2016) and virtual microfluidics systems containing fluid walls (Walsh et al. 2017) are also popular.

Silicon substrates for microfluidic devices have their merits, as the planar technology employed for integrated circuits and MEMS production was developed around them. The advantage of silicon as a mechanical material is its well-known technology, enabling vertical or lateral etching with an etch rate of 4–5 μm min^{-1}, and its excellent selectivity to other materials, allowing for the production of complex shapes. Silicon is also resistant to temperatures well in excess of 1000 °C; an insulating layer of SiO_2 can be produced by thermal oxidation of silicon. It also has excellent thermal conductivity and high value of Young's modulus. Silicon oxidation is an important step that covers the channel sidewalls and bottom with SiO_2 and, subsequently, modifies its surface for the chosen purpose. Microfluidic channels are often etched into silicon substrate and capped with anodically bonded glass specifically developed for this purpose to match the silicon thermal expansion coefficient. This technique is well developed but, by default, produces channels with a non-circular cross-section profile. Glass–glass microfluidic systems also do not produce circular channels; moreover, the choice of etching processes for glass is very limited compared with those for silicon.

Is there a way to simplify the Si-based technology, such as using only a single substrate without capping with a second one? A technique called "buried channel technology" (BCT) has been demonstrated (Ilic et al. 2002) using different methods. Researchers etched a trench in a Si substrate using deep reactive ion etching (DRIE) and coated the trench with a suitable material. This material was then selectively removed at the trench bottom using reactive ion etching. The Si at the bottom of the trench was dry etched by SF6 plasma, wet etched electrochemically in HF solution, or chemically etched in HF/HNO3 or KOH solution. The Si substrate can also be etched by XeF_2 vapors. The sidewall passivation was then removed and the trench filled with SiO_2 or Si_3N_4 prepared by a low-pressure chemical vapor deposition (LPCVD) technique. The substrate was subsequently placed into KOH solution, releasing the tubes. Built-in tensile stress in the stoichiometric LPCVD Si_3N_4 layer limits its thickness to ≈ 300 nm, as thicker layers develop cracks. The thin film filling the trenches requires them to be made with a maximum thickness between 0.5 and 0.6 μm; this tiny trench width limits the etched depth. Another option is to use low-stress Si_xN_y, wherein the layer can be significantly thicker [up to a few micrometers (Iliescu et al. 2017)], which relaxes the fabrication process window rule. The BCT technique was further improved (Boer et al. 2000) by replacing the LPCVD layer with parylene (Soon et al. 2010), which makes the entire technique much more robust, as there is no risk in depositing a parylene layer with a thickness of 0.1–50 μm. In addition, parylene is an optically transparent material. Researchers etched trenches in Si substrates and then deposited a layer of parylene. This layer coated the sidewalls and filled the channel to the top, thus sealing it to form a buried tube. The BCT was further improved (Fekete et al. 2012), by making the process compatible with complementary metal oxide semiconductor (CMOS) technology with complex microfluidic structures (Zellner et al. 2009). All these techniques require pinhole-free protection of sidewalls and highly isotropic etching without damaging the edges at the top, which is a rather complicated task.

Silicon itself is a great material for device fabrication, as its technology is well established and the material itself, commonly used with a crystallographic orientation of (100), has high value of Young's modulus at ≈ 179 GPa, making it a mechanically stable material. It also has thermal conductivity of ≈ 130 W m^{-1} K^{-1}, an exceptionally high value for nonmetallic materials, making silicon microfluidics suitable for applications requiring heating, cooling, or forming a temperature gradient. Unfortunately, silicon is not transparent in the visible spectrum. SiO_2, glass, PDMS, and cyclic olefin copolymers are transparent materials commonly used to fabricate microfluidics devices. However, making buried microchannels with round cross-sections, such as those made by BCT, is a complicated if not impossible task with these materials.

Here, we show a single level lithography BCT based on a combination of DRIE of Si, trench conformal coating with optically transparent parylene, femtosecond laser photoablation of the center of the trench bottom, parylene deposition, and Si etching by XeF_2. This simple yet robust method for creating buried microfluidics by opening the bottom of a parylene-coated channel paves the way for the development of complex microfluidic systems.

2 Experimental

2.1 Design considerations

Our goal was to fabricate a buried channel using a simple procedure. There are a few layout parameters linked to the channel diameter, and each is discussed below.

We wanted to employ two Si etching processes: DRIE and vapor etching by XeF_2. The DRIE etch rate is related to the opening dimension at the lithography mask. Different sizes are etched with different etch rates, resulting in a "lag" effect that researchers sometimes take advantage of (Feng et al. 2018) XeF_2 etching is a diffusion-limited process, and the etch rate through smaller openings in the mask is significantly slower than through larger holes. The different opening sizes during DRIE would subsequently cause an uneven channel diameter, which we decided to avoid; instead, we followed the rule of identical linewidth, resulting in a consistent channel diameter.

XeF_2 etching is a strictly isotropic process in which the vertical etching and lateral undercutting are practically identical, resulting in a semicircular shape. The targeted diameter of the channel was ≈ 250 µm (radius of ≈ 125 µm) and required the removal of ≈ 125 µm of silicon in the vertical direction. This defined a minimum etch depth of more than ≈ 125 µm; therefore, we set the targeted etch depth to 200 µm to provide a 60% safety margin.

The aspect ratio between the linewidth and etched depth during the DRIE process is 1:20 or greater; we chose a linewidth of 20 µm, which results in a non-challenging aspect ratio of 1:10. The etched trench is wide enough to accommodate the laser spot for the subsequent photoablation process. Finally, the trench has to be completely closed with a layer of parylene. If the trench width is 20 µm, then it requires the deposition of 10 µm of parylene, again a non-challenging process step. In this case, we deposited parylene with a thickness of 30 µm to ensure the sealing of the trench. This thickness does not practically affect the channel transparency.

Because the inlets/outlets should have a diameter of ≈ 1 mm, there is an apparent conflict, as the chosen linewidth for the entire design is 20 µm. We used a similar technique as before (Soon et al. 2010), forming overlapping circular channels in the area of inlets/outlets, with three concentric donuts with set diameters of 200, 600, and 1000 µm. The set distance between those lines is 180 µm (radius 2—radius 1—linewidth), which is less than the targeted etching of 250 µm (125 µm × 2). A design with these parameters would result in completely undercut structures at inlets/outlets, resulting in a hole with a diameter of ≈ 1020 µm, whereas the buried channel has the desired diameter of ≈ 250 µm. The subsequent parylene deposition, with a thickness of ≈ 30 µm sealing the trenches, cannot close the inlet/outlet holes. Overall, the maximum size of the channel is limited by the wafer thickness and the minimum size by spot size of the laser for photoablation.

Finally, the channels can be designed with practically any shape, either straight or less regular, e.g., serpentine. The only design rule we would have to follow is the minimum distance between channels given by their diameter. If this rule is not followed, then the channels would merge with each other, which is the desired result in the inlet/outlet regions.

Taking advantage of the lag effect, the process could also be semi-three-dimensional, with areas with shallower channels and smaller diameter and deeper channels with larger diameter. We wanted to avoid this, as it would cause a problem with laser focusing during the photoablation process.

2.2 Chip design

The microfluidic device layout was designed using Nanolithography Toolbox (Balram et al. 2016), a Java script-based software. We chose a simple microfluidic device with three inlets and a single outlet connected by a channel with a length of ≈ 25 mm and a double T-junction originally designed for capillary electrophoresis (Fig. 1). The script file was converted into agraphic database system II file format and transferred via direct-writer laser system onto a soda lime glass mask.

Fig. 1 Layout of a microfluidic chip with a channel, double T-junction, four inlets/outlets, and alignment marks for laser photoablation and for observation. Inlets are labeled with numbers 1, 2, and 3 while the outlet is number 4. Black arrows point to the two alignment marks for laser photoablation, and blue arrows point to the two alignment marks for microscope alignment. (Color figure online)

2.3 Fabrication

The microchannel fabrication was conducted using the Si (100) wafer with diameter and thickness of ≈100 mm and ≈535 µm, respectively. We performed standard lithography using positive photoresist (PR) AZ 9260 with thickness of ≈10 µm (Fig. 2a). After the PR was spun on the wafer, it was baked at ≈110 °C for ≈165 s. Contact lithography was then performed with ultraviolet light exposure of ≈1600 mJ cm^{-2}, split into three individual doses (Fig. 2b). The exposed PR was developed using a KOH-based developer for ≈300 s. We then etched the exposed Si using DRIE [known as the Bosch process (Larmer et al. 1999)] by performing loops consisting of etching and passivation steps with durations of 5 and 2 s, respectively. The etching was performed with SF_6 gas set with a pressure of ≈4 Pa, radio frequency (RF) plasma power of 1800 W, and SF_6 flow rate of $\approx 3.3 \times 10^{-6}$ m^3 s^{-1}. The passivation step with C_4F_8 gas with a pressure of ≈3.3 Pa was conducted with plasma RF power of 1500 W and C_4F_8 gas flow rate of $\approx 3.0 \times 10^{-6}$ m^3 s^{-1}. We used 310 loops to etch the Si substrate to a depth of ≈217 µm (Fig. 2c). We removed the PR using *N*-methyl-2-pyrrolidinone solution at ≈80 °C for ≈600 s. The wafer was exposed to O_2 plasma with power of ≈300 W for

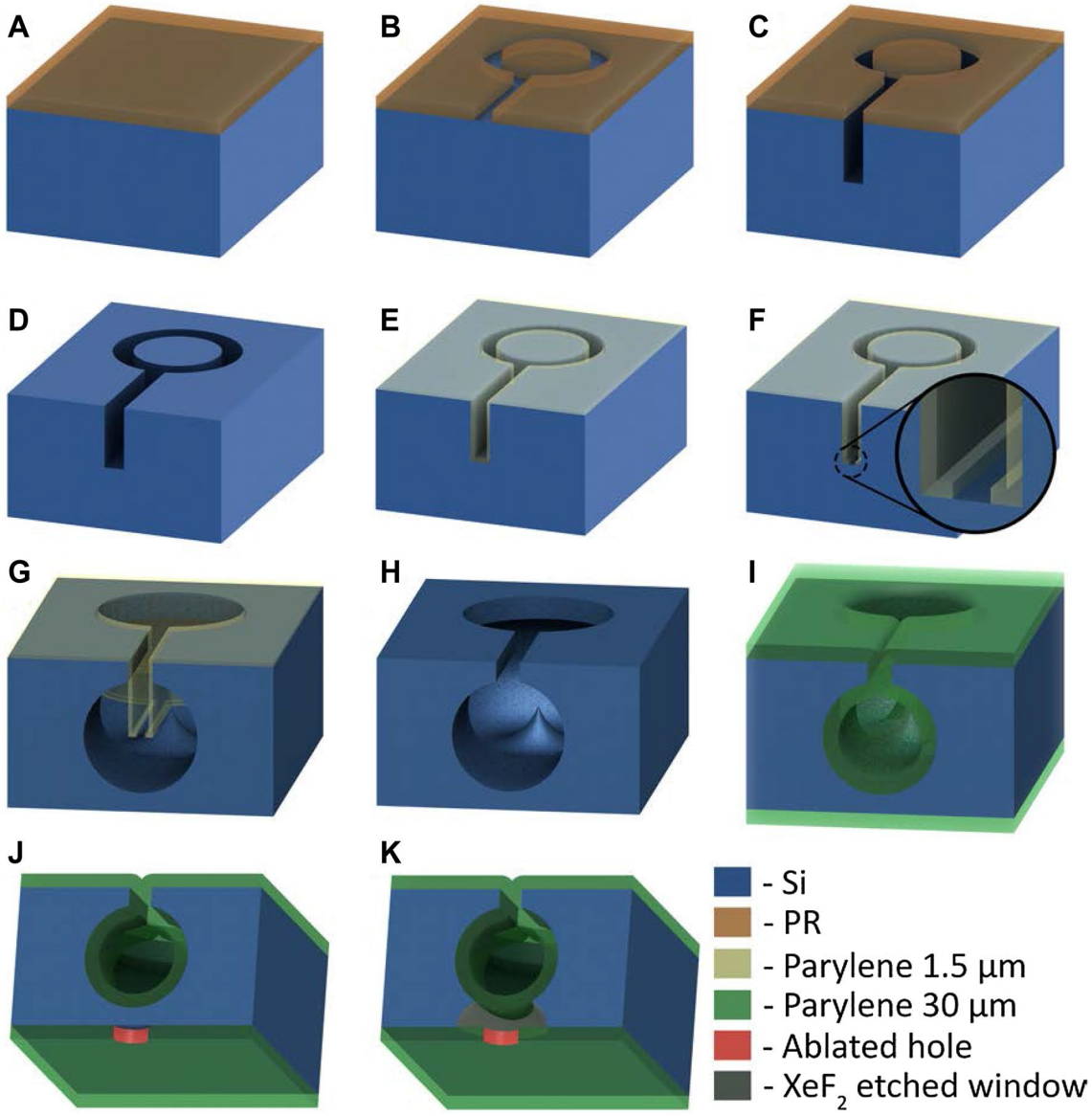

Fig. 2 Wafer fabrication process steps: **a** PR coating; **b** patterned PR after exposure and development; **c** DRIE of silicon substrate; **d** PR stripping; **e** first deposition parylene; **f** photoablation of parylene at the trench bottom (inset shows details); **g** Si isotropic etching using XeF_2 vapor to form the channel; **h** parylene removal using O_2 plasma; **i** second parylene deposition for channel sealing; **j** backside parylene removing; and **k** etching a backside hole by XeF_2 for an observation inside the channel

≈ 180 s at a pressure of ≈ 6 Pa to complete the PR removal (Fig. 2d). Subsequently, we deposited parylene with a thickness of ≈ 1.5 μm using a chemical vapor deposition technique. Parylene provides an excellent conformal coating (Fig. 2e). The pressure in the chamber during parylene deposition was maintained at ≈ 1.6 Pa to ensure uniformity of the parylene layer across the entire sample.

The crucial fabrication step was photoablation of the parylene at the bottom of the trenches using the femtosecond micromachining laser (Light Conversion, model PHAROS PH1-06, Yb:KGW lasing medium) with principal wavelength of ≈ 515 nm. The laser generated ultrashort pulses with duration of ≈ 300 fs with maximum amplitude of pulse energy of ≈ 200 μJ. The laser was focused into the bottom of the trenches using an aspherical lens with focal length of ≈ 40 mm, forming a laser spot size with diameter of ≈ 9.0 μm (Fig. 2f). Because of locally generated heat, photoablation of the parylene layer was performed with no microcracks or shockwave-induced damage to the sidewalls.

Next, we exposed the wafer to the XeF_2 vapors to achieve isotropic etching of the Si at the trench bottom where the parylene layer had been removed by the laser photoablation (Fig. 2g). This Si etching formed a channel with a nearly perfect circular cross-section profile. The parylene layer was then removed by an O_2 plasma etching step with power of ≈ 300 W and duration of ≈ 1 h (Fig. 2h) at O_2 pressure of ≈ 6 Pa. We then deposited a second layer of parylene with a thickness of ≈ 30 μm to seal the channels (Fig. 2i). The deposition parameters were the same as before.

After the structure was finished, we formed a hole in the parylene layer at the chip backside with the femtosecond laser as before (Fig. 2j) and exposed the silicon substrate there to XeF_2 vapor (Fig. 2k). This formed a hole at the chip backside, allowing optical access to monitor the channel.

We checked the most critical fabrication steps with scanning electron microscopy (SEM), starting with the cross-sections of the channel area after DRIE (Fig. 3a). The next image shows the channel after the first parylene layer is completely removed by O_2 plasma (Fig. 3b). Making a cross-section of a chip covered with parylene is tricky because, unlike silicon, parylene is not brittle at room temperature, meaning it cannot be cleaved. We scratched the parylene-covered microfluidic chip with a diamond scriber as usual and placed the chip into liquid nitrogen to cool it to a temperature of ≈ − 195 °C, making the parylene brittle. We then took the chip out, placed it on a wooden support, and cleaved it to show the channel after sealing the trench with parylene (Fig. 3c).

3 Results and discussion

We designed and fabricated a device with a nearly round channel cross-section. The most desirable cross-section of any pipe used for fluid transport is circular, as there are no singularities or imperfections in the flow along the pipe wall. Here, ≈ 87.5% of the cross-section of the etched channel in silicon was circular (Fig. 3b). There was an area next to the originally etched trench with rounded corners probably caused by slightly lower adhesion of the parylene to the silicon sidewalls of the etched trench; thus the undercutting of silicon there. Once the parylene was deposited, the channel was circular with a relatively small area with a "V" shape (Fig. 3c).

We demonstrated operation of this microfluidic device by generating a segmented flow inside the microfluidic system using the double T-junction (Fig. 4a). Because the parylene provides a hydrophobic surface, a segmented flow of water-based fluorescence was formed in a stream of mineral oil. We used this segmented flow system for convenience, as we perform quite a few experiments with this emulsion, especially for polymerase chain reactions. The chip was connected to three syringe pumps: inlet number 1 with fluorescein solution with concentration of ≈ 40 μmol L^{-1} and inlets

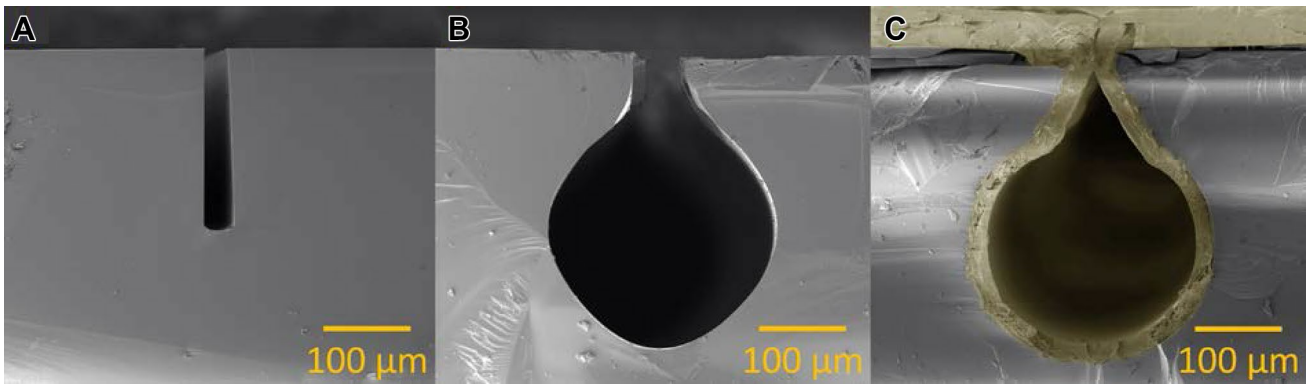

Fig. 3 SEM cross-section images of fabricated microfluidic chip: **a** after DRIE and resist stripping; **b** after photoablation process, silicon etching by XeF_2 vapor, and parylene removal; and **c** after channel sealing with a second layer of parylene (false yellow colors increase the contrast for parylene). (Color figure online)

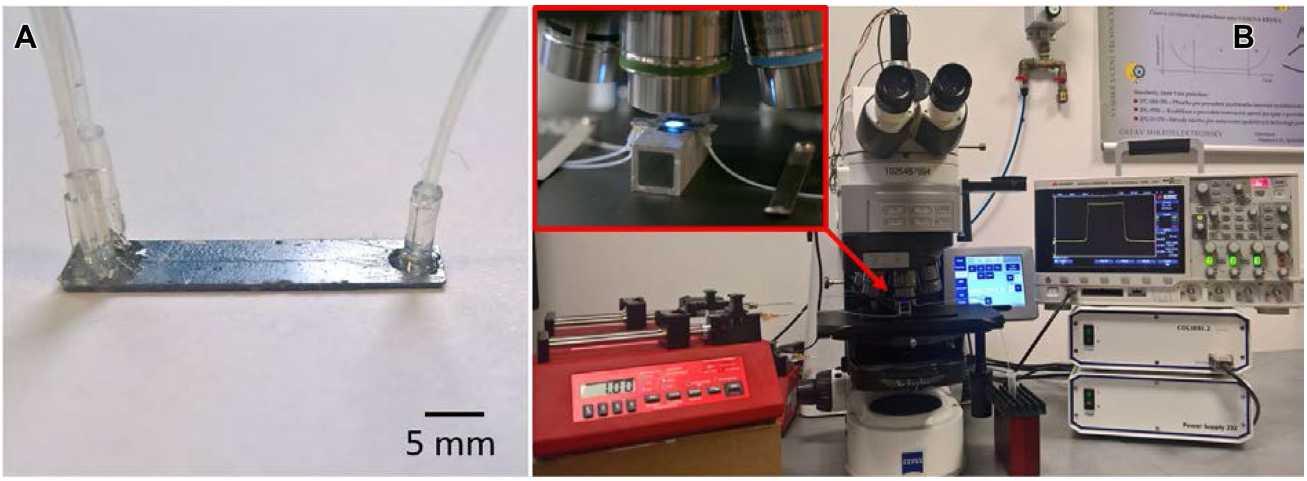

Fig. 4 **a** Fabricated chip with tubing connection; **b** testing setup for microfluidics system

2 and 3 with mineral oil. The center and one side inlet were connected to pumps with oil, while the second side inlet was connected to a pump with fluorescein. All pumps were set to a pumping rate of 1 μL min^{-1}. The chip was placed under an optical microscope (Fig. 4b), with the XeF_2-etched cavity positioned under the objective lens with magnification of 10× and numerical aperture (N.A.) of 0.25.

This visualization allowed us to monitor the flow inside the buried channel inside the opaque Si substrate without obstruction. We also captured the backside view of the channel using SEM (Fig. 5a), which is supported by the optical image (Fig. 5b).

We used a light-emitting diode (LED) with principal wavelength of ≈470 nm to illuminate the channel. We observed the emitted light in the range between ≈500 and ≈550 nm with a CMOS camera and then, to monitor the fluorescence amplitude, with a photomultiplier tube (PMT), both methods with a fluorescein isothiocyanate fluorescence filter set.

The intensity of the fluorescent image was rather low; thus the CMOS camera required a relatively long integration time of a few seconds, resulting in a blurred image. Therefore, we used an LED power supply with external control by a transistor–transistor logic-level signal. We set the exposure time on the camera to trigger a single light pulse with full brightness and duration of ≈5 ms. This system is similar to a photographic flash or a stroboscope that "freezes" the segmented flow image (Fig. 5b). The captured image showed a dynamic contact angle inside the microfluidic channel. The shape of the fluorescein plug was typical for moderately hydrophobic surfaces (Castro et al. 2018).

We then replaced the CMOS camera with a PMT and used an objective lens with magnification of 20× and N.A. of

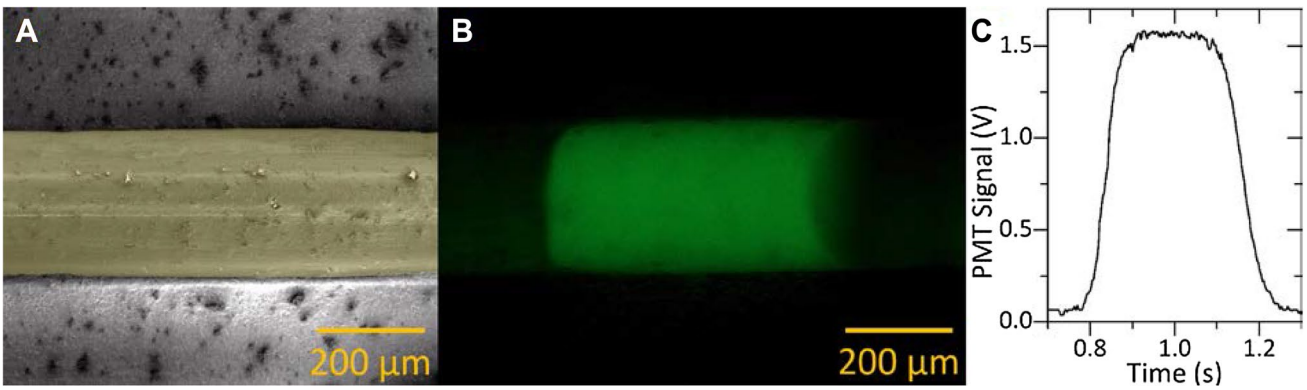

Fig. 5 **a** SEM image of channel from backside view using false yellow-colored parylene for contrast improvement. **b** Optical image of the fluorescein plug in the oil inside the microfluidic channel. The plug has a non-symmetrical shape typical for moderately hydrophobic surfaces. **c** Amplitude of fluorescence as a function of time monitoring the segmented flow inside the microfluidic chip. The rising and falling edges have different shapes, demonstrating the non-symmetry of the plug caused by the moderately hydrophobic parylene coating inside the channel

0.22. The internal microscope aperture was set to minimum to limit the illuminated spot inside the channel. The PMT gain was set to the minimum value by setting the external voltage power supply to 0.5 V, as the fluorescein provided a rather high amplitude signal. The PMT output signal was recorded by an oscilloscope (Fig. 5c).

The signal corresponded to the previous work of a fluorescein/oil-segmented flow inside channels coated with moderately hydrophobic material. This simple experiment demonstrated that the microfluidic chip was successfully fabricated, and we were able to form a segmented flow inside the chip.

4 Conclusion

We demonstrated a method to create a buried microfluidic channel with all processes conducted at ambient temperature.

The process is robust, as the opening in the channel bottom does not interfere with the sidewalls' protective parylene layer, unlike other techniques in which the sidewalls' thin SiO_2 layer is attacked by XeF_2 during Si etching. The technique of opening the bottom of a coated channel is unique and, along with subsequent isotropic silicon etching and parylene deposition, paves the way to utilize this simple method to make BCT chips at ambient temperature. We also introduced a new technique of chip cryo-cleaving at room temperature to obtain a cross-section of a chip covered with non-brittle material with hydrophobic surface properties.

We used this microfluidic device to demonstrate the feasibility of fabrication by forming a segmented flow inside the buried channel. For visualization, we opened a tiny spot at the chip backside and removed Si from that area. The etched hole allowed us to see inside the channel even though the channel was originally buried inside the opaque Si substrate.

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