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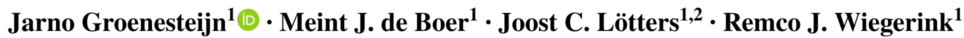
RESEARCH PAPER

A versatile technology platform for microfluidic handling systems, part I: fabrication and functionalization



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Abstract Many microfluidic devices are made using specialized fabrication processes, limiting the ability to integrate those devices on the same chip. In this paper, a versatile technology platform is presented that allows for integration of many different devices. It provides a method to design channels in a wide range of sizes and shapes with different functionalization options in close proximity to the fluid in the channels. The latter includes release of the channels for thermal isolation or mechanical movement and metal or piezoelectric layers for actuation and read-out. The channel walls are made using silicon-rich silicon nitride to provide durable, strong, chemically inert and thermally stable channels directly below the substrate surface .

Keywords Microfluidic · Microfluidic handling system · Fabrication · Microchannel

1 Introduction

A major advantage of microfluidic systems, compared to large-scale fluidics, is the potential for small, accurate, reliable and cost-effective liquid and gas handling systems. While many microfluidic devices have been introduced in the past, most of them require their own specialized fabrication process, limiting the available options to form different kinds of devices. To integrate multiple different devices into one microfluidic handling system, the separate chips often have to be connected using (external) fluidic interconnects. This way, the fluidic interconnects will have a relatively large volume, resulting in slow response times and requiring large sample sizes.

To make the ideal integrated microfluidic handling system, one fabrication process should allow many different microfluidic devices for all kinds of applications to be integrated on the same chip. The functional channels of the devices, the interconnect channels and the required interfacing electronics should be integrated on the same substrate without restricting the design options for each device.

Different applications pose different demands on the fabricated system. To avoid leakage and wear, the channel walls should be mechanically strong, chemically inert and leak tight for both liquids and gasses in a large temperature range. It should be possible to locally release the channel (completely or partially) from the substrate, e.g. for thermal isolation or freedom of movement. It is required to integrate transducer structures for actuation and measurement of the devices. This can be anything from metal tracks to piezoelectric or magnetic materials or optical waveguides. Functionalization of the inside of the channel, e.g. with a catalyst or with specific coatings for (bio)chemical reactions or adhesion should be possible. Multiple channels should be able to cross each other or run inside each other. Interface electronics should be integrated directly on the chip or package to reduce noise and other parasitic effects.

To be able to transfer proof-of-concepts to commercial devices, it should not only be possible to fabricate low-volume research devices, but it should also be possible to scale up the fabrication to industrial low-cost, high-volume processing in foundries. Last, and certainly not least, it should be straightforward to design the optimal fluidic element with respect to shape and size, for any application.

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The microfluidic platform proposed in this paper is based on several fabrication processes for silicon-based microfluidics (de Boer et al. 2000; Rusu et al. 2001; Deladi et al. 2005; Dijkstra et al. 2007, 2012), and with it, we try to approach the ideal platform as close as possible. The previously described fabrication processes were designed for specific applications and were not characterized for use outside those applications. This paper presents a platform that has been adapted from these processes such that it can be applied in a wide range of applications and it has been characterized to be able to use it as a standard tool for easy development of microfluidic devices. The platform features durable, strong, chemically inert and thermally stable channels with silicon-rich silicon nitride (Si_xN_y, SiRN) channel walls directly below the substrate surface which can be used for functional channels in the devices as well as the fluidic connection between devices.

Channels with a hydraulic diameter from less than 10 µm to well over 100 µm can be made within the same device, while the shape of the cross-sectional area can be tuned to the specific application, both without limiting the options for other integrated devices. The channels can be freely suspended, and topside, bottom-side and in-plane fluidic interfacing is possible. Transducer structures can be integrated in close proximity to the fluid using suitable materials. Commonly used actuation and read-out methods that can be combined in this platform are thermal, Lorentz force and electrostatic actuation (Dijkstra et al. 2008; Haneveld et al. 2010; Wiegerink et al. 2011; Droogendijk et al. 2012) and optical, resistive and capacitive read-out (Haneveld et al. 2008; Lötters et al. 2013; Haneveld et al. 2009). The fabrication uses process steps that can easily be transferred to a MEMS foundry, enabling easy upscaling.

An overview of the fabrication process is given in Sect. 2. Methods to integrate additional functionality into the device, e.g. metal tracks for actuation or fluidic inlets, are described in Sect. 3. The platform has been used to fabricate a wide range of microfluidic devices, some examples of these will be shown in Sect. 4. Besides the specific functionalization required for each of these applications, they also require a specific channel design to obtain channels of the right size and shape. While most applications have been presented before, this is the first time that the platform itself is presented in detail. As part of the platform, in Groenesteijn et al. (2017) we will present a method to find the right channel design for the required channels and discuss the fabrication of the channels in detail.

2 Fabrication outline

The fabrication of the devices can be roughly divided into three main steps: fabrication of the microchannels, fabrication of the functional structures and fabrication of the fluidic access to the channels. Two different kinds of wafers can be used: standard silicon wafers and silicon-on-insulator (SOI) wafers. The processing sequence depends on which type of wafer is used. In this section, an outline of the process for both types of wafer is given. The outlines show the fabrication used for the examples shown in Sect. 4 and include some of the functionalization options described in Sect. 3. In this paper, all figures showing a fabrication outline will use the legend shown in Fig. 1.

2.1 Fabrication outline when using standard silicon wafers

Figures 2 and 3 schematically show the outline of the fabrication process when a silicon wafer is used. The two columns each depict one of the following situations:

1. The left column shows a cross section along the length of a channel that is partially released from the bulk of the wafer on the right side and connected to a backside fluidic access hole at the left side.
2. The right column shows a cross-section perpendicular to a channel that will be released from the bulk of the wafer.

The process starts with depositing a 500 nm thick layer of silicon-rich silicon nitride (Si_xN_y, SiRN) using low-pressure chemical vapour deposition (LPCVD) on a 525 µm thick <100> silicon wafer. Using a mixture of 77.5 sccm SiH_2Cl_2 and 20 sccm NH_2 at 850 °C, this results in a layer with a tensile stress between 50 and 100 MPa deposited at about 4 nm min^{-1}. Gardeniers et al. (1996) A 50 nm thick layer of chromium is sputtered at the front side of the wafer. This layer will be used as a hard mask during the channel etch to protect the SiRN. A photoresist layer is deposited and patterned. The pattern contains the etch slits that outline the channel and determine the size and shape of the channels. Using many slits close together will result in a deep, round channel, while many slits spaced far apart will result in a wide, shallow cavity. The relation between the slit pattern and the resulting channel dimensions is discussed in a separate paper (Groenesteijn et al. 2017).

The slit pattern is transferred to the chromium layer using ion beam etching (IBE) and then to the SiRN layer using a directional plasma etch as shown in Fig. 2a. Using a semi-isotropic SF_6 plasma etch, the silicon is etched through the

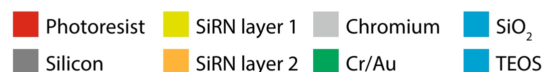

Fig. 1 Legend used in the schematic fabrication steps

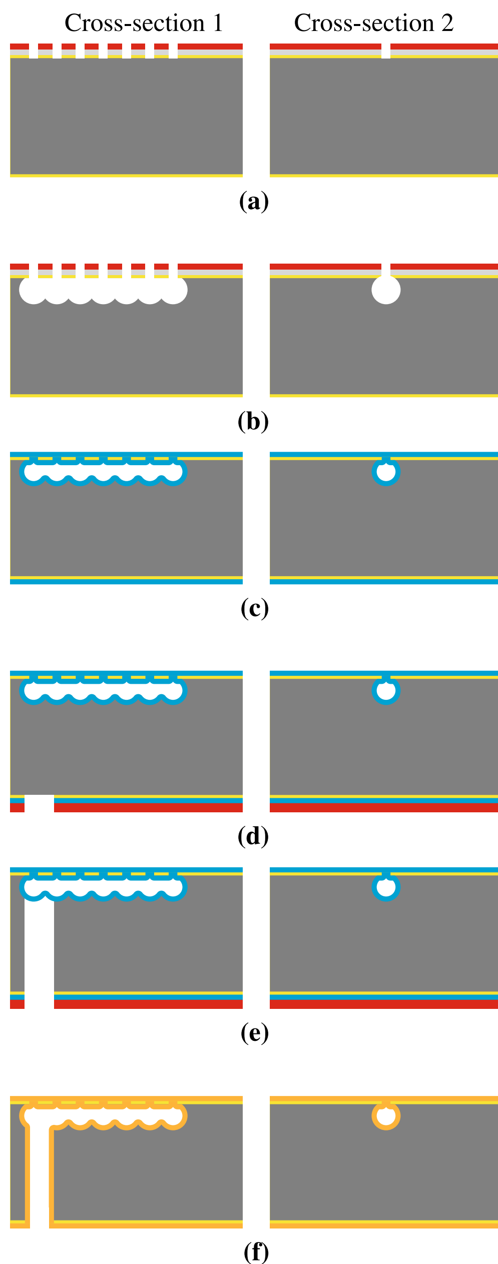

Fig. 2 Fabrication steps for the microchannels in a standard silicon wafer. The *columns* illustrate each step along two different cross sections as discussed at the beginning of Sect. 2.1. **a** Deposition and patterning of SiRN, chromium and photoresist. **b** Etching of the channels through the etch slits. **c** Deposition of a thick layer of SiO_2 using LPCVD of TEOS. **d** Patterning of the photoresist, SiO_2 and SiRN layers. **e** Etching of the backside access holes through the wafer. **f** Removal of SiO_2 and deposition of SiRN to form the channels

etch slits (Fig. 2b). The resist and chromium are removed and a layer of silicon dioxide (SiO_2) is depositing using LPCVD of tetraethyl orthosilicate (TEOS, $Si(OC_2H_5)_4$, Fig. 2c). This layer has two functions. Groenesteijn et al. (2012) The main function is to prevent etching the channels during the etch of backside fluidic access holes when the holes reach the channels. The other function is to protect the channel and the SiRN membrane on top while the channel is handled upside down during the etch from the backside. In our case, 1 µm of SiO_2 is thick enough to perform these two functions. Most critical in this is the required over-etch of the backside fluidic access holes due to wafer- and etch non-uniformities. The deposition temperature of 725 °C is low enough that this process will not change any stress in the previous SiRN layer.

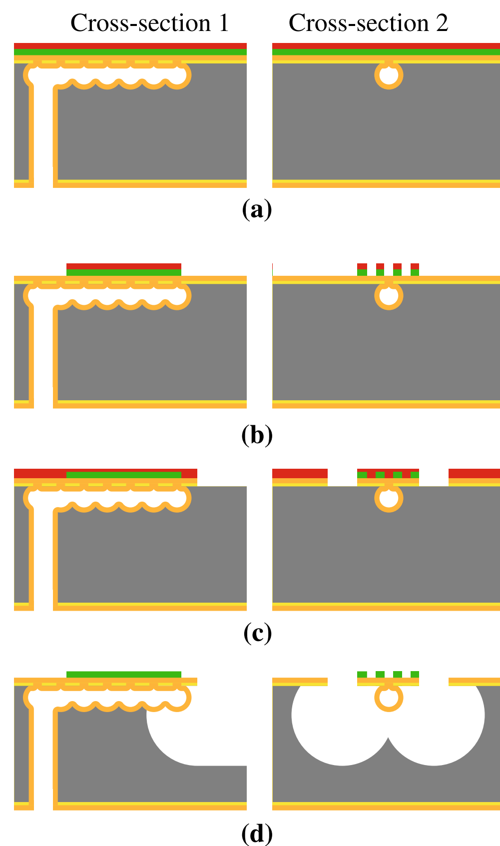

Fig. 3 Fabrication steps for the functionalization of the microchannels. The *columns* illustrate each step along two different cross sections as discussed at the beginning of this section. The legend is shown in Fig. 1. **a** Sputtering of a 10/200 nm thick layer of chromium and gold. **b** Patterning of the resist and the chromium/gold layer. **c** Patterning of the SiRN layer. **d** Release of the channels using an isotropic etch

A resist layer is deposited on the backside of the wafer and patterned using lithography. The pattern, containing the backside access holes, is transferred to the SiO_2 and SiRN layers using a directional plasma etch (Fig. 2d). The backside access holes are then etched through the silicon wafer using deep reactive-ion etching (DRIE). The SiO_2 layer in the channels is used as an etch stop as shown in Fig. 2e. The SiO_2 is removed using a 50% hydrofluoric acid (HF) wet etch and a layer of SiRN is deposited using LPCVD to close the etch slits and form the channel wall (Fig. 2f). The same deposition parameters are used as during the first

layer to deposit a layer of 1.5 µm. Here the LPCVD SiRN is used because of its chemical inertness, high strength, stability and good thermal properties (Williams and Muller 1996; Gardeniers et al. 1996; French et al. 1997; Freitag and Richerson 1998; Williams et al. 2003; Kaushik et al. 2005). In addition, it is biocompatible (Mazzocchi and Bellosi 2008), its surface can be functionalized (Parvais et al. 2003; Arafat et al. 2004) and the stress in SiRN can be tuned by the deposition parameters (Gardeniers et al. 1996; Habermehl 1998) which allows relatively thick layers.

Next are the additional functions. In this overview, we only discuss two optional functions: metalization to form electrodes for actuation and read-out and the release of the channels from the bulk of the wafer. More options are discussed in Sect. 3. Figure 3a shows a 10/200 nm thick layer of chromium and gold that is sputtered at the topside of the wafer, followed by deposition of photoresist. The chromium is used as adhesion layer for the gold. The photoresist is patterned using lithography. The pattern is then transferred to the metal using IBE (Fig. 3b).

After the metal has been patterned, the channels are released from the bulk. This is done by first depositing a new layer of photoresist and patterning it. This pattern contains the etch windows through which the silicon of the bulk will be etched. It also contains the topside fluidic access holes. The pattern is transferred to the SiRN layer by use of a directional plasma etch (Fig. 3c). The silicon is then etched using an isotropic SF_6 plasma etch. To prevent the channels from overheating, the process is done in steps with decreasing power. The last fabrication step is removal of the photoresist layer. An oxygen plasma is used to prevent stiction and capillary forces that might damage the free-hanging channels and structures. The result is shown in Fig. 3d. 3D artist impressions of a device with a backside inlet and a partly free-hanging channel is shown in Fig. 4. The cross sections shown in Fig. 3d are also displayed in Fig. 4a.

The chips can be separated by cleaving or diced, when the channels are protected by ie. a glass cover (Sparreboom et al. 2013).

2.2 Fabrication outline when using silicon-on-insulator (SOI) wafers

When a silicon wafer is used, several steps have to be performed to make sure that the fabrication of the channels and the backside access holes do not interfere with each other. When an SOI wafer is used, the channel and backside access holes are separated from each other by the buried oxide (BOX) layer, which means that they cannot interfere with each other until the BOX layer is etched. However, several extra steps have to be performed to etch the BOX layer. The thickness of the device layer determines the maximum depth of the channels and should be chosen to fit the applications. Here, we use a device layer thickness of 50 µm and a handle layer thickness of 400 µm. In the outline below (Figs. 5, 6), cross sections of three different situations are shown.

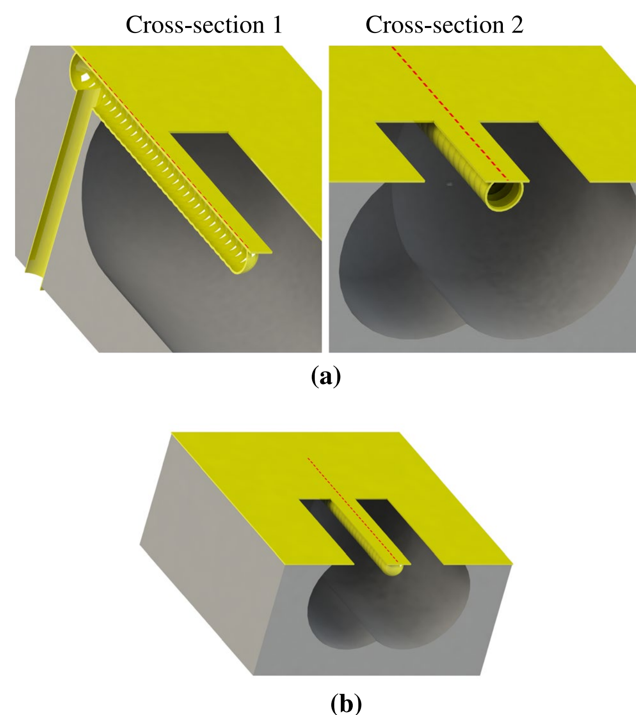

Fig. 4 3D artist impression of the final devices shown in the cross sections in Figs. 2 and 3. The SiRN is shown in *yellow*, while the silicon is shown in *grey*. The locations of the slits are indicated in *red*. The metal tracks on top of the channel are not shown. **a** Artist impressions of the cross sections shown in Fig. 3d. **b** Artist impression of the whole device (color figure online)

1. The left cross section is one along a channel that will be partially released at the end of the process.
2. The middle cross section shows a view perpendicular to two large channels that are connected through the BOX layer while a third, smaller channel is located between the two large channels. The smaller channel will be released at the end of the process, such that it can move freely. A structure like this is used for outflow channels of the in-line proportional valve described in Sect. 4.2. A backside access hole to a channel through the BOX layer is shown as well.
3. The right column shows a cross section of a large channel that is connected to a backside access hole.

Since the BOX layer is going to be used for fluidic channels, it needs to be thick enough so that there is still space left after the channel wall is deposited. Here, we choose for

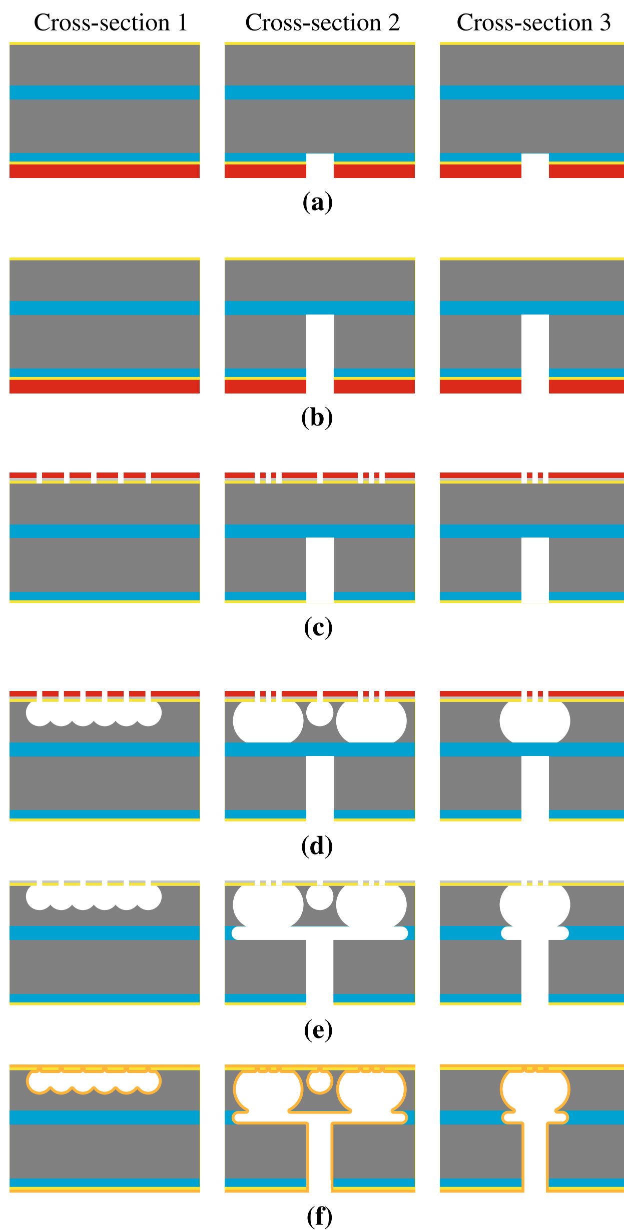

Fig. 5 Fabrication steps for the microchannels. The *three columns* represent the effect of these steps on the three different situations described at the beginning of Sect. 2.2. The legend is shown in Fig. 1. **a** Patterning of the resist, SiRN and SiO_2 at the bottom of the wafer **b** Etching of the backside access holes through the handle layer. **c** Patterning of the slit pattern in the chromium and SiRN hard mask. **d** Etching of the channels through the etch slits. **e** Etching of the BOX layer using HF. **f** Deposition of SiRN to form the channel wall

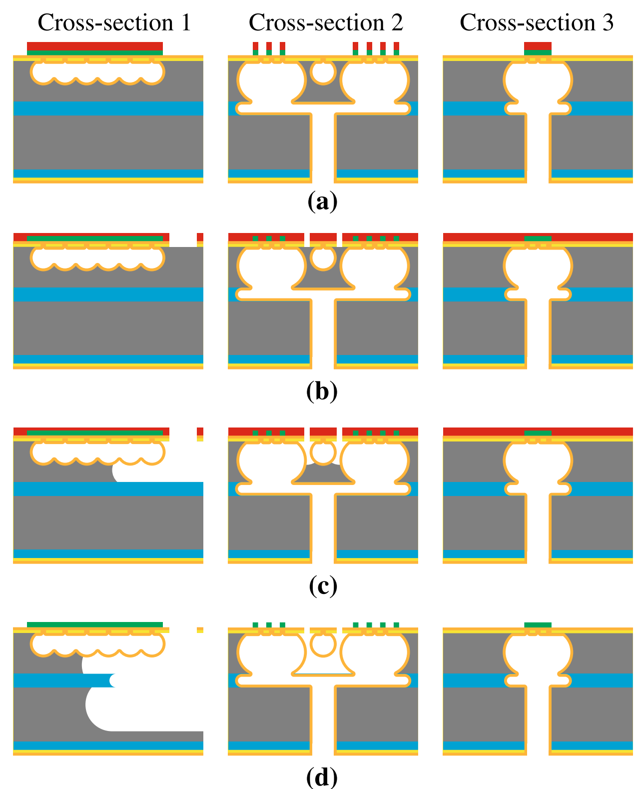

Fig. 6 Fabrication steps for the functionalization of the microchannels. The *three columns* represent the effect of these steps on the three different situations described at the beginning of this section. The legend is shown in Fig. 1. **a** Deposition and patterning of the Cr/Au electrodes. **b** Patterning of the release holes in the SiRN layer. **c** Etching of the device layer to (partly) release the structures. **d** Etching of the BOX layer and silicon underneath to completely release the structures

a BOX layer with a thickness of 5 µm. Due to the production of the SOI wafer, there was also a 4.5 µm thick SiO_2 on the backside of the wafer. The process starts with depositing a layer (1000 nm) of SiRN on the wafer using low-pressure chemical vapour deposition (LPCVD), followed by processing on the backside of the wafer (steps for backside fluid access holes, see Sect. 3.2.2). This SiRN layer is thicker than used with a standard silicon wafer because this layer is also etched during etching of the buried oxide layer. A photoresist layer will be deposited and patterned for etching the backside access holes. The pattern in the resist will be transferred to the SiRN and SiO_2 layers using a directional plasma etch (Fig. 5a). Using deep reactive-ion etching (DRIE), the holes are then etched through the handle layer (Fig. 5b). The BOX layer is used as an etch stop.

After the photoresist is removed, the microchannels are fabricated. It starts by sputtering a 50 nm thick layer of chromium at the front side of the wafer. This layer will function as a hard mask during the channel etch. A photoresist layer is deposited on the chromium and patterned using lithography. This pattern contains the etch slits that outline the channels. The location and density of the slits determine the shape and size of the channels that are etched through them and is discussed in detail in a separate paper. Groenesteijn et al. (2017) Note that in the figures, in the left column, the slits are spaced far apart, while in the middle and right column, sets of slits are placed close together. This will result in channels of different sizes. The pattern is

transferred to the chromium using ion beam etching (IBE). The pattern is then transferred to the SiRN using a directional plasma etch (Fig. 5c). Next the channels are etched using a semi-isotropic SF_6 plasma etch (Fig. 5d). After the photoresist is removed, the BOX is etched using 50% HF. This opens up the connection between large channels in the device layer and backside access holes in the handle layer. This also opens the connection through the BOX layer between large channels in the device layer that are close together. Since the HF etches the SiRN membrane at around 4 nm min^{-1}, the extra thickness of the layer compared to the one shown in Sect. 2.1 gives us an extra two hours of etching time as long as the topside of the wafer is still covered by the chromium layer. To prevent free-hanging structures in the device layer from sticking to the handle layer when the BOX is removed between them, the last part of the oxide can be removed using vapour HF. The SiRN layer is protected by the chromium layer during this etch. The result can be seen in Fig. 5e. The last step to fabricate the channels is to remove the chromium and deposit the channel wall. A thick layer of SiRN is deposited using LPCVD. The thickness of the layer is determined by the width of the slits and should be thick enough to fully close the slits (Fig. 5f). The HF etch also increased the width of the slits and thus a 2 µm thick layer is needed. After this step, the channels are closed and as a result, very hard to clean. Furthermore, there might now be free-hanging structures inside the channel with only a very small gap between the top and the bottom of the channel inside the BOX layer. To prevent contamination and stiction, the rest of the process should be done without using liquids or care should be taken that the fluids cannot enter the channels, e.g. by applying a protective layer over the backside to close the fluidic access holes.

Next are the steps to add functions. In this overview, one metal deposition step is used and the channels are released from the bulk of the wafer. A 10 nm thick chromium adhesion layer is sputtered on top of the closed channels followed by a 200 nm thick gold layer. Afterwards, a photoresist layer is deposited on the metal and patterned using lithography. The pattern contains the electrodes that are used for actuation and read-out of the devices. The metals are etched using IBE to transfer the electrode pattern (Fig. 6a).

The last step is the release of the channels and starts with a photoresist layer which is patterned using lithography. The pattern contains both the etch windows for the release and the topside fluidic access holes. This pattern is transferred to the SiRN using a directional plasma etch (Fig. 6b). The size of the etch windows in this pattern determines the etch rate of the release etch. The etch window in the left column is much larger than those in the middle column, meaning that during the isotropic silicon etch using an SF_6 plasma, much more silicon is etched through the large window than through the small windows. As a result, the BOX layer is reached through the large etch window, but not through the small etch window (Fig. 6c). Since an isotropic etch is used, there will be a ridge underneath the channels until the etch fully reaches the BOX layer. Using vapour HF, the BOX layer is etched at the places where the silicon etch is deep enough. Vapour HF is used instead of liquid-phase HF to prevent stiction and capillary forces from damaging the free-hanging structures. While vapour HF does etch SiRN, no notable deterioration of the channel wall has been found during this etch due to its short etching time (less than 15 min). After the BOX layer is etched, another SF_6 plasma etch is used to etch the silicon at the places where the BOX layer is removed. By not only removing silicon from the device layer, but also from the handle layer, the available space for free-hanging structures is increased. This allows for more freedom of movement or thermal isolation. This step also removes the last amount of silicon around the small channel in the middle column and allows it to move freely between the two large channels. The last step in the process is to remove the resist layer as shown in Fig. 6d. The final results as shown in the left and right cross sections in Fig. 6d are, with the exception of the BOX layer, the same as shown in Fig. 4. The centre cross section results in a more complex structure, of which an artist impression is shown in Fig. 7. The chips can be cleaved or, if the channels are protected, they can be diced (Sparreboom et al. 2013).

3 Process options for extra functionality

For a broad range of applications, it is required to bring functionalization, actuation or read-out methods close

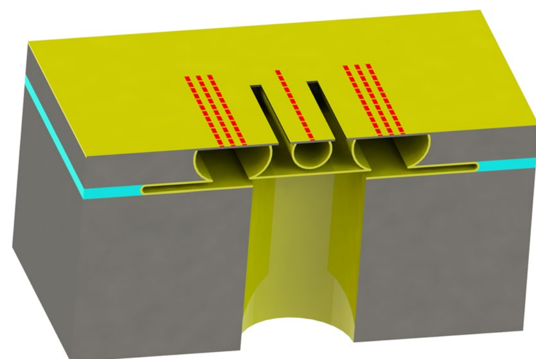

Fig. 7 3D artist impression of the cross section shown in the *centre* of Fig. 6d. The BOX layer is shown in *cyan*, the SiRN in *yellow* and the silicon in *grey*. The locations of the slits are indicated in *red*. The metal tracks on top of the channel are not shown (color figure online)

to or into the fluid channel. After the channel wall has been deposited and the etch slits are closed, the top of the channels is formed by a thick SiRN layer. When a wide channel is made, this layer can be considered as a membrane which can also be used for specific functions. The strength of the SiRN allows for further processing of the wafers on top of these membranes, for instance, to integrate transducer structures. Below, several options are given that can be integrated in the microfluidic platform proposed in this chapter.

3.1 Functional layers

3.1.1 Buried oxide layer

Section 2.2 shows that the process can also be done using silicon-on-insulator (SOI) wafers to allow certain functions. By designing channels of various depth, localized access to the BOX layer allows for integration of specific features. Using an SOI wafer usually adds two subprocesses to the total fabrication process. One to etch the BOX layer for functionality inside the channels (before the channel walls are deposited) and one to etch the BOX layer during the final release of the channels. When a long under-etch is required for the functionality of the BOX layer, it should be taken into account that etching using HF also etches SiRN (Williams and Muller 1996), and the thickness of the initial SiRN layer and the maximum allowable slit width should be changed if etched for a long time. In the case of vapour HF, a compound ($(NH_4)_2SiF_6$) is formed that might impede proper functioning of the device and should be removed by heating up the wafer (Witvrouw et al. 2000; Vereecke et al. 2000). A downside of using an SOI wafer is that the maximum depth of the channels is limited by the thickness of the device layer, which can be a problem when large channels are needed. Figure 8 shows several possible structures which can only be made using an SOI wafer. These options can be roughly divided into three groups where the BOX layer is used

- to selectively reach the handle layer during processing (Fig. 8a)
- as an electrical or mechanical isolation of a part of the device layer (Fig. 8c)
- as a fluidic channel (Fig. 8b, d).

Figure 9a shows a deep channel of varying width that was etched to the BOX layer during the channel etch. The following HF etch removed the BOX layer, resulting in a smooth, flat bottom of the channel. Figure 9b shows wide channels that reach to the BOX layer during the channel etch. Since they are encircling parts of the device layer, they electrically and mechanically isolate those parts.

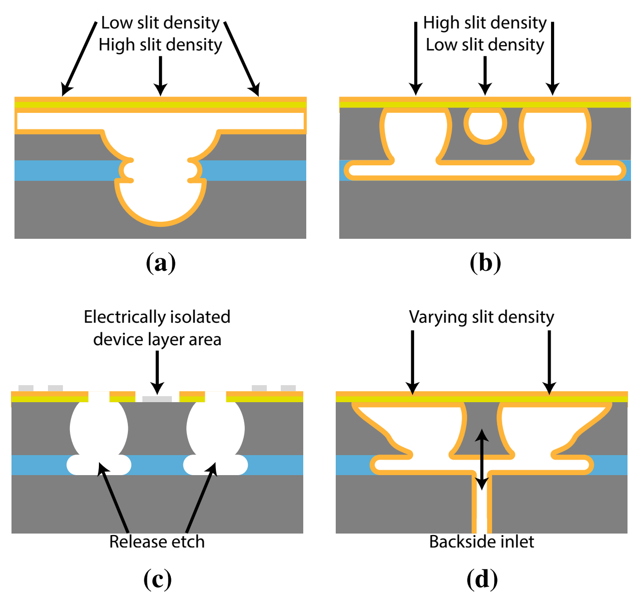

Fig. 8 Cross sections of several possible structures that can only be made using an SOI wafer. **a** Localized etching of the handle layer. **b** Crossing channels through the BOX. **c** Electrically isolated area of the device layer with external electrical contact. **d** Valve with a variable channel through the BOX Groen et al. (2015). The legend is shown in Fig. 1

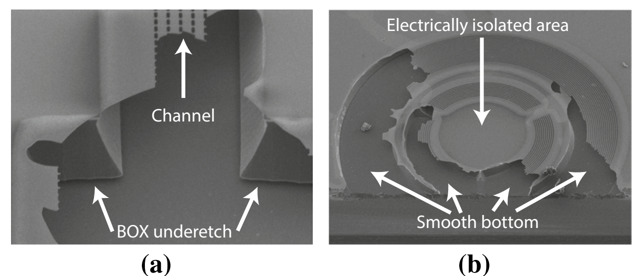

Fig. 9 **a** SEM image of a deep channel of varying width that reached the BOX layer during the channel etch. **b** SEM image of channels that reached the BOX layer and electrically isolated a part of the device layer

3.1.2 Metal layer

Metalization on top of the channels allows for integration of actuation and read-out methods close to the fluids. Sputtered layers of Cr/Au and Pt have been shown to provide enough step coverage to cover the small pits in the SiRN when the metal is crossing the closed etch slits (Fig. 10). To pattern the metal layers, preferably dry etching methods, like (reactive) ion beam etching ((R)IBE), should be used to prevent contamination of the channels. The metal layers have been used in this platform for thermal read-out (Dijkstra 2009; Lammerink et al. 2011) and actuation (Lötters

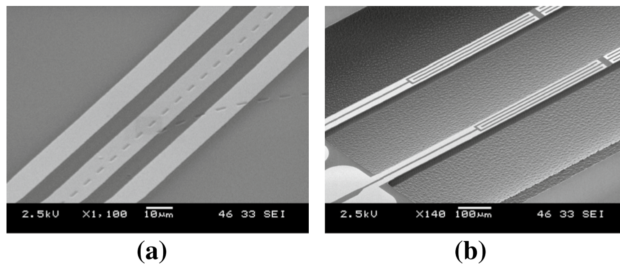

Fig. 10 SEM images of metal (10/200 nm Cr/Au) tracks on **a** closed etch slits and **b** released channels

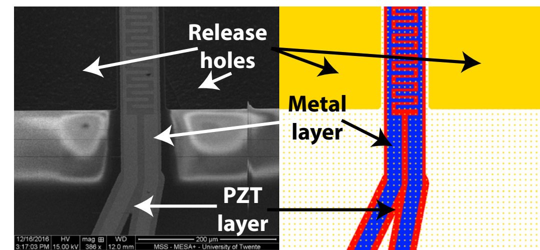

Fig. 11 SEM image and corresponding mask design of a PZT layer on a released channel. On *top* are interdigitated electrodes made using a titanium/platinum layer of 15/100 nm thick. The release window is shown in *yellow* in the design. The PZT layer in *red* and the metal electrode (with PZT underneath) in *blue*. The *bright coloured* parts in the SEM image that are not shown in the design correspond to the SiRN membrane that is under-etched during the release etch (color figure online)

et al. 2013), capacitive read-out (Haneveld et al. (2009); Lötters et al. (2015)) and actuation (Wiegerink et al. 2011; Droogendijk et al. 2012), resistive read-out and magnetic/Lorentz force actuation (Haneveld et al. 2008; Groenesteijn et al. 2012, 2014). Fabrication of metal functional structures is shown in Figs. 3 and 6 for fabrication using silicon and SOI wafers, respectively.

By etching the SiRN layer on top of the wafer before depositing the metal allows for electrical contact to the silicon underneath. This connection can be used to electrically ground the silicon or to use parts of the device layer (after electrical isolation, see Sect. 3.1.1) for electrical functions. If a contact between the silicon and the metal on top of the SiRN layer is required, the metal deposition should have sufficient step coverage. Experiments have shown that a step of 2.5 µm can be covered with a sputtered Cr/Au layer of 10/200 nm thickness.

3.1.3 Piezoelectric layer

Lead zirconate titanate (PZT, $Pb[Zr_xTi_{1-x}]O_3$, with $(0 \leq x \leq 1)$) is a piezoelectric material that can be deposited on a wafer using pulsed laser deposition (PLD, Blank et al. 2014), atomic layer deposition (ALD, Watanabe et al. 2006) or applying a sol–gel (Budd et al. 1985), while research is being done to find lead-free alternatives (Shrout and Zhang 2007). Using a piezoelectric material might replace the Lorentz force actuation and capacitive read-out used in the micro-Coriolis mass flow sensors and enables development of a new range of sensors and actuators, e.g. on-chip actuated valves, peristaltic pumps or ultrasonic flow sensors.

All three deposition methods require heating the wafer to temperatures over 600 °C in order to create crystalline PZT. In the processes described in Sect. 2, this would mean that the PZT layer will have to be deposited before the Cr/Au layer is deposited or the metal layer has to be exchanged with a metal that can withstand such high temperatures (e.g. platinum). Figure 11 shows a patterned, 1.4 µm thick layer of PZT on top of a channel which is, at the top, released from the bulk. On top of the PZT, there are Ti/Pt (15/100 nm thick) interdigital electrodes. The bright areas next to the PZT are caused by charging of the SiRN that has been under-etched during the channel release etch.

3.2 Channel functions

3.2.1 Channel release

Freely suspended channels can be used for many applications. When the channels are free of the silicon bulk, they can be used in fluid-mechanical resonant applications and it enables isolation of the channel from the silicon bulk. This reduces the influence of, e.g. thermal conductivity or electrical capacitances, enabling sensing of thermal or electrical properties of the fluid. Releasing channels from the bulk silicon can be done by creating etch windows and using an isotropic etching process to etch the silicon underneath the channels. Since the etch rate depends on the size of the etch window (Jansen et al. 1997), the depth (and thus also the width) of the release cavity can

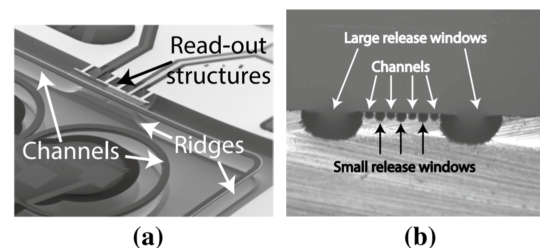

Fig. 12 **a** SEM image of a released channel. A ridge underneath the channel is formed due to the isotropic etch. **b** photograph of four partially released channels

be tuned to the required dimensions, e.g. when a channel needs to be partially released. Figure 12a shows a SEM image of a released channel. Underneath the channel, there is a ridge caused by the isotropic etch. The capacitive read-out structures at the top significantly reduce the (local) area of the etch window, resulting in a much higher ridge. Figure 12b shows a microscope photograph of four partially released channels. Large etch windows at the side resulted in deep etch cavities, smaller etch windows between the channels resulted in etched cavities only slightly larger than the channels themselves. The relevant steps to release the channels from the bulk of the wafer are shown in Figs. 3 and 6 for fabrication using standard silicon and SOI wafers, respectively.

3.2.2 Channel access

Fluidic access holes are required that can vary from small pores, for instance, for evaporation, to large holes to apply a fluid flow. Fluidic access holes to the channels can be made using three different methods: from the top, the side (inline) or the bottom.

Topside fluidic access Access holes from the top can be etched in the same step as when the etch windows for the release etch are etched (Fig. 3b, c) and offer direct access to the channels. However, connecting external fluidic connectors to topside access holes can increase the complexity of packaging methods since the relatively large size of external connectors can interfere with mechanical protection of the chip and with the electrical connections. If anything is connected to the topside fluidic access holes, that connector is in direct contact with the membranes on top of the fluidic channels. Stresses induced by this connection can easily break these membranes. Some success has been achieved by gluing a connector to a large section of the chip. Dijkstra et al. (2007) Topside access can also be used in cases that no connector has to be attached. For instance, as outlet for gasses or pores for evaporation.

In-plane fluidic access In-plane fluidic access holes to the side of the chip are in effect microchannels that are opened during singulation of the chips, allowing for in-plane fluidic access to the channels. However, making a leak-tight fluidic connection to the side of the device requires careful engineering of the package. If an external connector is placed on these access holes it will, just like with the topside access holes, be in direct contact with the membrane on top of the channels. In Dijkstra et al. (2014), an open in-plane fluidic access channel is used as inlet for a micro-Prandtl tube, where no external connector is connected to the chip as shown in Fig. 13b.

Bottom-side fluidic access Bottom-side access holes require extra fabrication steps in the form of a wafer-through etch, but has the advantage that the access holes

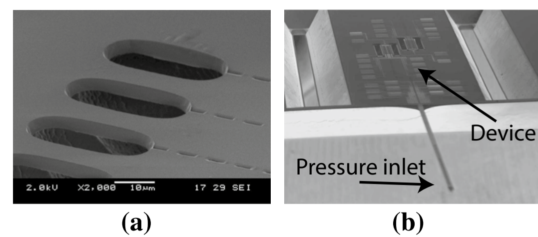

Fig. 13 SEM image of **a** a gas outlet Dijkstra et al. (2007) and **b** an in-plane fluidic inlet for a micro-Prandtl tube. Dijkstra et al. (2014)

are now separated from electrical or mechanical interfacing with the microchannels and thus allows for easier packaging. If external connectors are used to connect to the access holes, they will be connected to the flat underside of the chip and will not be able to damage the channels.

Fabrication of the bottom-side access holes depends on whether an SOI wafer is used or not. When a silicon wafer is used, a method has to be used to separate the channel-etch process and the backside DRIE process during etching. That is, if the channels are etched first, the DRIE process will also etch inside the channels once the access hole reaches them, resulting in unwanted large cavities at the inlets. This can be prevented by depositing a protective material, e.g. SiO_2 by LPCVD of TEOS, which closes off the channels and prevents them from etching. The SiO_2 can be removed afterwards using, e.g. HF. When etch slits are made on top of the SiO_2 layer, the slit will be damaged during etching due to notching, resulting in a wide slit which requires a thicker SiRN layer to close. This means that the channels have to be etched such that they connect to the side of the access hole, or the channels must be etched before the access holes. In the latter case, the backside processing will be done with the membranes on top of the channels in place, which risks damaging them. Using access trenches instead of round holes, wafer-scale non-uniformity in the DRIE process can be reduced to avoid the need for over-etching (Groenesteijn et al. 2012). The relevant steps are shown in Fig. 3.

When an SOI wafer is used, the backside inlet can be etched after the initial SiRN layer has been deposited and before the channels are etched, using a DRIE process that reaches through the handle layer to the BOX layer as shown in Fig. 5. After the DRIE process, the channels in the device layer can be patterned and etched. By making deep channels above the access holes, the access holes are connected to the channels when the BOX layer is removed. Since any processing on the backside is done before the channels are made, there is no chance of damaging the thin membranes on the topside when the wafer is processed upside down. Figure 14 shows two bottom-side access holes: one in a silicon wafer and one in an SOI wafer.

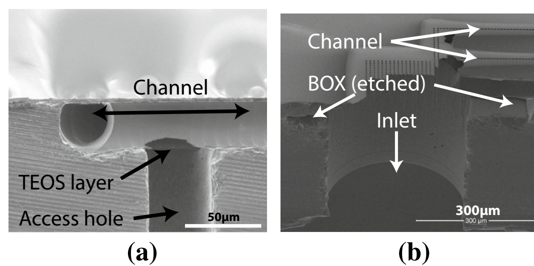

Fig. 14 SEM image of **a** an access hole in a wafer without buried oxide layer and **b** an access hole in an SOI wafer

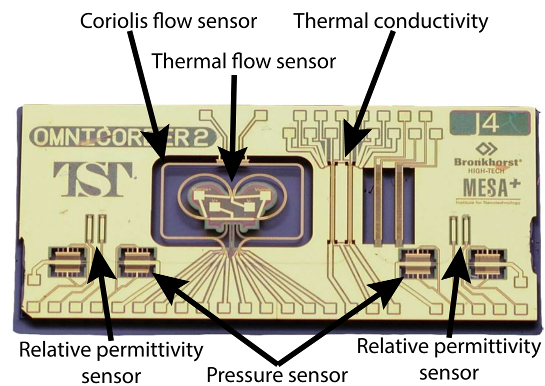

Fig. 15 Photograph of the single-chip multi-parameter microfluidic measurement system

4 Applications

Many different devices have been made based on the microfluidic platform described in this paper. Lötters et al. (2014), Lötters et al. (2015), Alveringh et al. (2015), Groenesteijn et al. (2016a), Groen et al. (2015), Groenesteijn et al. (2016b), Groenesteijn (2016), Larsen (2016). As an example to show the possibilities of the platform presented here, the designs of a multi-parameter flow sensor and a Coriolis mass flow controller with integrated proportional control valve are described here. The different devices that are integrated and the required functionalization steps are discussed. The designs are made using the channel-etch model described in Groenesteijn et al. (2017). Details of the devices and measurement results of these systems are shown in the cited papers. The multi-parameter flow sensor has been realized on a standard silicon wafer using the process outlined in Sect. 2.1. The micro-Coriolis mass flow controller is made using SOI wafers, and the fabrication outlined in Sect. 2.2.

4.1 Multi-parameter flow sensor

In Lötters et al. (2014), Lötters et al. (2015), Alveringh et al. (2015), Groenesteijn (2016), we proposed a single-chip multi-parameter microfluidic measurement system made in the fabrication process outlined in Sect. 2.1. This system does not use any of the functions offered by using an SOI wafer, but it can also be fabricated on an SOI wafer without changing the design, e.g. to integrate it with the proportional valve discussed in Sect. 4.2. The system comprises a thermal flow sensor, a Coriolis flow and density sensor, a relative permittivity sensor, pressure sensors (both at the inlet and outlet) and a thermal conductivity sensor. Each of these sensors poses different requirements on the size and shape of the channel. Using these sensors, the composition of mixtures can be calculated from the physical properties density, viscosity, heat capacity, thermal conductivity and relative permittivity. A photograph of the final chip indicating the separate sensors is shown in Fig. 15.

4.1.1 Flow sensors

The fluid flow is measured using two methods: using a thermal (calorimetric) flow sensor and using a Coriolis flow sensor. In Lammerink et al. (2011), we showed this combination in order to increase the total dynamic range of a flow sensor. In that case, the thermal flow sensor should have a flow range which slightly overlaps with that of the Coriolis sensor. This was achieved by using two channels with identical cross section, resulting in a Coriolis flows sensor capable of measuring down to 10 mg h^{-1}, while the thermal flow sensor could measure up to 30 mg h^{-1} of water. However, in the current system, the flow range should overlap more to be able to use the Coriolis mass flow sensor while calculating the specific heat. The Coriolis flow sensor model presented in Groenesteijn et al. (2016a) shows that the sensitivity of the Coriolis flow sensor is increased by decreasing channel diameter, while Groenesteijn (2016) shows that the maximum flow the thermal flow sensor can measure is increased by a long heater. To sufficiently increase the length of the heaters, without also increasing the pressure drop, the diameter of the channel should also be increased. This will have no influence on the flow performance of the sensor, as long as the diameter can be considered small compared to the length of the heaters. Both channels should be fully released from the bulk of the chip. For this, release holes of at least 250 µm are etched on each side of the channels. Since the thermal flow sensor consists of two circular channels inside the rectangular Coriolis sensor, this results in a large open cavity.

4.1.2 Relative permittivity sensor

The relative permittivity of a fluid can be measured by measuring the capacitance between an electrode on top of the channel and the grounded substrate underneath the channel. Modelling this as a parallel plate capacitance, this means that the electrode area should be large (long, wide channel) and the distance between the electrode on top of the channel and the substrate should be small (shallow channel). The channel should not be too wide to avoid dead volumes. A channel of 110 µm wide, 700 µm long and 45 µm deep would result in a capacitance of 15 fF when the channel is filled with air ($\varepsilon_r = 1$). Filled with water ($\varepsilon_r = 80$), this would increase to 1.2 pF. To reduce the (mostly) fluid-independent capacitance to the side of the channel, the channel is partly released using 25 µm wide release windows next to the channels.

4.1.3 Pressure sensor

The pressure inside the channels can be measured by measuring the deformation of a channel. The deformation can be measured by measuring the capacitance between comb fingers on the channel and on the bulk of the chip. If the bottom of the channel is embedded in silicon and thus kept from deforming, the top of the channel will bend upwards at increasing pressure. The tilt of comb fingers attached to the channel is a measure for the applied pressure. In Alveringh et al. (2015), we showed that a wider channel will result in a higher sensitivity (in ° bar^{-1}). However, a smaller membrane can withstand higher maximum pressure before breaking and the design is thus a trade-off between high sensitivity and high maximum pressure. To avoid dead volumes in the fluid path, the channel in the pressure channels is chosen to be at equal size as the channels connecting the different sensors. These connecting channels should have a large hydraulic diameter to avoid high pressure drop over the system. At a channel width of 90 µm, the maximum stress in the membrane will stay below 100 MPa at a pressure up to 2 bar, which is sufficient for the application. By using release windows of 150 µm, the channel will be mostly etched free, giving it as much freedom for deformation as possible, while making sure that the bottom of the channel is still inside the silicon bulk.

4.1.4 Thermal conductivity sensor

To measure the thermal conductivity of the fluid, heaters are placed on top of the channel, while the silicon bulk acts as heat sink. To accurately measure the thermal conductivity of the fluid, the amount of heat that is dissipated through other means (ie. conduction through the SiRN channel wall or fluid flow) should be minimized. This can be done by partly releasing the channel from the bulk, by making the channel very long and by using a small channel. For this, the size of the channel is chosen equal to that of the Coriolis flow sensor, while the length is chosen to maximally use the available chip space, resulting in a 2.5 mm long channel.

4.2 Micro-Coriolis mass flow controller

In Groen et al. (2015), Groenesteijn et al. (2016b), we proposed a mass flow controller comprising of a proportional control valve and a Coriolis mass flow sensor integrated on the same chip. The valve uses the BOX layer as a channel of which the height can be adjusted to control the flow and thus requires an SOI wafer. The process for this is outlined in Sect. 2.2. A photograph of the final chip is shown in Fig. 16a with the valve in detail in Fig. 16b. Figure 16c shows an artist impression of a cross section of the valve along the black line in Fig. 16a, b.

The chip contains three different devices: a Coriolis mass flow sensor, two identical pressure sensors and an in-line proportional control valve. The Coriolis flow sensor is designed much like the one in the multi-parameter sensor. However, the flow controller is intended to be used with gasses, which means that the small channels would have a high pressure drop over them. By using channels that are about twice as large as those used in the Coriolis flow sensor of the multi-parameter sensor, the pressure drop will be approximately 8 times lower. The used pressure sensor is identical to the pressure sensors

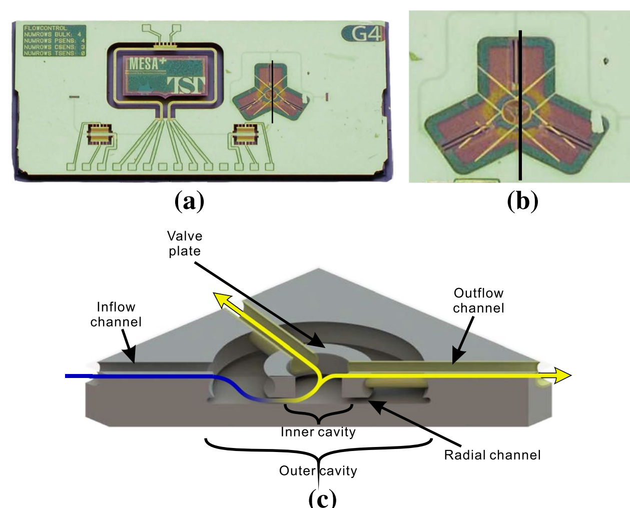

Fig. 16 **a** Photograph of the micro-Coriolis mass flow sensor with integrated proportional control valve. **b** Detailed photograph of the control valve. **c** Artist impression of the cross section of the valve showing the flow-patch. The cross section is taken at the *black line* in **a** and **b**

in the multi-parameter sensor. The valve consists of three different slit patterns:

- *Inner cavity* should be as small as possible while still reaching the BOX layer.
- *Outer cavity* should also reach the BOX layer, but can be much larger. The membrane on top will bend when the valve is opened or closed. By using a large membrane, the stress during bending will be reduced.
- *Outlet channels* these channels go through the outer cavity to the outside of the valve. These are as small as possible to have minimal influence on the outer cavity and to make sure they can be released from the surrounding silicon.

5 Discussion

There are many different methods of making microfluidic systems on a chip, each with its own advantages and challenges. Mark et al. (2010), Iliescu et al. (2012), Nge et al. (2013), Temiz et al. (2015), Kim and Meng (2015) The platform presented here is our attempt at creating a platform that can be used as widely as possible, but it is not possible to offer all advantages of other platforms, without any of their drawbacks.

One of the advantages of this platform, a very thin channel wall, also is one of its drawbacks. The thin channel wall allows for very sensitive measurement and handling of the fluid inside the channels; however, the pressure sensor presented in Sect. 4 works well because the partly released channel deforms due to the pressure inside the channel. When the channel is not used as a pressure sensor, this deformation can disrupt the normal operation. In Alveringh et al. (2015), we also show that large membranes can already burst at only a few bar pressure. However, tests have shown that small channels of around 40 µm diameter can withstand pressures of well over 200 bar. Due to these effects, it is inadvisable to design channels with diameters larger than 80 µm when they are released or wider than 200 µm when they remain embedded in silicon when operating at more than a few bar above ambient pressure.

During fabrication, the channel is etched in the silicon underneath a SiRN layer. The advantage of this is that the channels can be closed in one step using LPCVD and the channel wall thus exists from one, chemically inert material. Since the channel wall that is formed this way is very thin, external influences on the fluid (like thermal or electric actuation or read-out) can be brought in close proximity with the fluid. Fabricating the channels using this method allows for control of the shape and size of the channel by tuning the slit pattern used to etch the channels. It also does not require any (wafer-) bonding steps, like many glass- and polymer-based fabrication methods. However, a disadvantage of this method is that it does not allow us to apply any materials on the inside of the channel wall, except by flushing them through the whole system. In effect, this means that features like electrodes inside the channel or local functionalization of the channel wall are, so far, not possible in this platform.

6 Conclusions

A first step has been made towards an universally applicable microfluidic fabrication platform. The platform features microchannels directly below the substrate surface with diameters from less than 10 µm to well over 100 µm with a thin channel wall made of SiRN. These different channel sizes and shapes can be integrated on the same device by varying the etch-slit pattern. Using SiRN for the channel walls ensures that they are durable, strong, chemically inert and thermally stable. Functional structures can be easily integrated in close proximity to the fluid. The channels can be freely suspended, and topside, bottom-side and in-plane fluidic interfacing is possible. The separate fabrication steps that have previously been used have been characterized and the process flow was improved where necessary. New options have been investigated and added to the process when they proved useful. Using an SOI wafer as base for the platform allows for many new functionalities that were previously not possible.

Several examples are given of devices made using this platform to show how versatile the platform can be applied.

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