TECHNICAL PAPER

A low power static noise margin enhanced reliable 8 T SRAM cell

Appikatla Phani Kumar[1] · Rohit Lorenzo[1]

Abstract

This paper investigates a low leakage power 8 T (LP8T) SRAM cell with high read and write stability. The proposed LP8T (PLP8T) SRAM cell has separate write and read bit lines. As an outcome, the read disturbance is removed. Furthermore, the utilization of a schmitt-trigger (ST) inverter enhances the read stability. Moreover, the write assist technique can enhance the writing ability. When compared to conventional-6 T SRAM, the PLP8T SRAM cell improves HSNM, RSNM, and WSNM by $1.4\times$ $2.3\times$ and $1.3\times$ respectively. The PLP8T SRAM's read and write access times are lowered by 53.24 and 42.18%, respectively. The PLP8T SRAM has a 50% lower read and write power than conventional-6 T SRAM. In addition, there will be a sufficient improvement when compared to chang10T, HSWA9T, SEDFC8TT, and ST11T SRAM cells.

1 Introduction

In portable applications, the design of a low-power circuit is the main challenge because of several issues. The SRAM covers a significant part in the area of the chip, so it has the main contribution to the overall power utilization of the chip. Hence, the design of a low-power SRAM is significant and needs effort (Islam and Hasan 2012). It faces many performance and process-related challenges. Therefore, the low-power SRAM design draws the attention of the researcher. Supply voltage (VDD) scaling is the best way to minimize power utilization, but it degrades the performance and static noise margin (Lorenzo and Paily 2019). Moreover, due to technology scaling the influence of PVT (Process, Voltage, and Temperature) changes is increased on the performance of SRAM. Temperature dependency of leakage currents is significant in VLSI circuits, because they work at elevated temperatures due to power dissipation. The stability of SRAM cell is indicated by noise margin. Thermal noise and gate leakage current noise are the main contribution to total noise in a MOS transistor. These should be considered while designing an

SRAM (Soeleman and Roy 1999). The static noise margin (SNM) is directly proportional to VDD and exponentially related to the threshold voltage. Hence, the RSNM (read static noise margin) and WSNM (write static noise margin) are degraded. Furthermore, reading and writing stabilities are impaired. Due to technology scaling, the amount of standby power in the overall power of the cell is increasing. The leakage power is significant because the SRAM cells usually stay in hold mode for more time(Ahmad et al. 2018).

Therefore, to implement low-power memory circuits with reliable functioning, it is needed to design an SRAM cell to overcome the above mentioned drawbacks. Low power can be achieved in the subthreshold operation, where the supply voltage is lower compared to threshold voltage. But, the delay raises exponentially. Therefore, we can go for a near-V_{th} region in which the power supply is slightly more than the threshold voltage (Calhoun and Chandrakasan 2006). A large reduction in power can be achieved in this region and also there is a considerable improvement in delay can be achieved compared to sub-threshold operation. As an outcome, energy utilization can be reduced by optimization between delay and power with the near-threshold operation. Equation-1 shows that the drain current in the subthreshold region is exponentially proportional to gate to source voltage. So, the subthreshold leakage increases, if V_{DD} is less than the threshold voltage. Therefore, the operation in near-threshold region can reduce the subthreshold leakage. As a result, the static power consumption is reduced.

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$$I_D = I_{Do} \exp\left(\frac{vgs - v_t}{nv_t}\right)\left(1 - \exp(\frac{-v_{ds}}{v_t})\right) \qquad (1)$$

where I $_{Do}$ is the subthreshold current at $V_{gs} = 0$, V_t means threshold voltage, V_{ds} means drain to source voltage, and V_{gs} means Gate to source voltage.

Because of its unsatisfactory RSNM (read static noise margin) at low V_{DD}, the conventional 6T SRAM has a significant probability of reading disturbance. As a result of its failure to maintain the device strength ratio under minimum energy operation, the cell cannot be able to switch the storage node data, resulting in writing failure (Lorenzo and Pailly 2020). To solve the issues in SRAM cells, numerous design configurations have been developed so far. Using a different path for write and read operations, the cells proposed in Samandari-Rad and Hughey (2016); Lorenzo et al. (2022) exhibit better enhancement in RSNM due to cross-connected inverters being isolated from bit lines. Utilization of one-sided structures is the critical solution to mitigate dynamic power consumption because the bit line activity factor is minimized to lower than 0.5. On the other hand, a one-sided cell not able to perform the write-1 operation without a write assist technique, especially at lower voltages. To perform write operation successfully, several one-sided cells have been developed. A schmitt trigger SRAM cell (Cho et al. 2020) and a half select free write assist SRAM cell (Lorenzo and Pailly 2022) have been developed earlier to enhance RSNM and WSNM at the same time. These cells show robust behavior, under process variations. On the other hand, these cells have the drawback of dynamic power consumption and area. To address the aforementioned issues, here we have proposed a low leakage power 8 T (LP8T) SRAM cell.

The proposed LP8T SRAM has the following features.

1) For write and read operation, it has different bit lines.
2) Single-ended structure can reduce energy consumption and area.
3) Enhancing the static noise margin.
4) Read stability is enhanced using cross-connected standard and ST inverters
5) Write-ability is enhanced using the ST inverter write assist technique.
6) Leakage or hold power consumption of the cell is also reduced.

Here's how the paper is arranged. Section 2 narrates the existing SRAM cell designs. The proposed design is introduced in Sect. 3. Comparison of simulated results is described in Sect. 4. The paper is concluded Sect. 5.

2 Earlier reported SRAM cells

2.1 Conventional6T-SRAM cell

The conventional6T SRAM is illustrated in Fig. 1, which suffers from reading failure-induced SNM degradation with VDD scaling (Torrens et al. 2017). So, it is hard to get enough read and write stability at a time. Another challenge in 6 T SRAM is the small .

ON–OFF current ratio of access transistors, which do not allow to incorporate more number of cells in every vertical column of a memory array. This 6 T SRAM cell consumes 26.5 µW and 24.12 µW power in read and write operations respectively. The read and write access times of this cell is 165.82 pSec and 143.54 pSec respectively.

2.2 Chang-10T SRAM cell

Chang10T SRAM is illustrated in Fig. 2, which is designed to enhance the RSNM. This cell eliminates the half select problem by turning off the additional transistors connected in series to pass gate in write operation (Chang et al. 2009). However, this circuit has two serial transistors in the write path, which shows poor WSNM. Due to its differential structure, this cell has energy consumption, and area overheads, and consumes more read or write power. It consumes a read power of 22.86 µW, write power of 21.38 µW. The leakage power of chang10T SRAM is 2.43 nW. The read and write access times of this cell is 77.29 pSec and 85.96 pSec respectively.

2.3 HSWA9T SRAM cell

A half select free write assist 9 T (HSWA9T) SRAM is illustrated in Fig. 3. This cell uses read decoupled and feedback cutting write assist technique to enhance RSNM and.
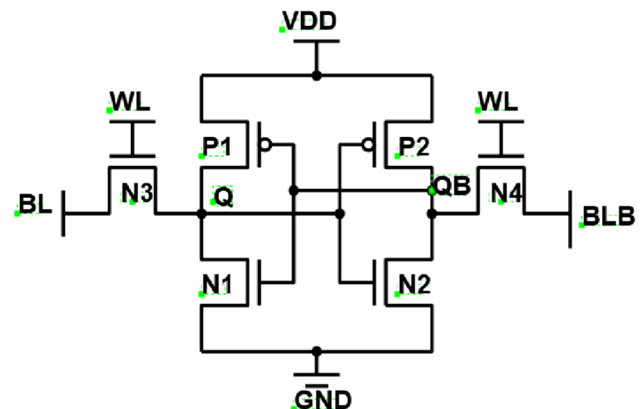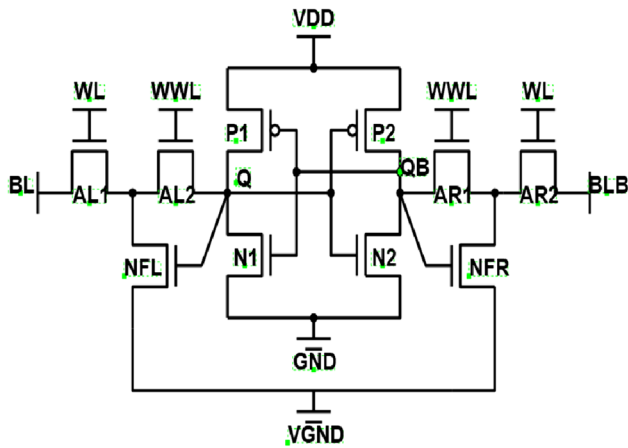

Fig. 1 Conventional-6T SRAM cell
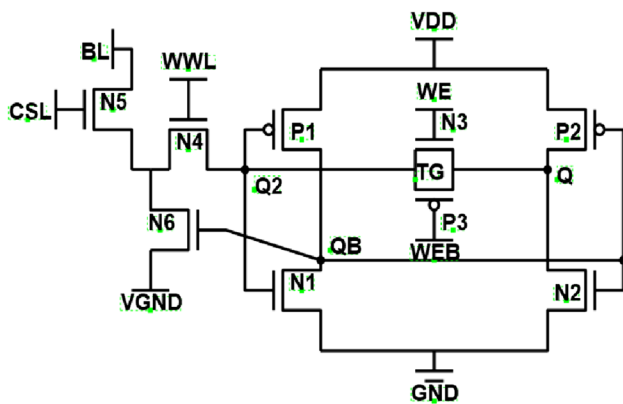
Fig. 2 Chang10T SRAM cell

Fig. 3 HSWA9T SRAM cell

WSNM. It consumes less power because of one-sided structure (Pal et al. 2019). The complexity of the circuit is increased due to a greater number of control signals. The delay of the circuit is more. The read and write power utilization of this cell are 24.26 µW and 23.47 µW respectively. The leakage power of this SRAM is 3.001 nW. The read and write access times of this cell is 127.48 pSec and 113.38 pSec respectively.

2.4 ST11T SRAM cell

Schmitt trigger-based 11 T (ST11T) SRAM cell, depicted in Fig. 4, designed to enhance HSNM and RSNM. Due to cross-connected ST inverters hold stability is enhanced and separate read buffer improves the read stability (Ahmad et al. 2016). The write-1 ability is improved by row based floating VVSS scheme. The write-1 operation is performed by only one cell and the remaining all perform the write-0 action. So, the write-0 cells can drive the VVSS. Hence, write-1 ability enhancement is not significant. Due to the increased transistor count, this cell has the wide area. This cell consumes read and write power of 15.74 µW and
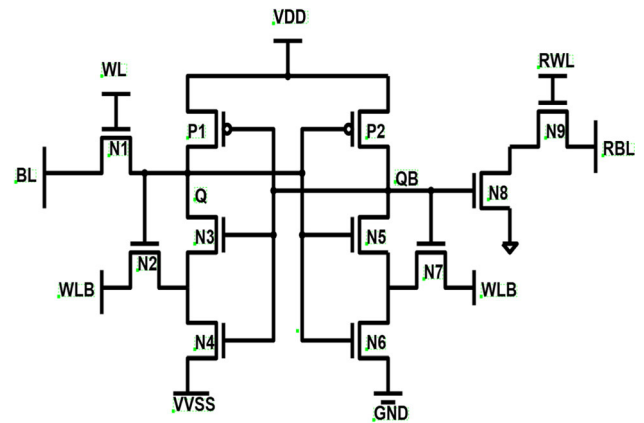

Fig. 4 ST11T SRAM cell

15.89 µW respectively. The read and write access times of this cell is 72.68 pSec and 95.42 pSec respectively.

2.5 SEDFC8T SRAM cell

Single-ended dynamic feedback control (SEDFC) 8 T SRAM cell is depicted in Fig. 5. It works at the ultra-low voltage in sub-nanometer node (Kushwah and Vishvakarma 2015). This SEDFC8T SRAM cell uses dynamic feedback cutting with one-sided write to improve the writing ability and to overcome read disturbance it uses dynamic read decoupling. Read and write power consumption of the cell is less but due to subthreshold operation, subthreshold leakage occurs. The read power of this cell is 16.68 µW and the write power is 14.89 µW, and the leakage power is 2.073nW. The read and write access times of this cell is 71.46 pSec and 128.75 pSec respectively.
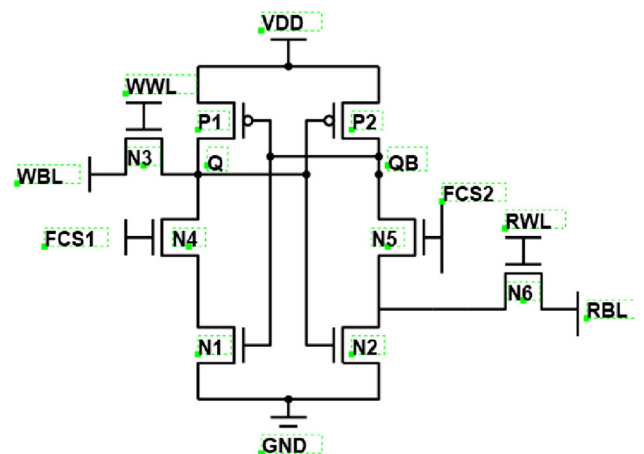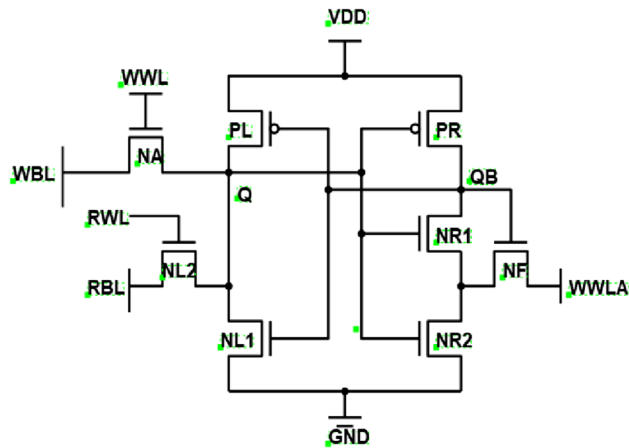

Fig. 5 SEDFC8T SRAM cell

Fig. 6 Proposed LP8T SRAM cell

3 Proposed LP8T SRAM cell

The circuit diagram of PLP8T SRAM is illustrated in Fig. 6. The PLP8T SRAM is mainly comprises a cross-coupled pair of the conventional inverter (PL, NL1) and schmitt-trigger inverter (PR, NR1& NR2). The transistors NA and NL2 are write and read access transistors respectively and.

are operated by row-based control signals WWL and RWL respectively. The drain of the feedback transistor (NF) is connected to WWLA which is a column based control signal. The PLP8T SRAM uses individual bit lines for write and read operations such as WBL and RBL respectively. Different control signals used in LP8T SRAM for various operations are shown in Table 1

3.1 Hold operation

In hold mode both read and write word lines (RWL and WWL) are disabled. So, the write and read access transistors are turned OFF. This decouples the storage nodes from bit lines and the controls signal WWLA is enabled to maintain feedback. So, the hold stability is improved.

Table 1 Control signals in PLP8T SRAM

Signals	Hold	Read	Write-0	Write-1
RBL	1	1	1	1
RWL	0	1	0	0
WBL	1	1	0	1
WWL	0	0	1	1
WWLA	1	1	1	0

3.2 Read operation

During the read mode, the write word line (WWL) is made low to eliminate writing paths, while WWLA is enabled. As a consequence, the normal inverter can drive the storage node Q. Firstly, RBL is pre-charged to VDD. When RWL is made high to turn ON the NL2, then RBL may be discharged or remains at pre-charge value depending on the storage node (Q) value. Generally, failure in reading occurs due to the read failure from the bit line. When read disturbance occurs at the storage node, its voltage overshoots the inverter's trip voltage, the storage node data can be altered. But in the proposed design, we use an ST inverter and its trip voltage is high compared to the normal inverter. Hence, the data cannot be inverted. Therefore, the proposed LP8T SRAM cell mitigates the problem of reading failure by utilizing the cross-connected ST inverter and conventional inverter along with a separate read path. RSNM is also enhanced like HSNM.

3.3 Write operation

To initiate the write mode operation, the read word line (RWL) is first disabled, which turns off the NL2 and disables the read path. Then WWL is activated to turn ON the access transistor (NA). So, the data from WBL can be transferred to the storage node. Either write-0 or write-1 can occur based on the data at WBL. To perform write-0 operation WWLA made'1', WBL made'0' by write driver and for write-1 operation, WBL made'1' by write driver, and column-based WWL is switched to "0". Hence, the feedback is removed from the ST inverter and its trip voltage becomes equal to the standard inverter. Hence the schmitt trigger inverter behaves like a normal inverter. The storage node Q is driven to'1' via the access transistor and the Schmitt-trigger inverter output QB is now switched to'0'. Then the WWLA is changed to'1' after QB data is flipped.

However, due to the NMOS access transistor's weak drivability, there is no sufficient improvement in write ability. The negative V_{WWL} technique is used to enhance the write-1 ability of the proposed design. When WWL is applied with negative voltage, the node Vx immediately becomes negative due to the activated feedback transistor. The reduction in Vx can increase the robustness of PR1, which decreases the schmitt trigger inverter's trip voltage.

So that, the write-1 operation becomes easy. In the write-1 operation when WWL is made "0", the feedback is removed and the trip voltage is reduced by 21.9%. When WWL is applied with a negative value of −0.2 V, the reduction in trip voltage is 52.4%. Therefore, the write-1

ability is significantly improved by the negative VWWL assist technique (Kulkarni and Roy 2011).

4 Simulation results and Comparison

In this segment, the analysis of simulation outcomes and comparison with previous SRAM cells are presented using FinFET-18 nm technology. The performance parameters considered for the comparison are static noise margin, delay, power, and leakage power (Tu et al. 2010). All the performance metrics analyzed at 27 °C temperature. The PLP8T SRAM cell is compared with conventional6T, chang10 T, HSWA9T, ST11T, and SEDFC8T SRAM cells. Transistor sizing plays a vital role in read and write stabilities (Ahmad et al. 2017). The factors that affect the stability of SRAM are attentively considered for design (Lorenzo and Chaudhury 2017a). Typically, the β ratio should be in between 1.2 and 3 for better RSNM. The γ ratio should be less than 1.2 for better WSNM (Kumar et al. 2016). The design parameters of the transistors considered in the design is given in Table 2 All the transistors considered in this design have same parameters.

4.1 Hold static noise margin

The stability of SRAM is measured using a parameter called static noise margin (Gupta and Roy 2015). The hold stability corresponds to HSNM, which can be obtained using the butterfly curve. Due to the utilization of cross-connected conventional inverter and ST inverter, the HSNM of PLP8T SRAM is improved compared to previous SRAM cells. Figure 7 shows the comparison of HSNM of PLP8T SRAM with conventional6T and SEDFC8T SRAM cells.

4.2 Read static noise margin

The SRAM stability is determined in reading mode by a parameter called RSNM, which is estimated with the help of butterfly curve. Read butterfly curves of PLP8T SRAM,

Table 2 Parameters of transistors considered in the design

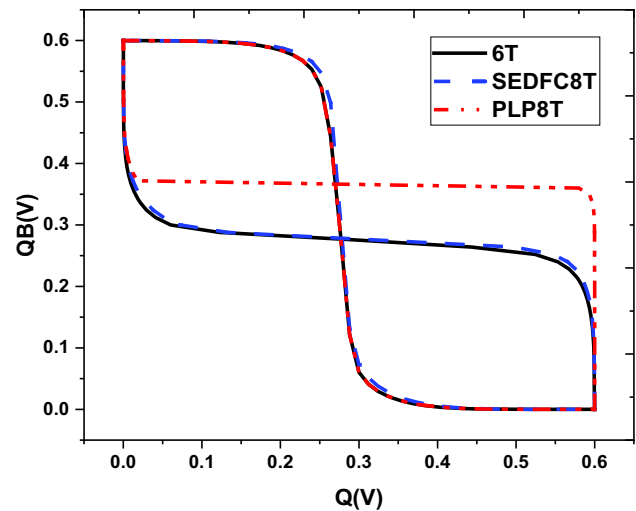| Parameter	Value
Transistors selected for design	p1svt, n1svt
Gate length	18 nm
Fin pitch	48 nm
Number of fins perfinger	2
Number of Fingers	1
Threshold voltage	0.25 V

Fig. 7 HSNM comparison of PLP8T SRAM with 6T SRAM

conventional 6 T SRAM, and SEDFC8T SRAM are plotted at 0.6 V and illustrated in Fig. 8. Because read decoupling is used in the Chang10T, HSWA9T, and ST11T cells, the RSNM is the same as the HSNM. The conventional6T cell suffers greatly from reading disturbance due to the single path for read and write with the information storage nodes (Chiu et al. 2014). Due to its robust read path transistor, the SEDFC 8 T SRAM has a high RSNM than the conventional−6 T SRAM. Because of the robust cross-coupled construction of the conventional inverter and ST inverter, as well as the separate read path, the PLP8T SRAM has the high RSNM.
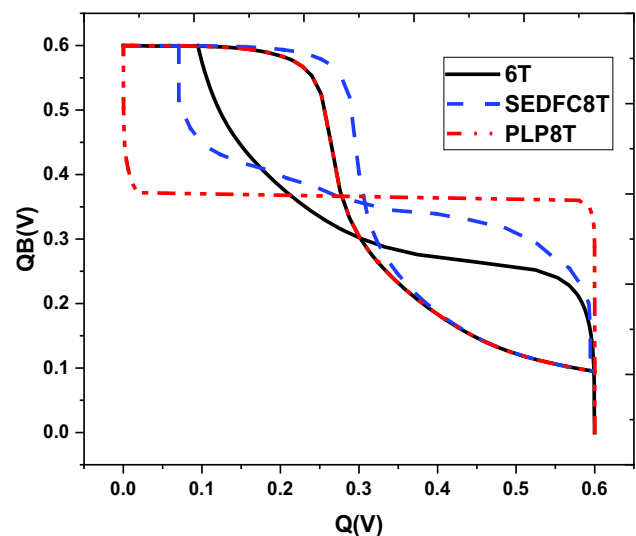

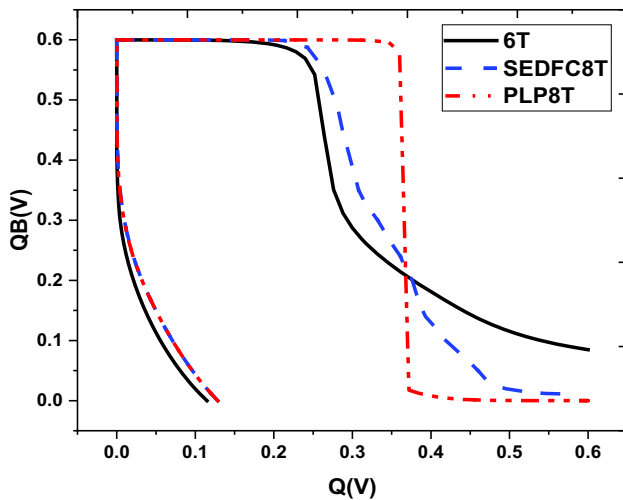**Fig. 8** RSNM comparison of PLP8T SRAM with 6T SRAM

Fig. 9 WSNM comparison of PLP8T SRAM with 6T SRAM

Fig. 10 Read and write access time comparison of PLP8T SRAM

4.3 Write static noise margin

The writing capability of the SRAM cell is calculated by a parameter named WSNM (Aly and Bayoumi 2007). Figure 9 depicts the WSNM of the PLP8T, conventional-6 T SRAM, and SEDFC8T SRAM cell at a 0.6 V power supply. Because two serial connected transistors are existed in the writing paths and the lack of write-assist technology, the HSWA9T and Chang10T memories have the lower WSNM than other studied memories. The 6 T and SEDFC8T cells have a greater WSNM compared to other cells due to the presence of single access transistor in the writing channels. Because of the write-assist approach utilized in these memories, the WSNM of SEDFC8T, and ST11T cells is greater than that of the other SRAM cells. Because of the cross-connected structure of the conventional inverter and ST inverter, the proposed LP8T cell offers maximum WSNM.

4.4 Read and write access time

The duration from the moment word line (WL) reaching VDD/2 to the moment sensing yield 5σ is measured as read access time (Roy and Islam 2020a). Write delay can be defined as the time just after WL reached to VDD/2, when stored data reached to 90% of VDD (Pal et al. 2020). Figure 10 depicts the comparison of read and write access times of proposed LP8T SRAM with all studied SRAM cells. In this proposed cell write access time is longer compared to chang10T SRAM cell, due to its differential bit line structure. The proposed LP8T cell has a read access time of 66.43 ps and a write access time of 92.83 ps which is less compared to traditional-6 T, HSWA9T, SEDFC8T, and ST-11 T SRAM cells.
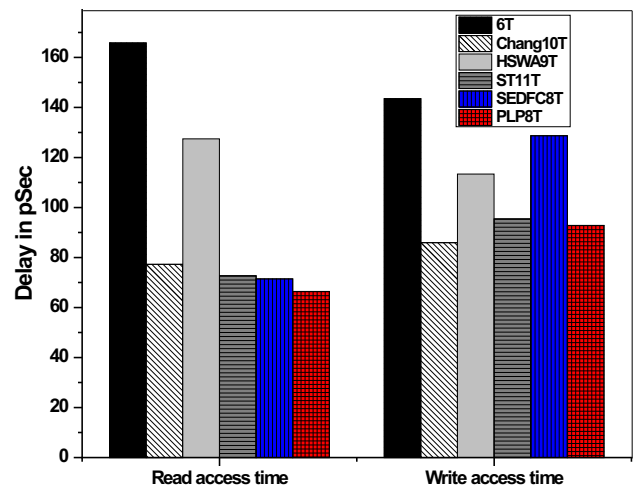
4.5 Read and write power

In single-bit-line architectures, power utilization is reduced due to low switching activity of BL (Lorenzo and Chaudhury 2017b). The discharging and charging of the bit line takes less power, matching to differential bit line structures (Roy and Islam 2020b). Hence the read and write power utilization of PLP8T SRAM cell is lower than chang10T, SEDFC8T, HSWA9T, and ST-11 T SRAM cells as it uses a single bit line. The read power of PLP8T SRAM is minimized by 53.24% comparing to conventional6T-SRAM. The read power comparison of PLP8T SRAM at various process corners is depicted in Fig. 11. Write power of conventional-6 T SRAM is maximum amid all other cells. In PLP8T SRAM cell write power is lowered by 42.18% comparing to traditional-6 T SRAM. However, the read power of HSWA9T, chang10T, SEDFC8T, and ST-
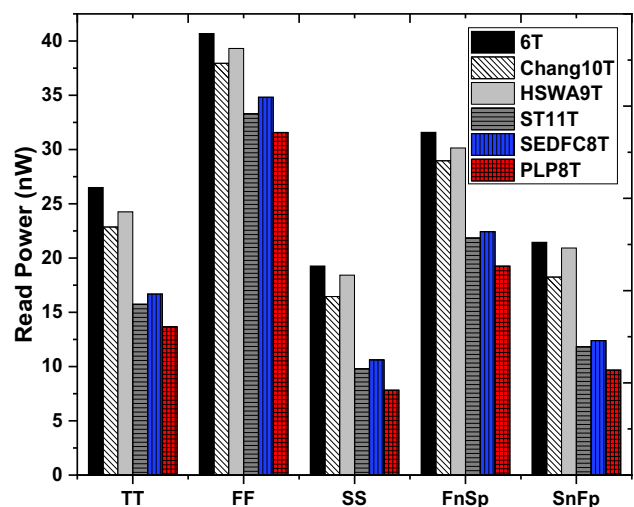

Fig. 11 Read power comparison of PLP8T SRAM at different process corners

11 T SRAM cells are high because of a greater number of transistors in the reading path. The comparison of write power consumption of PLP8T SRAM cell with previous SRAM cells at various process corners demonstrates in Fig. 12. Montecarlo simulations are performed for 500 samples to observe the mean and standard deviation. The read power distribution plot is depicted in Fig. 13. Similarly, the write power distribution plot is depicted in Fig. 14. From Figs. 13 and 14 it is evident that the mean value of read and write power is 13.6102 nW and 11.5708 nW respectively.

4.6 Leakage (or) standby power

Standby power is a key parameter to consider while designing a low-power SRAM (Roy and Islam 2019), especially in latest technologies where the ratio of standby power to total power is rising. This is due to the SRAM cell spends the majority of its time in standby mode. The two main sources of the total leakage current are gate leakage current and subthreshold leakage. The gate leakage decreases because of the high-K insulation employed at this technological node. Therefore, the leakage in sub-threshold region takes the critical role in finding the total leakage current estimate in the deep nanometer regime (Sinha and Islam 2017). The comparison of PLP8T SRAM's leakage power with earlier reported SRAM cells at different temperatures is illustrated in Fig. 15 and the comparison with integer values is given in Table 3 It is observed from the hold operation that, all leakage paths are removed in hold mode from bit lines and V_{DD} to ground. Hence, the PLP8T SRAM cell consumes less leakage power.
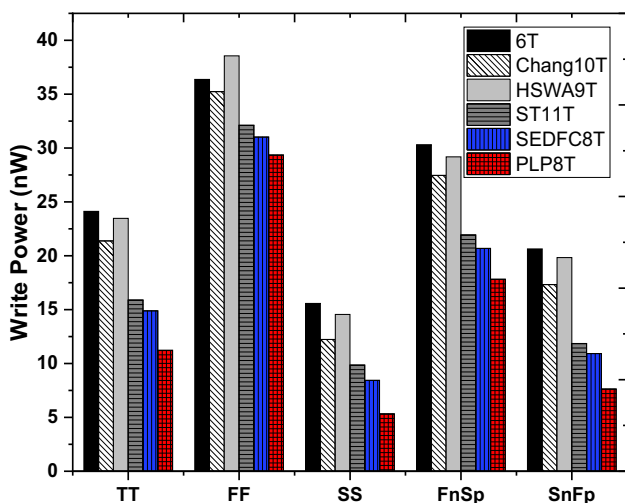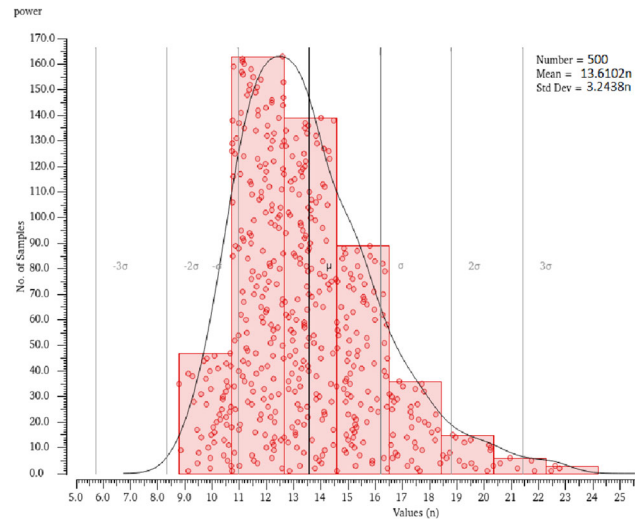

Fig. 13 Read power distribution of PLP8T SRAM cell

Fig. 14 Write power distribution of PLP8T SRAM cell

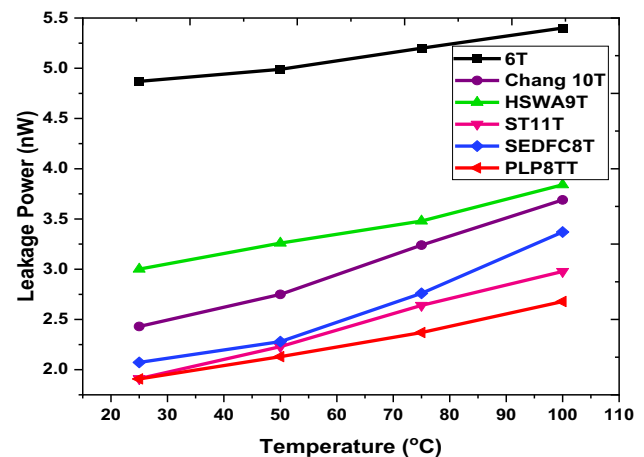Fig. 12 Write power comparison of PLP8T SRAM at different process corners
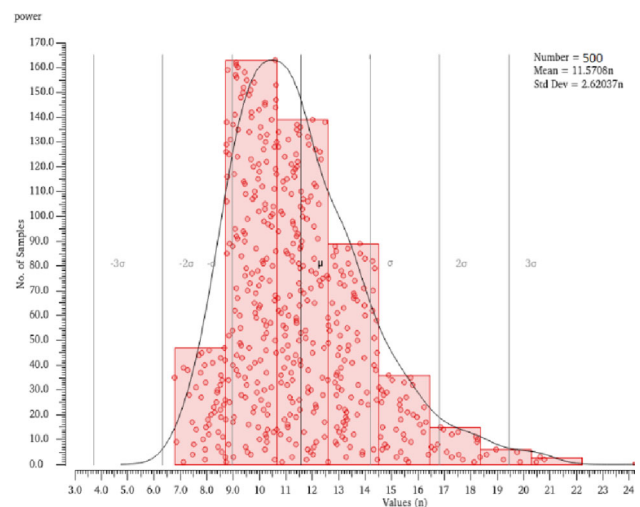
Fig. 15 Leakage power comparison of PLP8T SRAM

Table 3 Leakage power comparison of PLP8T SRAM

| SRAM	Leakage Power (nW)			
	25 °C	50 °C	75 °C	100 °C
Conventional-6 T SRAM	4.87	4.99	5.2	5.4
Chang-10 T SRAM	2.43	2.75	3.24	3.69
HSWA9T SRAM	3.001	3.26	3.48	3.84
ST11T SRAM	1.912	2.23	2.64	2.978
SEDFC 8 T SRM	2.073	2.28	2.76	3.37
PLP8T SRAM	1.908	2.13	2.37	2.679
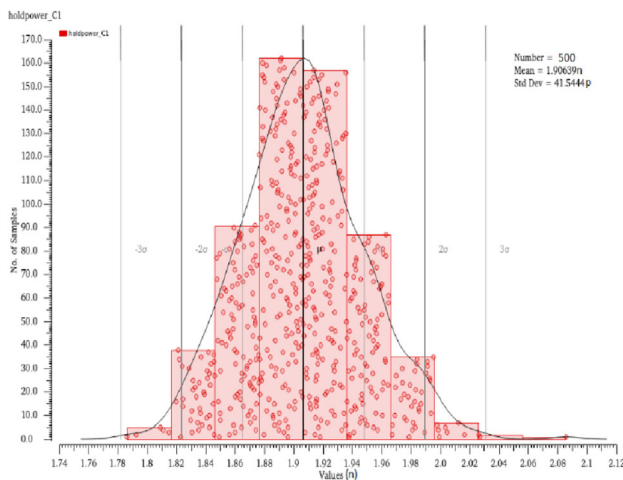
Fig. 16 Leakage power distribution of PLP8T SRAM cell

Montecarlo simulations are performed for 500 samples to observe the standard deviation and mean. The leakage distribution plot is depicted in Fig. 16. The leakage power consumption of PLP8T SRAM is 39.26, 15.37, 17.68, 10.54, and 13.23% less than conventional-6 T, chang10 T, HSWA9T, ST-11 T, and SEDFC8T SRAM cells respectively.

4.7 Cell area

The layout of PLP8T SRAM cell is illustrated in Fig. 17. For area comparison, the layout of conventional-6 T, Chang10T, HSWA9T, ST11T, SEDFC8T, and PPL8T SRAM cells are drawn using 45 nm technology as depicted in Fig. 18.

The area of 6 T SRAM is less because of its easy and compact structure. The PLP8T SRAM shows a 1.45 × overhead in area comparing to conventional-6 T SRAM. But it shows less area when comparing to remaining SRAM cells considered in this work. The other SRAM cells has more area than the PLP8T SRAM because
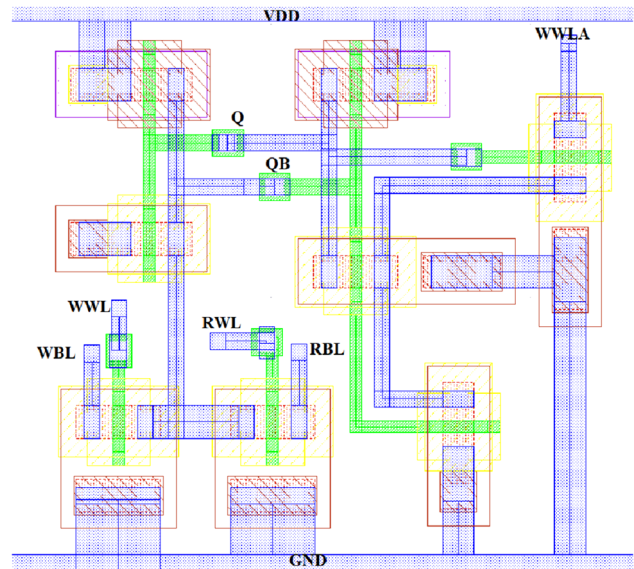
Fig. 17 Layout of PLP8T SRAM cell
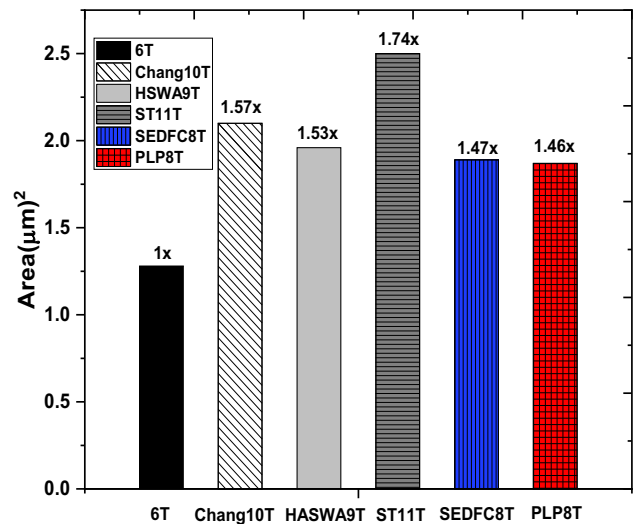
Fig. 18 Area comparison of PLP8T SRAM

of the more transistors, the complexity of the control signals, or the differential structure.

4.8 Electric quality metric

The performance of an SRAM cell can be measured using the electric quality metric (EQM) (Lorenzo and Chaudhury 2016), shown in Eq. (2).

$$EQM = \frac{RSNM \times HSNM \times WSNM}{P_{LEAK} \times T_{RA} \times T_{WA} \times P_{READ} \times P_{WRITE}} \quad (2)$$

where, RSNM Read static noise margin, HSNM = Hold static noise margin, WSNM = Write static noise margin in mV, P_{LEAK} = leakage power, P_{READ} and P_{WRITE} = Read
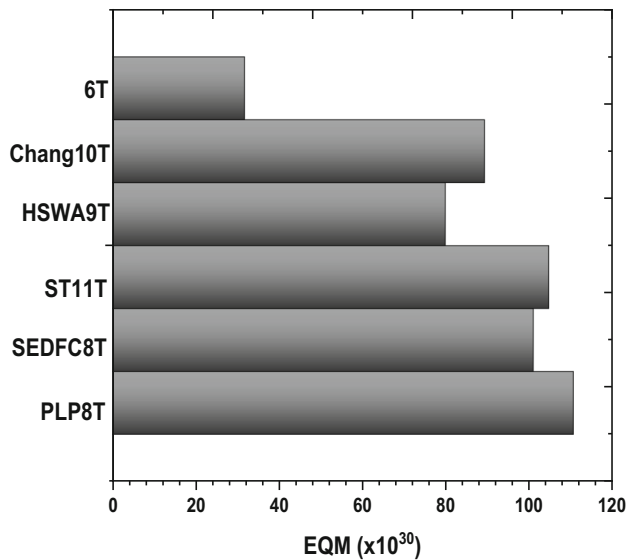
Fig. 19 Electric Quality Metric comparison of PLP8T SRAM

power and Write power in μW, 6. T_{RA} and T_{WA} = Read and write access times in ns.

The EQM comparison of PLP8T SRAM with other SRAM cells considered for this work is illustrated in Fig. 19. The metric of the PLP8T SRAM cell is enhanced by 72.53, 16.47, 18.75, 12.24, and 10.38% comparing to traditional-6 T, Chang10T, HSWA9T, ST-11 T, and SEDFC8T SRAM cells respectively.

5 Conclusion

This paper demonstrated a one-sided schmitt-trigger-based 8 T-SRAM cell, to improve the static noise margin, mitigate the power utilization, and operate SRAM in near-threshold region. The PLP8T SRAM significantly improved read stability, and writing capacity in near-threshold region, and it is analyzed for stability, power, delay, leakage, and area. Read stability was improved by using a cross-connected standard inverter and ST-inverter. Write-ability was improved by using the separate paths for write and read operations. The speed of operation of the cell is enhanced due to reduced read and write access times. The PLP8T SRAM utilizes low power compared to conventional6T, chang10T, HSWA9T, ST11T, and SEDFC8T SRAM cells. The HSNM, RSNM, and WSNM also improved by 1.4 ×, 2.3×, and 1.3× respectively when comparing to conventional6T-SRAM and also, the SNM is enhanced compared to earlier proposed SRAM cells such as chang10 T, HSWA9T, ST11T, and SEDFC8T. The write and read power utilization also lowered by 42.18, and 53.24% comparing to conventional-6 T SRAM respectively and also it is observed that read write power

utilization of PLP8T is less compared to earlier proposed cells considered in this work.

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