Microsystem Technologies (2022) 28:2107–2122
https://doi.org/10.1007/s00542-022-05354-0

TECHNICAL PAPER

Very small size capacitive DMTL phase shifters using a new approach

Omid Reza Afrang[1] · Saeid Afrang[1] · Azrul Azlan Hamzah[2]

Received: 17 December 2021 / Accepted: 18 July 2022 / Published online: 8 August 2022

Abstract
Very small size K_a-band two-bit and K-band six-bit capacitive DMTL phase shifters are designed, calculated and simulated using a new approach. It is done based on information in the return loss diagram. The equations related to the resonance frequencies in the return loss diagram are extracted from the input impedance poles. It is due to the same resonance frequencies of return loss and input impedance diagrams in the linear region. Around these resonance frequencies, it is possible to have a high phase shift and small size together with acceptable return loss. The total proposed two and six-bit phase shifters length are 1.8 mm and 5 mm, respectively. These lengths are the smallest size among the two and six-bit capacitive DMTL phase shifters till now. Moreover, cantilever beam switches with low actuation voltage are used in two-bit phase shifter due to their compatibility with the integrated circuits. The equations-based calculated results are again calculated and simulated in MATLAB and HFSS softwares, respectively.

1 Introduction

Micro-electro-mechanical systems (MEMS) are used in various commercial and industrial applications (Mishra et al. 2019). BioMEMS devices are widely used in medical sciences such as disease detection and drug delivery (Çağlayan et al. 2020; Rotake et al. 2020). Micro-Electro-Mechanical Converters (MEMC) are one of the most utilized MEMS devices. They are designed to convert mechanical energy (or vibrations) into electrical one (Dragunov et al. 2022). One of the interesting fields of MEMS technology is the Radio-Frequency Micro-Electro-Mechanical-Systems (RF MEMS) which offer many advantages to design and fabricate high-performance devices and systems such as filters (Dey and Koul 2020; Entesari and Rebeiz 2005), phase shifters (Daw et al. 2008; McFeetors et al. 2004; Fernandez-Bolanos et al. 2008; Jin et al. 2008; Lacroix et al. 2008; Shafai et al. 2003; Cpw et al. 2007), and other broadband communication applications (Rebeiz 2004). Switches, inductors, and capacitors are the main elements used in RF MEMS-based devices. The phase shifters are one of the RF MEMS-based devices.

Phase shifters in general are mainly used in phased array systems.

Phased array systems, in turn, are widely used in civilian applications such as radars, 5G MIMO for cell phones (Nishimura et al. 2022; Bharadwaj et al. 2020), and communication systems to achieve electronic beam forming and fast beam scanning. The phased array principle is also used in acoustics (Qin et al. 2021), and phased arrays of acoustic transducers are used in medical ultrasound imaging scanners (Elloian 2021; Allevato et al. 2019).The phase shifter design is a major issue in building phased arrays, especially at millimeter-wave frequencies.

Phase shifters based on ferroelectric materials (Flaviis et al. 1997; Kazakov et al. 2010), PIN diodes (Yang and Yang 2011; Trinh et al. 2022), or field-effect transistors switches (Medina-Rull et al. 2020; Maruhashi et al. 1998) have lower switching times as an advantage and higher insertion loss as a defect compared to RF MEMS-based phase shifters. MEMS phase shifters are mainly divided into four types: reflect-line (Li et al. 2019), switched line (Jian et al. 2006; Du et al. 2013a; Huang et al. 2015), loaded line (Lou et al. 2010), and Distributed MEMS Transmission Line (DMTL) (Afrang et al. 2017; Du et al. 2010, 2013b; Puri et al. 2013; Sengar et al. 2013; Dey and Koul 2015; Afrang and Majlis 2008; Chen et al. 2013; Ramli and Arslan 2017). In the DMTL phase shifters, MEMS switches and static or variable capacitors are

✉ Saeid Afrang
s.afrang@urmia.ac.ir

[1] Electrical Engineering Department, Faculty of Electrical and Computer Engineering, Urmia University, Urmia, Iran

[2] Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia, 43600 Bangi, Malaysia

periodically loaded in the Transmission line (T-Line). The phase shift is done by changing the impedance of the structure. The mentioned phase shifters are classified into two types: analog and digital. Barker and Rebeiz (2000) introduced an analog DMTL phase shifter. In this approach, phase changes continuously varied from 0° to 360° using MEMS varactors. In the Digital phase shifters, a discrete set of phase delays are obtained using MEMS switches. In 2000 Borgioli (Liu et al. 2022) introduced a digital phase shifter using MEMS switches together with Metal–Insulator–Metal (MIM) capacitors. Later, Hayden and Rebeiz (2003) and Hayden (2002) introduced Metal-Air-Metal (MAM) capacitors in the digital phase shifter.

Recently, Teymoori et al. (2020) and Chakraborty et al. (2017) have introduced new DMTL phase shifters. The phase shifter introduced by Teymoori et al. is a small size six-bit DMTL phase shifter at 32 GHz. In their proposed structure, the first three bits is used in a cell. The size of the structure is 8.5 mm with 17 switches. Chakraborty et al. have presented a new DMTL phase shifter based on miniature switched capacitors for phased array radar applications. Their proposed structure has a 30-degree phase shift with three similar capacitive switches periodically located on CPW for each unit-cell and 660-μm spacing. Furthermore, the maximum lateral dimension of their structure is 4 mm at k-band (22 GHz).

The main challenge in the MEMS-based phase shifters is the large size of the device compared to the other phase shifters. Hence, designing a small-size phase shifter is required. Results show that the small-size phase shifters have some advantages over bigger ones, such as a much higher part count per wafer and lower loss and cost. Obtaining a large phase shift together with lower spacing per unit cell is the solution. Therefore, we need to have a higher capacitance ratio. Note that a higher capacitance ratio causes higher return loss. This paper proposes two and six-bit capacitive DMTL phase shifters with a significant size reduction and appropriate return loss. Adjusting the quiescent point around the return loss peak solves the problem, and the desired phase shifts together with acceptable return loss are achieved. To prove our goal, we calculate the parameters from the related equations, and then calculate them in MATLAB software to achieve optimum values. Finally, to verify the best values are simulated in the structure-based software (HFSS).

2 Schematic design and calculation of two-bit DMTL phase shifter

Figure 1 indicates the schematic of the proposed unit cell DMTL phase shifter on the High Resistance Silicon (HRS) substrate. The structure in Fig. 1 is a general form of a unit cell used in capacitive DMTL phase shifters. The key point in this research is to present a new approach to this type of phase shifter. The result of the new approach is a large reduction in cell length compared to other similar types. It should be noted that some changes are made to reduce the switching voltage compared to other similar structures. In this way, two cantilever beam switches are used instead of a fixed–fixed beam switch.

Generally, RF-MEMS-based structures are modeled as an electric circuits. The equivalent electrical circuit of the proposed structure in the up and down-state position is shown in Fig. 2a, b, respectively. The components in Fig. 2 are extracted from Fig. 1. The existed components in the structure are inductor, capacitors, and connectors.

Inductor: The only inductor in the structure is due to the conductor line indicated by the "signal line". As it is known in electrical engineering, the equivalent circuit of the metal wire or line is indicated by the inductor. This inductor is named by "sL_t", where "s" means the length of the line.

Capacitors: The capacitors in the structure are made of two metal layers with a dielectric interface layer. There are two types of capacitors in the structure. One type is a parallel plate capacitor, and another is a coplanar capacitor. The metal layers of coplanar type are signal line planes together with ground planes. The dielectric layer of this type on the upside is the air and on the downside is the silicon wafer. This capacitor is named "sC_t," where "s" indicates the length of one side of the related metal layers. There are three types of parallel plate capacitors in the structure. They are named AC capacitor of cantilever switch "$C_{c(AC)}$," DC capacitor of cantilever switch "$C_{c(DC)}$," and static MAM capacitor "$C_s/2$" The capacitor "$C_{c(AC)}$," consists of the overlap area of the metal signal line layer and the end of the metal cantilever. The dielectric layer between these layers is air in this capacitor. This layer is an interface between the mentioned layers. The capacitor "$C_{c(DC)}$," consists of the overlap area of the metal cantilever and metal layer named "Electrode." There are two dielectrics between the mentioned layers. These interfaces are SiO_2 and air. Finally, the capacitor "$C_s/2$" consists of the overlap area between the metal electrode and the fixed–fixed metal beam. The fixed–fixed metal beam is connected to the metal ground layer through a metal interface named "Anchor." The dielectric layer between the mentioned metal layers is air. This layer is an interface between the mentioned layers.

Connectors: The metal anchor layers in the structure act as a connector. The metal connector connects the cantilever beam anchor to the metal electrode.

As shown in Fig. 1, the structure is designed on a Co-Planar Waveguide (CPW) line with two MEMS cantilever

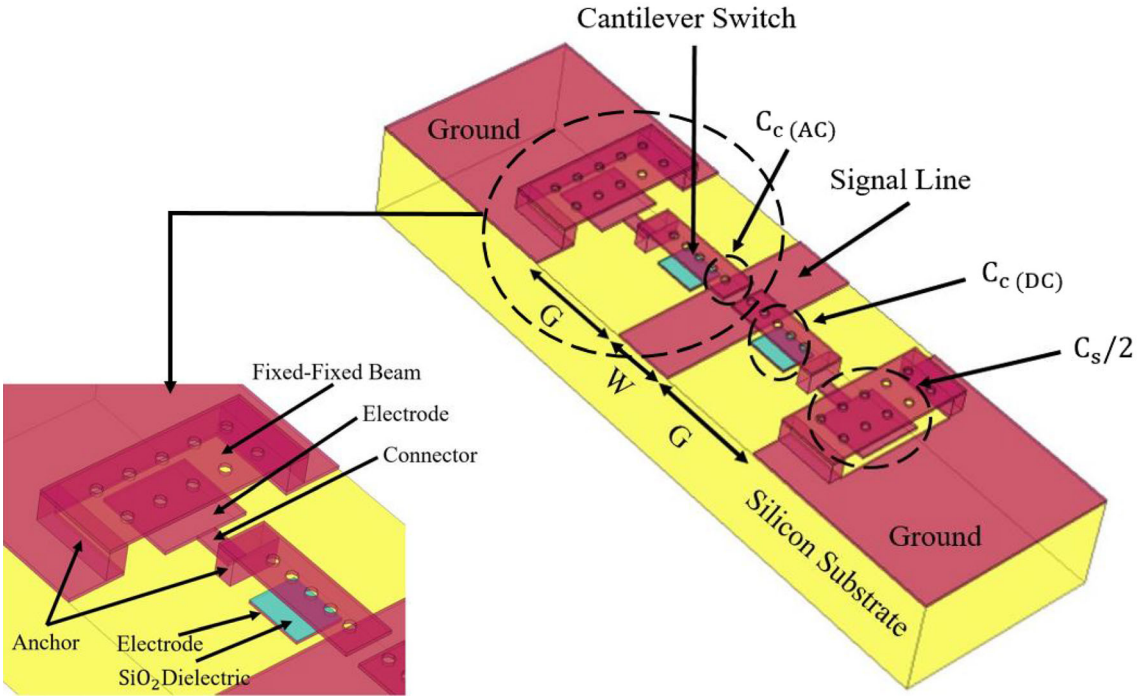

Fig. 1 The schematic of the proposed unit cell of the two-bit DMTL phase shifter

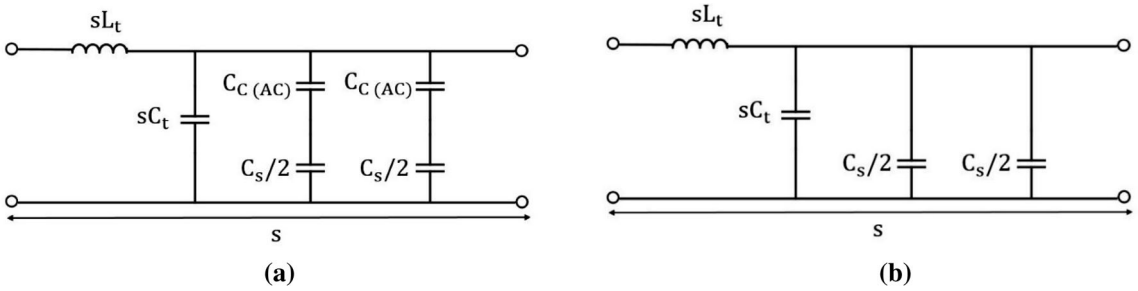

Fig. 2 One cell equivalent circuit of the proposed structure in the **a** up and **b** down-state position

type DC contact shunt switches. These switches are in series with "$C_s/2$" and "$C_{c(AC)}$," capacitors. One electrode is located under each cantilever. When the voltage is applied between these electrodes and corresponding cantilevers, the state of the switches is changed simultaneously.

One cell equivalent circuit of the proposed structure in the up and down-state position is shown in Fig. 2a, b, respectively.

This circuit is only valid for the frequencies in the linear region. In the linear region, the Bragg frequency is around three or more than three times the quiescent frequency. The ohmic and leakage resistance is not considered in the equivalent circuit. The effect of this simplification in the phase shift and return loss is negligible, except, the attenuation of return loss in the resonance points. From the Figures, sL_t and sC_t are the T-line inductance and capacitance of the unit cell, respectively. Each MEMS cantilever switch is in series with $C_s/2$ at one end and an AC capacitor at the other end in the up-state position. The overlap area between the cantilever end and signal line makes the mentioned AC capacitor ($C_{C(AC)}$). When the voltage is applied the free end of the cantilever moves downward and makes DC contact with the signal line. As a result, there is no AC capacitor between the plates in the down-state position.

The proposed structure aims to determine a frequency that satisfies a given phase shift and appropriate return loss with a small size. The computational method achieves the desired frequency by considering the assumptions and thus limitations. The assumption and thus limitation of the model is the working in a special area (around resonance frequency). This area limits the range of quiescent frequency. By calculating, the phase shifter can be adjusted

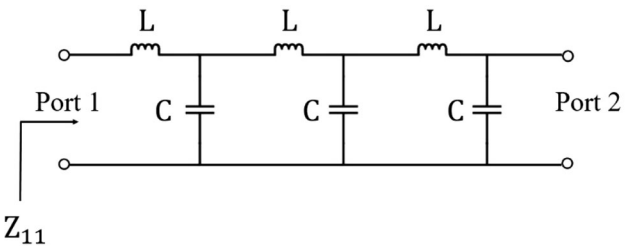

Fig. 3 Equivalent circuit of the three-cell

for the desired frequencies. The device will not work outside the specified frequency. The desired phase shift per cell is obtained from Eq. (1) (Hayden 2002).

$$\Delta\phi = \frac{360 s f Z_0 \sqrt{\varepsilon_{r,eff}}}{c}\left(\frac{1}{Z_d} - \frac{1}{Z_u}\right) \text{Degrees/section} \quad (1)$$

where, s, f, Z_0, $\sqrt{\varepsilon_{r,eff}}$ and c are unit cell length (spacing), quiescent frequency, characteristic impedance effective dielectric constant, and speed of light, respectively. In this equation, Z_u and Z_d are the impedances in the up and down-state position, respectively.

The unit cell length indicated by "s" determines the size of the proposed structure. As is clear from Eq. (1), the phase shift of the structure is size-dependent, and as will be shown in the remaining Eqs. (2)–(27), all other parameters, including return loss, resonance frequencies, Z_u, Z_d, etc. are size-dependent. Our target is to obtain a high phase shift together with a small spacing and reasonable return loss in a unit cell. According to Eq. (1), small spacing decreases the phase shift, therefore to achieve the high phase shift, it is needed to increase the other parameters of Eq. (1), including the relative permittivity of the substrate, characteristic impedance, and impedance difference in the up and down-state position. We assume silicon (ε_r = 11.9) as a substrate because of its high relative permittivity. Considering the substrate type and T-line loss, the characteristic impedance is 70 Ω (Hayden 2002). We also assume 200 μm and 35 GHz, for the spacing, and quiescent frequency, respectively. To achieve high phase shift, a higher impedance difference is needed. As it is known, higher impedance difference results in higher impedance mismatching with respect to port impedance. This high mismatching results in high return loss (higher than −10 dB). This problem appears when we use one cell due to the lack of any resonance peak. Multi-cells result in multi resonance frequencies in the return loss diagram. The return loss around these resonance frequencies is improved. Therefore, it is possible to have a high phase shift with acceptable return loss around the resonance frequencies.

Table 1 Two-bit calculated parameters

Parameter	Value
Static MAM capacitors (C_s)	150.47 fF
Cantilever AC capacitor ($C_{c(AC)}$)	8.68 fF
Per unit length T-line capacitance (C_t)	1.209×10^{-10} F/m
Per unit length T-line inductance (L_t)	5.925×10^{-7} H/m
Unit cell down-state impedance(Z_d)	26.05 Ω
Unit cell up-state impedance(Z_u)	54.6 Ω
Second resonance frequency (f_2)	35 GHz
Third resonance frequency (f_3)	60.6 GHz

For LSB design (90°), we consider different cell states. In the first state, the 90° is done using only one cell. To achieve such a high phase shift by only one cell, the impedance in the down-state position should be very low. This low impedance results in a high return loss. Due to the lack of resonance peak in the return loss diagram, it is impossible to obtain a reasonable return loss. In spite of peak resonance existing in the two-cell return loss diagram, due to very low down-state impedance, the return loss is not acceptable except only in the resonance frequency. To know the return loss behavior of the three-cell, it is needed to calculate the return loss resonance peaks. From Z_{11}, we can find the return loss behavior of the three-cell circuit. The poles of Z_{11} indicate the resonance frequencies in the return loss diagram. Figure 3 shows the equivalent circuit of the three-cell.

The corresponding input impedance $Z_{11}(\omega)$ of Fig. 3 as a function of ω and related poles are as follow:

$$Z_{11}(\omega) = \frac{\omega^6 L^3 C^3 - 5\omega^4 L^2 C^2 + 6\omega^2 LC - 1}{\omega^5 L^2 C^3 - 4\omega^3 LC^2 + 3\omega C}\Omega$$

$$\omega_1 = 0, \omega_2 = \frac{1}{\sqrt{LC}}, \omega_3 = \frac{\sqrt{3}}{\sqrt{LC}} \quad (2)$$

where C represents the equivalent capacitance including sC_t, $C_{C(AC)}$ and C_S in the up/down-state position and L is the T-line inductance. The corresponding frequencies related to the poles ω_2 and ω_3 are f_2 and f_3, respectively. These frequencies are resonance frequencies. The input impedance at these frequencies is high. It means the return

Table 2 The resonance frequencies extracted from the Eq. (9) in the down state position

The extracted frequencies from the poles	Value(GHz)
f_2	18.1
f_3	35
f_4	49.5
f_5	60.6
f_6	67.6

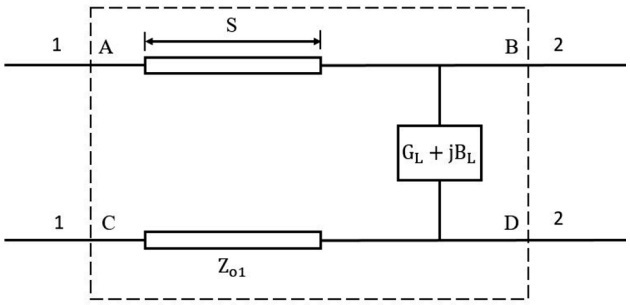

Fig. 4 Equivalent circuit of the three-cell of ABCD parameter of the unit cell

loss of the structure at these frequencies is in the best condition.

According to Eq. (1), the impedance in the down-state position should be very low to obtain a high phase shift considering the small unit cell size. However, low impedance in the down-state position results in high mismatching with respect to port impedance and consequently high return loss. Hence the quiescent frequency of the proposed three-cell in the down state position should be equal to one of the corresponding frequencies related to poles of the Eq. (2) due to better return loss around these poles. The selected resonance frequency should be compared with the Bragg frequency. The Bragg frequency is the frequency at which the line impedance becomes zero and is as follow (Hayden 2002):

$$\omega_{Bragg} = 2\pi f_{Bragg} = \frac{2}{\sqrt{sL_tC_{down}}} \tag{3}$$

As mentioned before, the linear region requires the Bragg frequency very higher than the quiescent frequency. The Bragg frequency is two times f_2 and 1.15 times f_3. It means the resonance frequency "f_3" of the three-cell is around the Bragg frequency. Therefore, it is impossible to consider the "f_3" as a quiescent frequency, and our only choice is the resonance frequency "f_2" as a quiescent frequency in the down state position to have appropriate return loss, as shown in Eq. (4).

$$f_2 = \frac{1}{2\pi\sqrt{sL_tC_{down}}} = \frac{1}{2\pi\sqrt{sL_t(sC_t + C_S)}}\text{GHz} \tag{4}$$

In Eq. (4), L_t and C_t are as follow:

$$L_t = \frac{\sqrt{\varepsilon_{eff}}Z_0}{c}\text{H/m} \tag{5}$$

$$C_t = \frac{\sqrt{\varepsilon_{eff}}}{Z_0 c}\frac{F}{m} \tag{6}$$

The calculation is continued by extracting the capacitance (C_S) from the Eq. (4).

The next step is to find the down-state impedance from Eq. (7) (Hayden 2002):

$$Z_d = \sqrt{\frac{sL_t}{sC_t + C_S}}\Omega \tag{7}$$

Now we can find up-state impedance using Eq. (1). Assuming three cells, $\Delta\phi$ for LSB design in this equation is 30 degrees. The AC capacitance of cantilever $C_{C(AC)}$ is extracted from up-state impedance.

$$Z_u = \sqrt{\frac{sL_t}{sC_t + 2C_{c(AC)}C_s/(2C_{c(AC)} + C_s)}}\Omega \tag{8}$$

The values of two-bit calculated parameters are shown in Table 1

From Table 1, the unit cell up-state impedance is 54.6 Ω, which means the mismatch with respect to port impedance is low. Therefore, the return loss in quiescent frequency will be in the appropriate condition. The extracted C_{down} from Eq. (4) is applied to the related f_3 formula in Eq. (2). The extracted f_3 is 60.6 GHz.

For MSB design (180-degree), we use three-cell LSB as a unit cell. Therefore, six-cell is needed to obtain a 180-degree phase shift. Due to repeating three-cell in 180-degree phase shift, three-cell poles is appeared in the six-cell input impedance. As a result, it is possible to simplify the denominator of the Z_{11}. The corresponding input impedance $Z_{11}(\omega)$ of six-cell as a function of ω and related poles are as follow:

$$Z_{11}(\omega) = \frac{\omega^{12}L^6c^6 - 11\omega^{10}L^5c^5 + 45\omega^8L^4c^4 - 84\omega^6L^3c^3 + 70\omega^4L^2c^2 - 21\omega^2LC + 1}{(\omega^5L^2C^3 - 4\omega^3LC^2 + 3\omega C)(\omega^6L^3C^3 - 6\omega^4L^2C^2 + 9\omega^2LC - 2)}\Omega \tag{9}$$

$$\omega_1 = 0, \omega_2 = \frac{\sqrt{2-\sqrt{3}}}{\sqrt{LC}}, \omega_3 = \frac{1}{\sqrt{LC}}, \omega_4 = \frac{\sqrt{2}}{\sqrt{LC}}, \omega_5 = \frac{\sqrt{3}}{\sqrt{LC}}, \omega_6 = \frac{\sqrt{2+\sqrt{3}}}{\sqrt{LC}}$$

The corresponding resonance frequencies f_3 and f_5 in the six-cell are the same as the resonance frequencies f_2 and f_3 in the three-cell. The choice in the six-cell in the

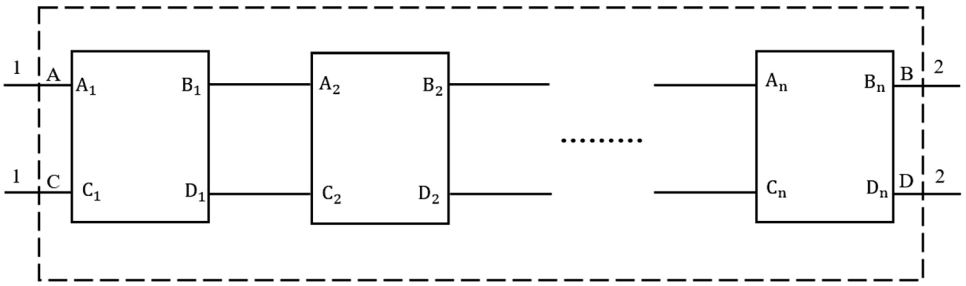

Fig. 5 Proposed multi-cell structure

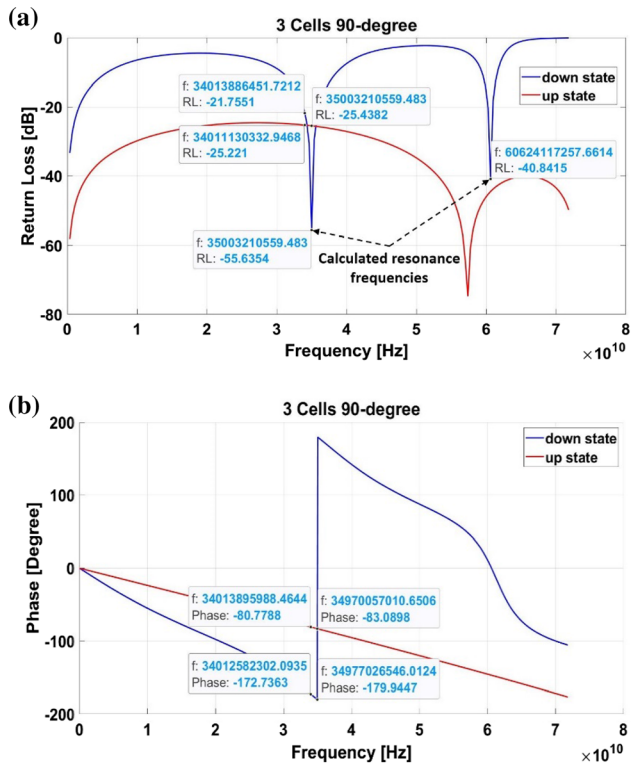

Fig. 6 Calculated results of **a** return loss and **b** phase of the 90° in the up and down-state position

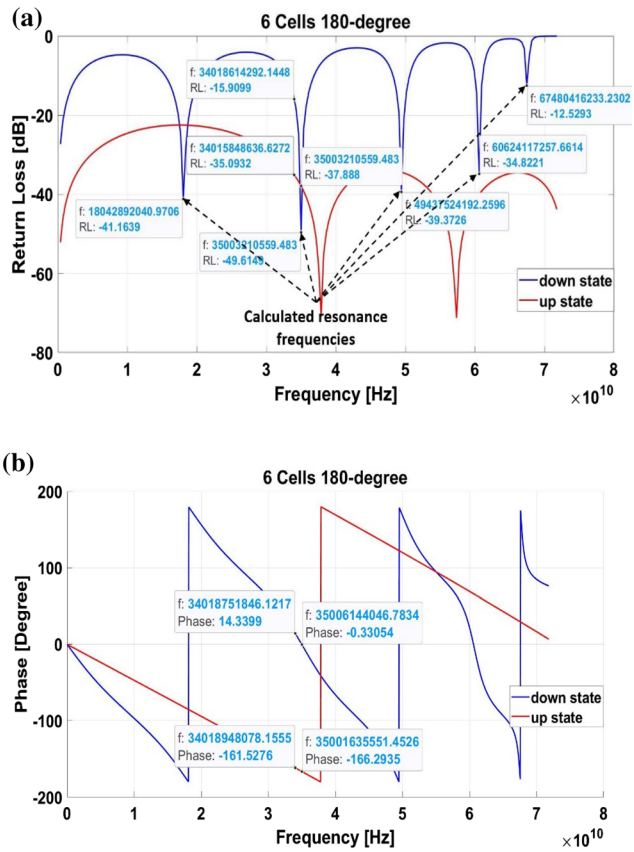

Fig. 7 Calculated results of **a** return loss and **b** phase of the 180° in the up and down-state position

down-state position is the resonance frequency f_3 in the input impedance equation as the quiescent frequency.

The resonance frequencies of Eq. (9) in the down-state position are also calculated considering the unit cell inductance and capacitance in Table 1. The calculated results are shown in Table 2.

The final step for achieving a two-bit DMTL phase shifter is the combining the LSB and MSB. In the proposed two-bit DMTL phase shifter, three-cell as a unit cell is repeated three times. As a result, all three-cell poles are found in nine-cell poles. One of these poles in the down-sate position is the desired pole as the quiescent frequency.

The calculated parameters from the Eqs. (1)–(9) are verified using ABCD matrix-based scattering parameters in MATLAB software. The inputs of these equations are the calculated parameters (inductance and capacitances) shown in Table 1.

To derive unit cell ABCD parameters, the equivalent circuit in Fig. 4 is used. In this circuit, Z_{o1}, is the characteristic impedance. The length of the lossy T-line determines the periodic separation. The structure is placed over this line. The term $(G_L + jB_L)$ is the shunt load.

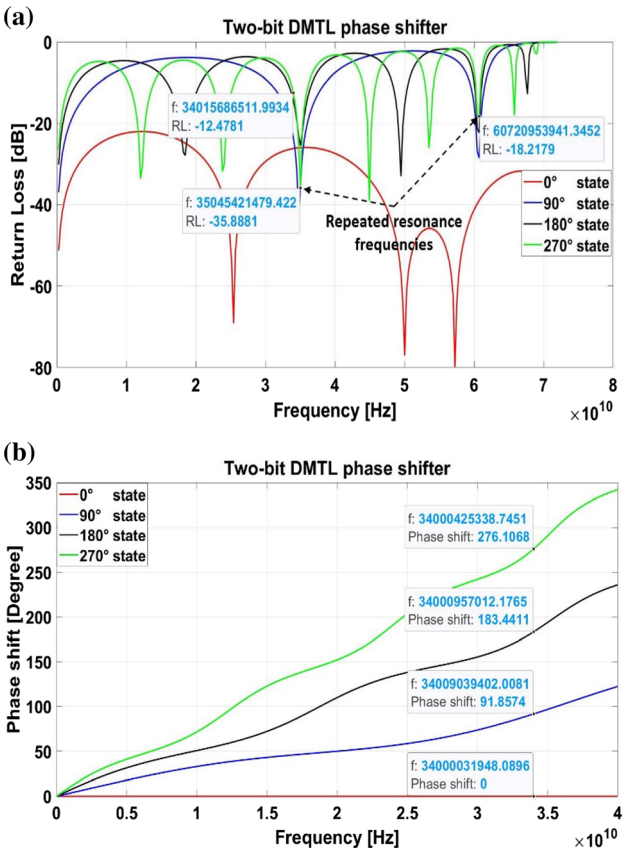

Fig. 8 Calculated results of **a** return loss and **b** phase shift of the four-state two-bit DMTL phase shifter

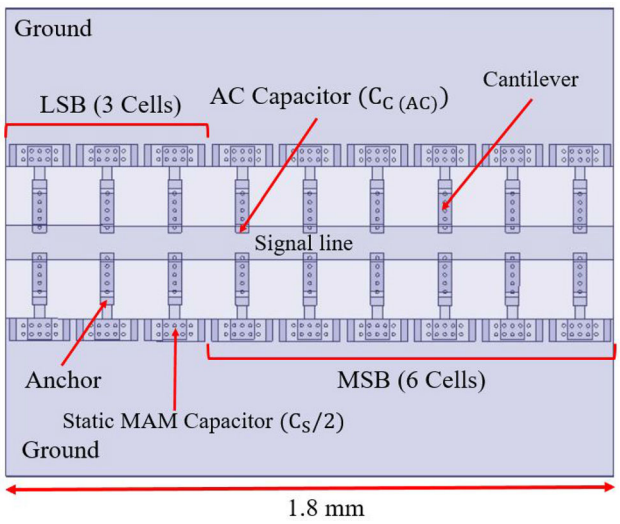

Fig. 9 The schematic of the top view of the two-bit DMTL phase shifter

The ABCD matrix of the lossy T-line is given by Pozar (2011):

$$\begin{bmatrix} A_{T-line} & B_{T-line} \\ C_{T-line} & D_{T-line} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma.s) & Z_{o1}.\sinh(\gamma.s) \\ Y_{o1}.\sinh(\gamma.s) & \cosh(\gamma.s) \end{bmatrix} \tag{10}$$

$$\gamma = \alpha + j\beta \tag{11}$$

where, γ, α and β are the complex propagation constant, attenuation and the phase constant of the T-line respectively. α, β and phase velocity (v_p) are as follow:

$$\alpha = \frac{sR_t}{2Z_{01}} \tag{12}$$

$$\beta = \frac{\omega}{v_p} \tag{13}$$

$$v_p = \frac{1}{s\sqrt{L_tC_t}} \tag{14}$$

The ABCD matrix of the shunt load is given by:

$$\begin{bmatrix} A_L & B_L \\ C_L & D_L \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ G_L + jB_L & 1 \end{bmatrix} \tag{15}$$

As mentioned before, the ohmic and leakage resistance is not considered in this research. Hence, $\alpha = G_L = 0$ is considered. The susceptance of the shunt load is as follow:

$$B_L = \omega.C_L \tag{16}$$

The ABCD matrix of the unit cell is obtained by multiplying the matrices Eqs. (10) and (15).

The proposed structure includes multi cells, is shown in Fig. 5.

The overall ABCD matrix of the structure is as follow:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \times \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \times \ldots . \times \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} \tag{17}$$

In Eq. (17), the n equals 3, 6, and 9 correspond to LSB (90-degree), MSB (180-degree), and two-bit DMTL phase shifter design, respectively.

S_{11} and S_{21} in terms of ABCD parameters of LSB, MSB, and two-bit DMTL phase shifter connected to a line with port impedance ($Z_0 = 50\Omega$) are as follow (Pozar 2011):

$$S_{11} = \frac{A + B.Y_0 - C.Z_0 - D}{A + B.Y_0 + C.Z_0 + D} \tag{18}$$

$$S_{21} = \frac{2}{A + B.Y_0 + C.Z_0 + D} \tag{19}$$

Finally, the 3-cell 90-degree, 6-cell 180-degree, and two-bit return loss and phase shift are also obtained using Eqs. (20) and (21), respectively.

$$RL = 20\log(S_{11})dB \tag{20}$$

Table 3 Dimensions and material properties

Parameter	Value
Silicon thickness and resistance	500 μm, 3000 Ω cm
G/W/G (μm)	175/100/175
Static MAM capacitor ($C_s/2$) gap and its electrode width and length (μm)	1, 60 × 72
Cantilever AC capacitor ($C_{c(AC)}$) gap and its electrode width and length (μm)	1, 20 × 40
Cantilever beam length, width and thickness (μm)	130 × 40, 0.8
Young modulus of aluminum (GPa)	68.85

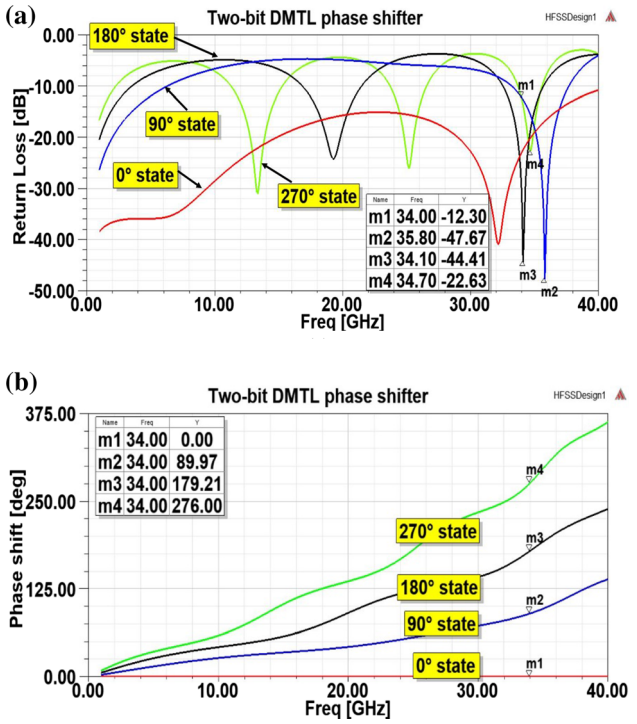

Fig. 10 Simulated results of **a** return loss and **b** phase shift of the four-states two-bit DMTL phase shifter

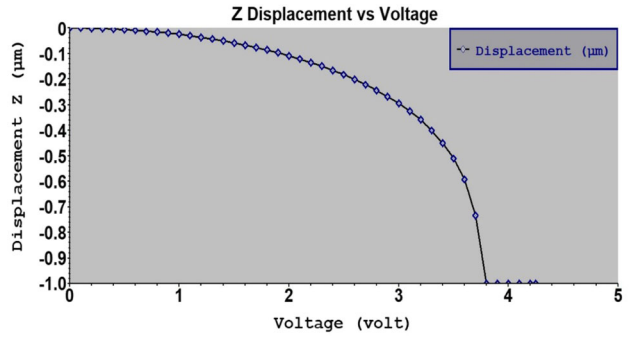

Fig. 11 Simulation result of cantilever beam displacement versus voltage

$$\Delta\varphi = \text{phase}(S_{21})|_{\text{down state}} - \text{phase}(S_{21})|_{\text{up state}} \text{Degrees} \quad (21)$$

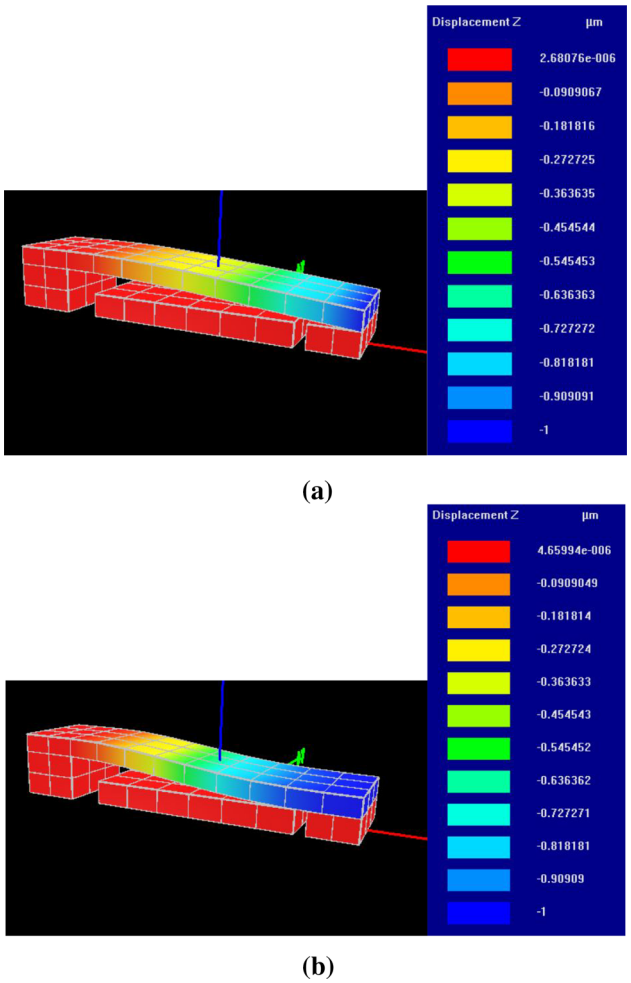

Fig. 12 Switch in the down state position **a** imperfect **b** perfect contact

The MATLAB results in Fig. 6a, b show return loss and phase of the three-cell (90-degree) in the up and down-state position, respectively. Figure 6a verifies the calculated resonance frequencies of Table 1.

As it is seen, the phase shift at 35 GHz is slightly higher than the calculated results. It is due to the non-linear behavior of the structure. The linearity of the structure is related to the amount of Bragg frequency (Hayden 2002). Considering Eqs. (3), and (4) in the proposed structure, the Bragg frequency is two times the resonance frequency. The

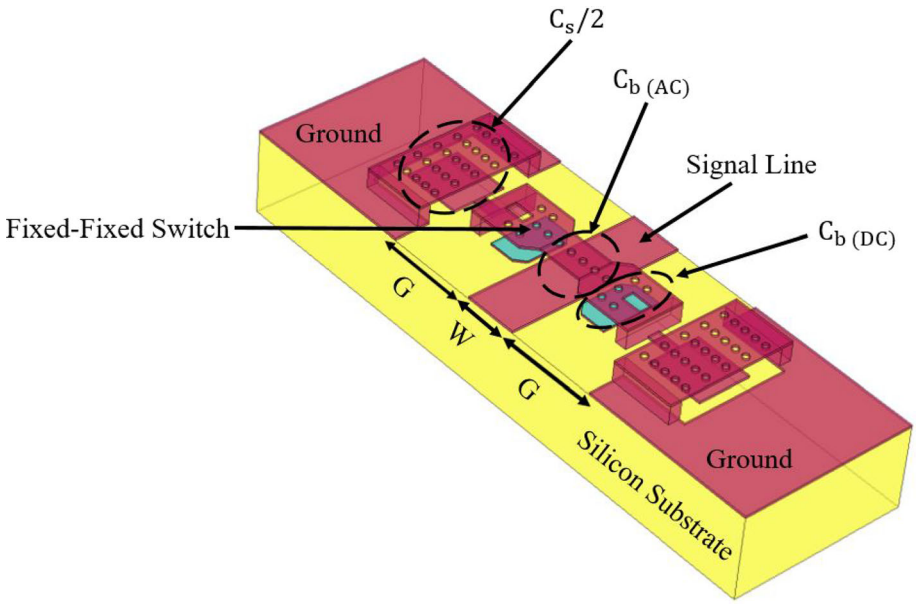

Fig. 13 The schematic of the proposed unit cell of the six-bit DMTL phase shifter

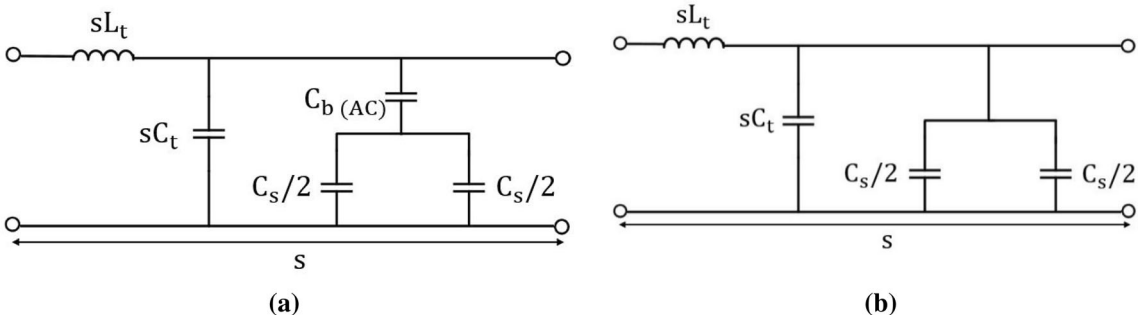

Fig. 14 One cell equivalent circuit of the proposed structure in the **a** up and **b** down-state position

exact linear condition occurs when the Bragg frequency is around three or more than three times the resonance frequency.

To be more linear, we move the quiescent point slightly to the lower frequencies. In the three-cell structure, the linearity and consequently proper phase shift occur in the 34 GHz. In Fig. 6a, b return loss in the up and down-state position and phase shift at 34 GHz are −25.22 dB, −21.75 dB, and 91.96°, respectively.

We continue this procedure to six-cell (180°). The MATLAB results in Fig. 7a, b show the return loss and phase in the up and down-state position, respectively. Figure 7a verifies the calculated resonance frequencies of Table 2.

In Fig. 7a, b return loss in the up and down-state position and phase shift at 34 GHz are −35.09 dB, −15.90 dB, and 184.15°, respectively.

Finally, nine-cell two-bit phase shifter is calculated in MATLAB software. The nine-cell total size by considering the unit cell size (200 μm) is 1.8 mm. It is the smallest size in the two-bit DMTL phase shifters. Figure 8a, b show the return loss and phase shift of the 4-state (i.e., 0°, 90°, 180°, and 270°), respectively. According to Fig. 8a, the two resonance frequencies of the three-cell as a unit cell are repeated in the two-bit phase shifter with exact values in 270° and slightly different in 90° and 180° states. In the 270° all cells are in the same condition (all in down-state position) and are matched with three-cell as a unit cell. In states 90° and 180°, some cells are in the up-state position. These cells are different from the mentioned three-cell as a unit cell. As a result, the resonance frequency is moved to the left or right. In the Figures, the worst return loss is -12.47 dB, and phase shift at 34 GHz for 4-state (i.e., 0°, 90°, 180°, and 270°) are 0°, 91.85°, 183.44°, and 276.1°, respectively.

Table 4 Calculated parameters for the unit cell of each bit of the six-bit DMTL phase shifter

Bit	180°	90°	45°	22.5°	11.25°	5.625°
Number of cells	8	4	6	5	1	1
Static MAM capacitors (C_s fF)	174	174	60	39	63.5	44.5
MEMS Fixed–Fixed switch AC capacitor ($C_{b(AC)}$ fF)	31.5	31.5	31.5	34	10.5	30.5
Unit cell down-state impedance($Z_d\Omega$)	24.5	24.5	37.5	43	36.5	41.5
Unit cell up-state impedance($Z_u\Omega$)	48	48	51.5	53	60	53

3 Two-bit DMTL phase shifter simulation results

The final step is reconfirming calculated results using a Finite Element Method (FEM) named by HFSS software. This step uses the parameters extracted from the Eqs. (1)–(9). The proposed structure is simulated using HFSS software to verify the calculated results. Figure 9 shows the schematic of the top view of the two-bit phase shifter. The cells are the same as in Fig. 1.

The dimensions and material properties are shown in Table 3:

There are some considerations in modeling the MAM capacitors. The MAM capacitor is located inside the cut ground plane. The cut ground plane adds capacitance to the MAM capacitor (Hayden 2002). Another parameter that affects the MAM capacitor is the fringing field. By considering these two items, the MAM capacitor is modeled. The simulation is also done by considering the fabrication process condition, including perforated capacitors and cantilever beams, and also the same MAM capacitor and cantilever beam air gaps.

Figure 10a, b show the return loss in the up and down-state position and phase shift at 34 GHz for 4-state (i.e., 0°, 90°, 180°, and 270°), respectively. From the Figures, the worst return loss is −12.30 dB, and phase shift at 34 GHz for 4-state (i.e.,0°, 90°, 180°, and 270°) are 0°, 89.97°, 179.21°, and 276°, respectively.

4 Electromechanical considerations

Until now, all the switches used in the DMTL phase shifters are based on fixed–fixed type beams. The spring constant of these beams is high. High spring constant results in high switching voltage. The residual stress in the fixed–fixed type beam also increases the switching voltage. The cantilever beam, due to its low spring constant and zero residual stress, is the appropriate candidate to use in the integrated circuits. The conventional MEMS switch used in DMTL phase shifters is a capacitive fixed–fixed beam-type switch in each cell. In this research, each cell consists of two cantilever-type DC contact switches. The material and geometrical parameters of the switch are indicated in Table 3.

Figure 11 shows the simulation result of cantilever beam displacement versus voltage using IntelliSuite software. From this Figure, the first contact voltage is 3.8 V. At this voltage, the cantilever end edge touches the signal line, and contact is imperfect. Figure 12a shows mentioned condition. The desired and perfect contact is between the cantilever AC capacitor plates, as shown in Fig. 12b. In such condition, the applied voltage is 4.25 V.

5 Schematic design and calculation of six-bit DMTL phase shifter

Figure 13 shows the schematic of the unit cell structure of the six-bit DMTL phase shifter. It is the modified structure of the unit cell indicated in Fig. 1. As seen from the Figure, the two cantilever beam switches are changed to one fixed–fixed DC contact shunt switch. One cell equivalent circuit of the proposed structure in the up and down-state position is shown in Fig. 14a, b, respectively.

The used design method in a two-bit phase shifter is again used in the design of the six-bit DMTL phase shifter. The small size is the main goal of the paper. As mentioned before, around the resonance frequency, it is possible to have a high phase shift and small size together with acceptable return loss. This procedure is applied to 45°, 90°, and 180° bits in the six-bit phase shifter design.

To change the quiescent frequency, it is needed to change the resonance frequency. The resonance frequency is changed by the capacitance load and the number and length of the cells. In the two-bit design and for 90°, the minimum cells with reasonable return loss and small size is three cells at 35 GHz. If one cell is added, the first resonance frequency is decreased. In the design of the six-bit DMTL phase shifter, it is assumed 200 μm and 25 GHz, for the spacing and quiescent frequency, respectively. Therefore, in 90°, four cells are considered.

The corresponding input impedance $Z_{11}(\omega)$ of four cells as a function of ω and related poles are as follow:

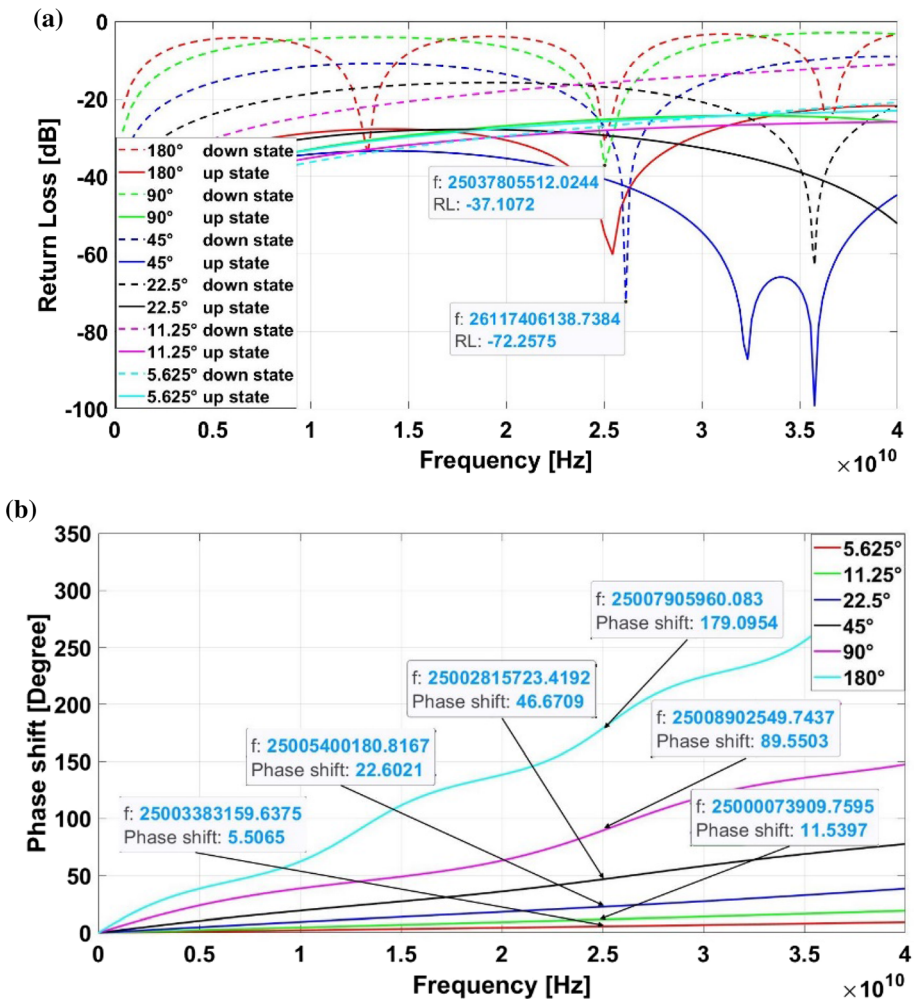

Fig. 15 Calculated results of **a** return loss in the up and down-state position and **b** phase shift of six independent bits

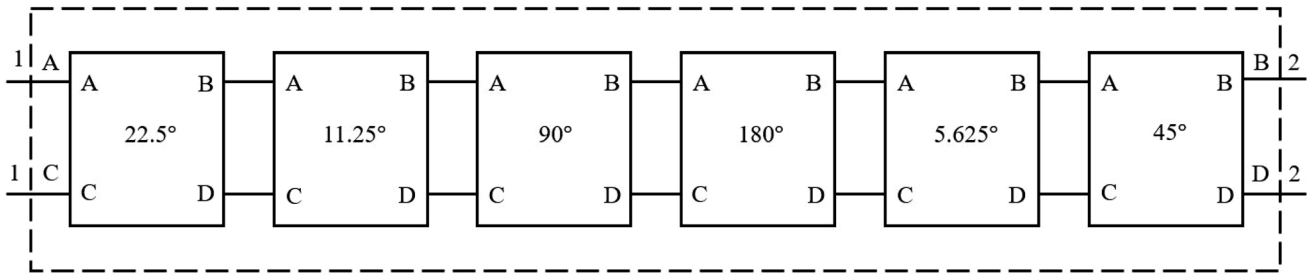

Fig. 16 Proposed model of the six-bit DMTL phase shifter

$$Z_{11}(\omega) = \frac{\omega^8 L^4 C^4 - 7\omega^6 L^3 C^3 + 15\omega^4 L^2 C^2 - 10\omega^2 LC + 1}{\omega^7 L^3 C^4 - 6\omega^5 L^2 C^3 + 10\omega^3 LC^2 - 4\omega C}\Omega \quad (22)$$

$$\omega_1 = 0, \omega_2 = \frac{\sqrt{2-\sqrt{2}}}{\sqrt{LC}}, \omega_3 = \frac{\sqrt{2}}{\sqrt{LC}}, \omega_4 = \frac{\sqrt{2+\sqrt{2}}}{\sqrt{LC}}$$

Same as the design procedure of 90° bit in two-bit, due to the high mismatch with respect to port impedance in the down-sate position, the quiescent frequency in this state should be equal to one of the resonance frequencies in the Eq. (22). These frequencies should be compared with the Bragg frequency. From Eq. (3) the Bragg frequency is 2.6 times the frequency f_2, 1.4 times the frequency f_3 and 1.08 times the frequency f_4. The resonance frequencies f_3 and f_4 are around the Bragg frequency. Therefore it is impossible to consider them as the desired quiescent frequency, and our only choice is the frequency f_2.

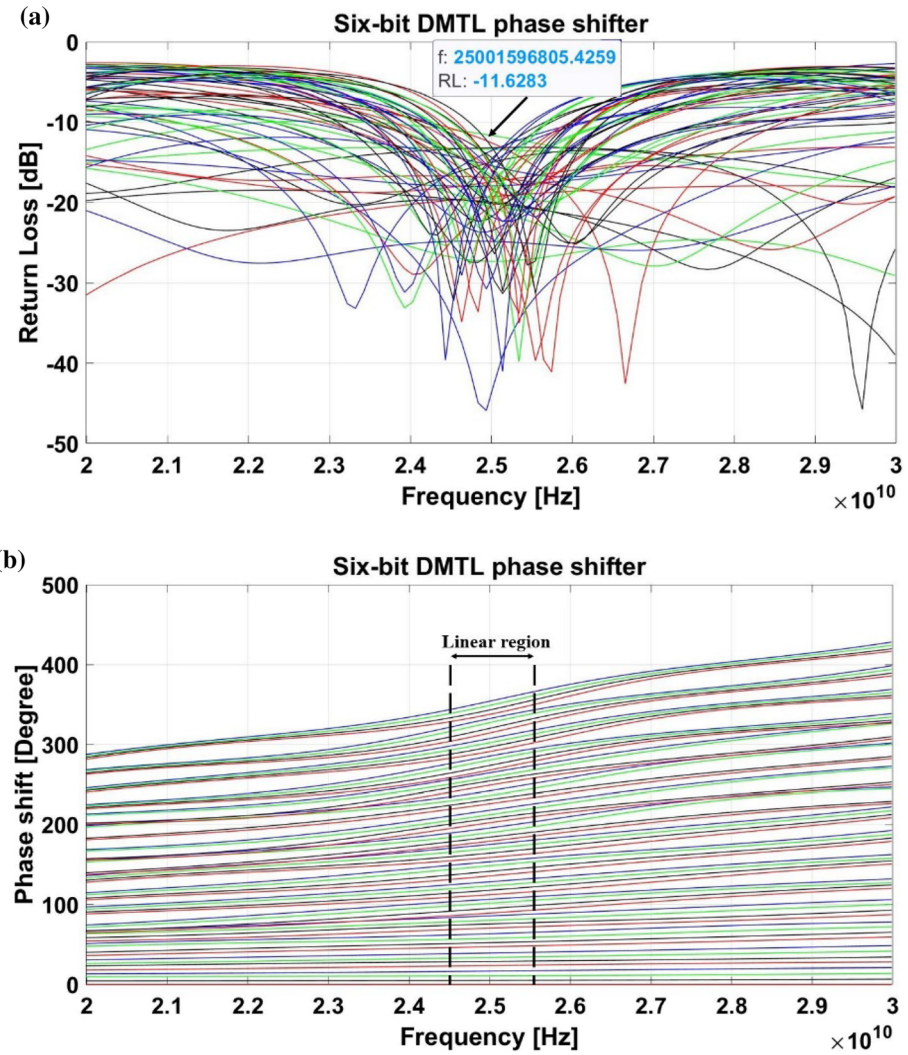

Fig. 17 Calculated results of **a** the return loss and **b** phase shift of all 64 states

$$f_2 = \frac{\sqrt{2-\sqrt{2}}}{2\pi\sqrt{sL_tC_{down}}} = \frac{\sqrt{2-\sqrt{2}}}{2\pi\sqrt{sL_t(sC_t+C_S)}}\text{GHz} \quad (23)$$

As mentioned before, the two cantilever beam switches are changed to one fixed–fixed DC contact shunt switch. Therefore, the equivalent circuit and impedance in the up-state position are changed. Equation (24) shows the up-state impedance of the unit cell of the proposed six-bit DMTL phase shifter.

$$Z_u = \sqrt{\frac{sL_t}{sC_t + \frac{C_{b(AC)}C_s}{C_{b(AC)}+C_s}}}\Omega \quad (24)$$

The Eqs. (1), (5)–(7), and (22)–(24), are used to extract the parameters of 90° bit. The values of calculated parameters are shown in Table 4.

In 180° design, four-cell (90°) is as a unit cell. Therefore, eight-cell is needed to obtain a 180° phase shift. Due to repeating four-cell in 180° phase shift, four-cell poles of Eq. (22) appear in the eight-cell input impedance poles.

In the 45° bit design, six cells are needed to drag the second pole or first resonance frequency to around the desired frequency (25 GHz). The corresponding input impedance $Z_{11}(\omega)$ of six cells as a function of ω and related poles are the same as Eq. (9). The Eqs. (1), (5)–(7), (9) and (24) are used to extract the parameters. The values of calculated parameters are shown in Table 4.

The three remaining bits require a small phase shift per cell. The return loss of such a small phase shift per cell is acceptable. Therefore, there is no need to have resonance peaks around the desired frequency. The design procedure and equations of the three remaining bits are as follow (Hayden 2002):

$$\Gamma_{in} = 10^{RL_{max}/20} \quad (25)$$

$$Z_L = 50\sqrt{\frac{1\pm\Gamma_{in}}{1\mp\Gamma_{in}}}\Omega \quad (26)$$

AC capacitor width and length (μm)	45×100	45×100	45×100	48×100	30×45	42×100

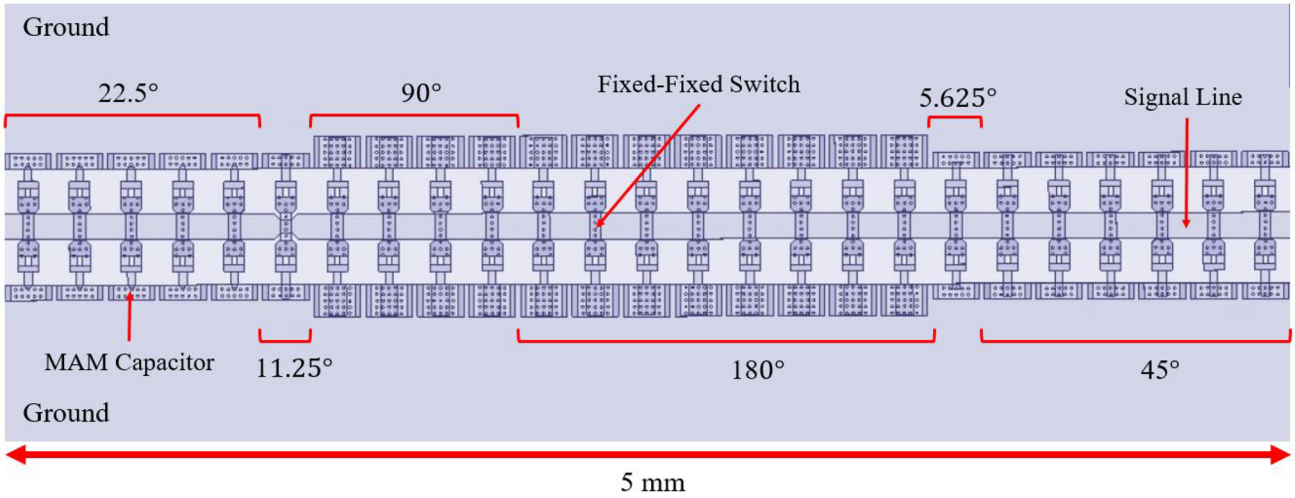

Fig. 18 The schematic of the top view of the six-bit DMTL phase shifter

Table 5 Capacitors plate area of six-bit phase shifter

Bit	180°	90°	45°	22.5°	11.25°	5.625°
Static capacitor width and length (μm)	68 × 120	68 × 120	30 × 50	10 × 20	30 × 53	20 × 30
AC capacitor width and length (μm)	45 × 100	45 × 100	45 × 100	48 × 100	30 × 45	42 × 100

The Eqs. (25) and (26) indicate the relation between load impedance and return loss.

The design starts by considering the appropriate return loss of the cells in the up and down-state position. The return loss is directly proportional to the phase shift of the unit cell. The return loss of −25 dB is possible due to the small phase shift of LSB in the up-state position. The corresponding up-state impedance from Eqs. (25) and (26) is 53 Ω. Then, the down state impedance is extracted from Eq. (1). This impedance is 41.5Ω. Therefore, the corresponding down state return loss from Eq. (25) is −15 dB. Now, it is possible, calculate the C_S and $C_{b(AC)}$ using Eqs. (7) and (24). These capacitor capacitances are 44.5 fF and, 30.5 fF respectively. This procedure is used to calculate, up state impedance, down-state impedance, $C_{b(AC)}$, and C_S, respectively, for 11.25° and 22.5° bits. The calculated results are shown in Table 4. The phase shift of the 11.25° bit is designed the same as the 5.625° bit using only one cell. Due to the higher phase shift, the corresponding return loss of 11.25° bit is higher than LSB. Therefore, the return loss of −15 dB is considered.

It is not possible to consider only one cell to 22.5° bit due to its high return loss. Therefore it is needed to use more cells. There are two options considering the desired return loss. One option is creating resonance peak around the desired frequency. The second option is dividing the 22.5° to small phase shift using more cells. As it is known, a small phase shift per cell improves the return loss. In the design, the second choice is used, and using five cells with 4.5° for each cell; it is possible to have −25 dB return loss. If the first option is used, it requires more than five cells to drag the resonance peak around the desired resonance frequency.

In the next step, same as the two-bit, and to verify, the calculated parameters from Table 4 are applied to Eqs. (10)–(21) and (27) related to ABCD matrix-based scattering parameters in MATLAB software.

The MATLAB results in Fig. 15a, b shows return loss in the up and down-state position and phase shift of the six

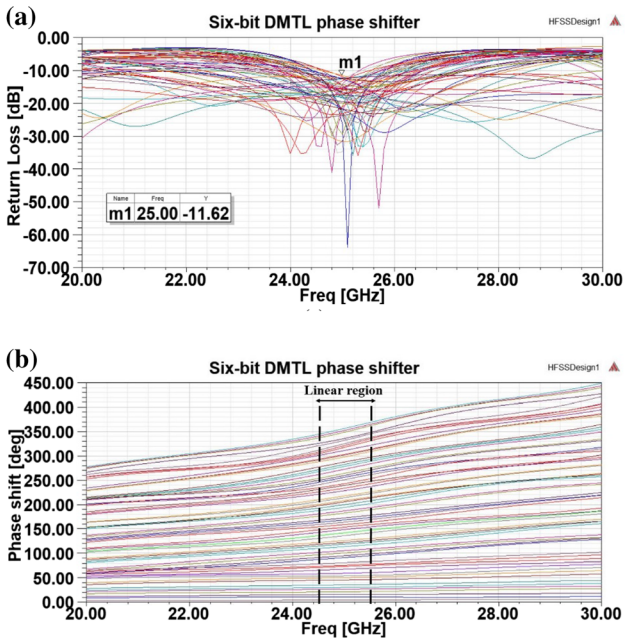

Fig. 19 Simulated results of **a** return loss and **b** phase shift of the 64 states of the six-bit DMTL phase shifter at 25 GHz

main bits, respectively. Each bit in these Figures is independent and separate from the rest of the bits.

The next step is the connecting the six independent bits to achieve the six-bit phase shifter. Figure 16 shows the complete model of the proposed six-bit DMTL phase shifter. As is seen in Fig. 16, the extracted ABCD matrices of six independent bits in Eq. (17) are multiplied to achieve the six-bit DMTL phase shifter.

Equation (27) is used to derive the ABCD parameters of the proposed six-bit DMTL phase shifter.

$$\begin{bmatrix} A_{6-bit} & B_{6-bit} \\ C_{6-bit} & D_{6-bit} \end{bmatrix} = \begin{bmatrix} A_{22.5^\circ} & B_{22.5^\circ} \\ C_{22.5^\circ} & D_{22.5^\circ} \end{bmatrix} \times \begin{bmatrix} A_{11.25^\circ} & B_{11.25^\circ} \\ C_{11.25^\circ} & D_{11.25^\circ} \end{bmatrix} \times \begin{bmatrix} A_{90^\circ} & B_{90^\circ} \\ C_{90^\circ} & D_{90^\circ} \end{bmatrix} \times \begin{bmatrix} A_{180^\circ} & B_{180^\circ} \\ C_{180^\circ} & D_{180^\circ} \end{bmatrix} \times \begin{bmatrix} A_{5.625^\circ} & B_{5.625^\circ} \\ C_{5.625^\circ} & D_{5.625^\circ} \end{bmatrix} \times \begin{bmatrix} A_{45^\circ} & B_{45^\circ} \\ C_{45^\circ} & D_{45^\circ} \end{bmatrix} \quad (27)$$

The total 25 cells size considering the unit cell size of 200 μm is 5 mm. It is the smallest size in the six-bit DMTL phase shifters. Figure 17a, b show the return loss and phase shift for all 64 states, respectively. As it is seen from Fig. 17a, b, due to acceptable return loss between the frequencies 24.5 GHz and 25.5 GHz, the phase shift is approximately linear. From Fig. 17a the worst return loss is −11.62 dB.

The final step is the reconfirming calculated results using FEM by HFSS software. This step uses the calculated parameters from Table 4. It is done in the next section.

6 Six-bit DMTL phase shifter simulation results

The proposed structure is simulated using HFSS software to verify the calculated results. Figure 18 shows the schematic of the top view of the six-bit DMTL phase shifter. The CPW line dimension and silicon thickness and resistance are the same as the two-bit structure. The capacitors

Table 6 Comparison of the present work with the state-of-the-art RF MEMS based phase shifters

References	Teymoori et al. (2020)	Afrang et al. (2017)	Du et al. (2010)[a]	Hayden and Rebeiz (2003)[a]	Ramli et al. (2017)	Chakraborty et al. (2017)[a]	This work (two-bit; six-bit)
Number of bits	6	6	5	2	2	1	2; 6
Number of cells	17	32	31	21	41	6	9; 25
Unit cell size (μm)	500	400	660	400	1850	660	200; 200
Operating Freq. (GHz)	32	30	10	37.7	2.45	22	34; 25
Max return loss (dB)	−10.8	−11	−13.6	−11.5	< −10	−25	−12.3; −11.62
Actuation voltage (V)	3.2–3.6–6.6	3.4–6.8	30.1	20	9.68	14.6	4.25; 6.75
Total length (mm)	8.5	12.8	20.46	8.4	28.35	4	1.8; 5
Substrate	Glass	Glass	HRS	Glass	HRS	Quartz	HRS

[a]Measurement results

plate area of all bits is shown in Table 5. The air gap of all capacitors is the same and equal to 1.5 μm. Figure 19a, b show the return loss and phase shift at 25 GHz for all 64-state, respectively. From the figures, the worst return loss is −11.62 dB.

7 Comparison

Table 6 presents a comparison between the state-of-the-art RF MEMS-based DMTL phase shifters and the current study. It is evident from the table that the proposed two and six-bit design results in better total length, and also two-bit design requires lower actuation voltage as compared to previously published research works. Reduction in the lateral dimension of two and six-bit phase shifter has minimized substrate area wastage which generates cost-effective output. Based on Table 6 and in comparison with our proposed phase shifter, the nearest six-bit phase shifter length is 8.5 mm. The actuation mechanism of the mentioned phase shifter is based on the unit cell level. It means that the number of input control is proportional to the number of cells. It should be noted that the actuation mechanism of the proposed phase shifter is based on bit-level actuation as it is in the conventional phase shifters.

8 Conclusion

A very small size K_a-band two-bit and K-band six-bit DMTL phase shifter was introduced in this research work. The improvement in size became possible by analyzing the return loss behavior in all frequencies. The calculated results showed that it is possible to have a small size, high phase shift, and reasonable return loss of unit cell for the frequencies near the resonance frequencies. The extracted two-bit and six-bit phase shifters lengths are 1.8 mm and 5 mm, respectively. These lengths are the smallest size among two-bit and six-bit DMTL phase shifters. The worst return loss in the two-bit and six-bit is −12.3 dB and −11.62 dB, respectively. The cantilever beam used in the two-bit phase shifter switches decreased the perfect contact voltage to 4.25 V. To verify, calculated results were then calculated and simulated using MATLAB and HFSS software, respectively.

References

Afrang S, Majlis BY (2008) Distributed transmission line phase shifter using MEMS switches and inductors. Microsyst Technol 14(8):1173–1183. https://doi.org/10.1007/s00542-008-0637-9

Afrang S, Samandari K, Rezazadeh G (2017) A small size Ka band six-bit DMTL phase shifter using new design of MEMS switch. Microsyst Technol 23(6):1853–1866. https://doi.org/10.1007/s00542-016-2987-z

Allevato G, Hinrichs J, Großkurth D, Rutsch M, Adler J, Jäger A, Pesavento M, Kupnik M, Grosskurth D, Rutsch M, Adler J, Jäger A, Pesavento M, Kupnik M (2019) 3D imaging method for an air-coupled 40 kHz ultrasound phased-array. Univ RWTH Aachen. https://doi.org/10.18154/RWTH-CONV-238964

Bharadwaj PM, Kathavathe AR, Sandarsh MK, Hegde R, Kumar S (2020) MIMO versus phased array antenna systems for 5G mobile communication systems. Perspect Commun Embedded-Syst Signal-Process-PiCES 4(4):64–68

Çağlayan Z, Demircan Yalçın Y, Külah H, Çağlayan Z, Yalçın YD, Külah H (2020) A prominent cell manipulation technique in BioMEMS: dielectrophoresis. Micromachines 11(11):990. https://doi.org/10.3390/mi11110990

Chakraborty A, Gupta B (2017) Utility of RF MEMS miniature switched capacitors in phase shifting applications. AEU-Int J Electron Commun 75:98–107. https://doi.org/10.1016/j.aeue.2017.03.011

Chen A, Jiang W, Chen Z, Li Y (2013) A low-loss ka-band distributed metal-air-metal mems phase shifter. Przegląd Elektrotech 2013(7):77–80

Cpw S, Lctik AD, Wu Q, Tang K, Feng Z-R, Sun F-L, Li L-W (2007) A DMTL phase shifter using insulation layer and saw-shaped CPW. In: 2007 Asia-Pacific microwave conference. IEEE, New York, pp 1–4

Daw AF, El-Dessouky MS, El-Hannawy AE, El Hady MM (2008) 2 GHz RF MEMS based microwave phase shifter with high resolution tuning. In: 2008 international conference on computer engineering & systems. IEEE, New York, pp 35–40

De Flaviis F, Alexopoulos NG, Stafsudd OM (1997) Planar microwave integrated phase-shifter design with high purity ferroelectric material. IEEE Trans Microw Theory Tech 45(6):963–969. https://doi.org/10.1109/22.588610

Dey S, Koul SK (2015) 10–25 GHz frequency reconfigurable MEMS 5-bit phase shifter using push–pull actuator based toggle mechanism. J Micromech Microeng 25(6):65011. https://doi.org/10.1088/0960-1317/25/6/065011

Dey S, Koul SK (2020) Reliable, compact, and tunable MEMS bandpass filter using arrays of series and shunt bridges for 28-GHz 5G applications. IEEE Trans Microw Theory Tech 69(1):75–88. https://doi.org/10.1109/TMTT.2020.3034182

Dragunov VP, Ostertak DI, Kiselev DE, Dragunova EV (2022) Impact-enhanced electrostatic vibration energy harvester. J Appl Comput Mech 8(2):671–683. https://doi.org/10.22055/jacm.2021.38781.3312

Du Y, Bao J, Zhao X (2010) 5-bit MEMS distributed phase shifter. Electron Lett 46(21):1452–1453. https://doi.org/10.1049/el.2010.2492

Du Y, Bao J, He Z, Jiang J (2013a) A X-band switched-line 5-bit phase shifter with RF MEMS multithrow switches. In: The 8th annual IEEE international conference on nano/micro engineered and molecular systems. IEEE, New York, pp 296–299

Du YJ, Bao JF, Jiang JW (2013b) A new design of multi-bit RF MEMS distributed phase shifters for phase error reduction. Microsyst Technol 19(2):237–244. https://doi.org/10.1007/s00542-012-1649-z

Elloian J (2021) Design of a flexible ultrasound phased array with adaptive phasing for curvature. Columbia University, Columbia

Entesari K, Rebeiz GM (2005) A 12–18-GHz three-pole RF MEMS tunable filter. IEEE Trans Microw Theory Tech 53(8):2566–2571. https://doi.org/10.1109/TMTT.2005.852761

Fernandez-Bolanos M, Lisec T, Dainesi P, Ionescu AM (2008) Thermally stable distributed MEMS phase shifter for airborne

and space applications. In: 2008 38th European microwave conference. IEEE, New York, pp 100–103
Hayden JS III (2002) High-performance digital X-band and Ka-band distributed MEMS phase shifters. University of Michigan, Michigan
Hayden JS, Rebeiz GM (2003) Very low-loss distributed X-band and Ka-band MEMS phase shifters using metal-air-metal capacitors. IEEE Trans Microw Theory Tech 51(1):309–314. https://doi.org/10.1109/TMTT.2002.806520
Huang Y, Bao J, Li X, Wang Y, Du Y, Huang Y, Bao J, Li X, Wang Y, Du Y (2015) A 4-bit switched-line phase shifter based on MEMS switches. In: 10th IEEE international conference on nano/micro engineered and molecular systems. IEEE, New York, pp 405–408
Jian Z, Wei Y-YY, Chen C, Yong Z, Le L (2006) A compact 5-bit switched-line digital MEMS phase shifter. In: 2006 1st IEEE international conference on nano/micro engineered and molecular systems. IEEE, New York, pp 623–626
Jin L, Wu Q, Tang K, He X, Yang G, Fu J, Zhang R, Lee J (2008) A novel design of RF-MEMS phase shifter based on bridge-like coplanar waveguide. In: 2008 6th IEEE international conference on industrial informatics. IEEE, New York, pp 171–175
Kazakov SY, Shchelkunov SV, Yakovlev VP, Kanareykin A, Nenasheva E, Hirshfield JL (2010) Fast ferroelectric phase shifters for energy recovery linacs. Phys Rev Spec Top-Accelerators and Beams 13(11):113501. https://doi.org/10.1103/PhysRevSTAB.13.113501
Lacroix B, Pothier A, Crunteanu A, Blondy P (2008) Phase shifter design based on fast RF MEMS switched capacitors. In: 2008 European microwave integrated circuit conference. IEEE, New York, pp 478–481
Li X, Chan KY, Ramer R (2019) E-band RF MEMS differential reflection-type phase shifter. IEEE Trans Microw Theory Tech 67(12):4700–4713. https://doi.org/10.1109/TMTT.2019.2944623
Liu Y, Borgioli A, Nagra ASAS, York RARA, Liu Y, Nagra ASAS, York RARA (2000) Low-loss distributed MEMS phase shifter. IEEE Microw Guided Wave Lett 10(1):7–9. https://doi.org/10.1109/75.877230
Lou J, Hao J, Hu X, Li Q, Dai P (2010) Design and fabrication of 2-bit loaded-line MEMS phase shifter. In: 2010 international conference on microwave and millimeter wave technology. IEEE, New York, pp 1652–1654
Maruhashi K, Mizutani H, Ohata K, Fet UUA (1998) Ka-band 4-bit monolithic phase shifter using unresonated FET switches. IEEE MTT-S international microwave symposium digest (Cat. No. 98CH36192). IEEE 1998:51–54
McFeetors G, Okoniewski M (2004) Analog tunable microwave phase shifters using RF MEMS. In: 2004 10th international symposium on antenna technology and applied electromagnetics and URSI conference. IEEE, New York, pp 1–4
Medina-Rull A, Pasadas F, Marin EG, Toral-Lopez A, Cuesta J, Godoy A, Jiménez D, Ruiz FG, Jiménez D, Ruiz FG (2020) A graphene field-effect transistor based analogue phase shifter for high-frequency applications. IEEE Access 8:209055–209063. https://doi.org/10.1109/ACCESS.2020.3038153
Mishra MK, Dubey V, Mishra PM, Khan I (2019) MEMS technology: a review. J Eng Res Rep 4(1):1–24. https://doi.org/10.9734/jerr/2019/v4i116891
Nishimura K, Kao H-Y, Ishimura S, Tanaka K, Inohara R, Ishimura KON, Hsunk AO, Shimura SHI, Anaka KAT, Nohara RYOI (2022) Multiple beam-steering for 5G multi-user MIMO mobile fronthaul based on IFoF and RoF transmission. Opt Continuum 1(5):1165–1175
Pozar DM (2011) Microwave engineering. Wiley, New York
Puri M, Das A, Sengar JS (2013) A novel design of monolithically integrated phased array antenna employing 4-bit dmtl phase shifter. In: 2013 Tenth international conference on wireless and optical communications networks (WOCN). IEEE, New York, pp 1–6
Qin Z, Liu X, Ma C (2021) Acoustic wave reflection control based on broadband differential phase shifters. Front Mech Eng 7:83. https://doi.org/10.3389/fmech.2021.703019
Ramli NA, Arslan T (2017) Design and simulation of a 2-bit distributed S-band MEMS phase shifter. In: 2017 18th international conference on thermal, mechanical and multi-physics simulation and experiments in microelectronics and microsystems (EuroSimE). IEEE, New York, pp 1–5
Rebeiz GM (2004) RF MEMS: theory, design, and technology. Wiley, New York
Rebeiz GM, Barker NS (2000) Optimization of distributed MEMS transmission-line phase shifters-U-band and W-band designs. IEEE Trans Microw Theory Tech 48(11):1957–1966. https://doi.org/10.1109/22.883878
Rotake D, Darji A, Kale N (2020) Fabrication, calibration, and preliminary testing of microcantilever-based piezoresistive sensor for BioMEMS applications. IET Nanobiotechnol 14(5):357–368. https://doi.org/10.1049/iet-nbt.2019.0277
Sengar JS, Das A, Puri M. Design of 3-bit digital DMTL phase shifter for C-to Ku-band applications. In: 2013 third international conference on advances in computing and communications. IEEE, New York, pp 427–432
Shafai C, Shafai L, Sharma S, Chrusch DD (2003) Fabrication and testing of a microstrip phase shifter using micromachined reconfigurable ground plane. In: IEEE Antennas and Propagation Society international symposium. Digest. Held in conjunction with: USNC/CNC/URSI North American radio science meeting (Cat. No. 03CH37450). IEEE, New York, pp 274–277
Teymoori MM, Dousti M, Afrang S (2020) A low-loss compact six-bit DMTL phase shifter for phased array antenna applications. Int J Circuit Theory Appl 48(12):2111–2129. https://doi.org/10.1002/cta.2871
Trinh KT, Feng J, Shehab SH, Karmakar NC (2019) 1.4 GHz low-cost PIN diode phase shifter for *L* -band radiometer antenna. IEEE Access 7:95274–95284. https://doi.org/10.1109/ACCESS.2019.2926140
Yang JG, Yang K (2011) Ka-band 5-bit MMIC phase shifter using InGaAs PIN switching diodes. IEEE Microwave Wirel Compon Lett 21(3):151–153. https://doi.org/10.1109/LMWC.2010.2104314