Microsystem Technologies (2021) 27:3457–3464
https://doi.org/10.1007/s00542-020-05140-w

TECHNICAL PAPER

Design and optimization of asymmetrical TFET using meta-heuristic algorithms

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Received: 19 November 2020 / Accepted: 21 November 2020 / Published online: 2 January 2021
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Abstract

The complex process of semiconductor device design requires precise models and efficient optimizers. This article puts forward an Asymmetrical Hetero-Dielectric (AHD) Triple Material Gate (TMG) n-type Junctionless Tunnel Field Effect Transistor (JL-TFET). A higher gate control is achieved by using triple material in control gate and hetero-dielectric oxide, which results in high ON current and low leakage. The surface potential based model for the proposed structure is derived by analytically solving 2-D Poisson's equation with hetero-dielectric gate oxide. This work also adopts intelligent techniques for extraction of optimal model parameters by using the derived mathematical model for the proposed JLTFET structure. The optimization technique used in this work combines the advantage of Particle Swarm Optimization (PSO) algorithm and Differential Evolution (DE) algorithm. A comparison with the conventional design process reflects that the use of optimization technique provides a novel approach to tune the process parameters. This technique outperforms the state of art design techniques and provides best accuracy along with exceptional computational efficiency. A current ratio of 1.25×10^{10} A and Point Subthreshold Swing (SS) values of 9 mV/dec and average SS of 48 mV/dec is achieved by optimizing the proposed structure.

1 Introduction

Tunnel field effect transistors (TFET) (Bhuwalka et al. 2005; Bhuwalka et al. 2006) with Subthreshold Slope (SS) below 60 have become the adroit candidate for low power applications. However, with shrinking device dimension, the fabrication of semiconductor based devices with abrupt junctions became increasingly complex (Pratap et al. 2016). Thus, Junctionless TFET (JL-TFET) were proposed (Ghosh and Akram 2013) with uniform doping throughout the device and no abrupt junction, thereby reducing fabrication complexity (Damrongplasit et al. 2013; Gundapaneni et al. 2012). The JLTFET combines the concept of JLFET and TFET, where an N + N+N + structure can be converted into a PIN structure by effectively controlling the polar gate work function (Ghosh and Akram 2013). This work incorporates the concept of JLTFET with triple material gate (TMG) (Bagga et al. 2015; Vanitha et al. 2015; Dewan et al. 2016) along with the use of asymmetric hetero-dielectric in a Si based structure. The proposed structure is found to improve the current ratio, SS and comparatively involves less fabrication complexity (Toh et al. 2007). The use of asymmetric dual k is known to improve the electric field across the junction (Raushan et al. 2018) and thereby increasing the ON current. Although, a number of models have been proposed for JLTFET (Ghosh and Akram 2013; Bal et al. 2014; Akram et al. 2014), but the analytical model for TMG AHD JLTFET is introduced for the first time in this work. The proposed structure is analytically solved for the expression of surface potential. The derived expression is then used as a tool to optimize the structure. The sole theory is to amalgamate the above three concept in a single device and study its impact. However, state of art techniques in semiconductor design involves rigorous process of tuning the design parameters and re-simulating the structure to achieve the specified target. Thus, these empirical techniques have become a bottleneck for semiconductor device designers. Therefore, this paper highlights the use of optimization algorithms to tune the device parameters. The

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surface potential model incorporates all physical effects even in downscaled devices. Thus, surface potential based model for the proposed device is derived and is used to optimize the structure. The traditional optimization approaches such as numerical based approaches (Pinnau 2007), derivative based techniques (Lian et al. 2018) are known to suffer from local optima stagnation, poor convergence and are not suitable for complex quantum model analysis. This paper uses various modern optimization approaches (Zhang et al. 2009; Talukder 2011; Kameyama 2009; Liu et al. 2014; Storn and Price 1995; Mirjalili and Lewis 2016a, b) to design the structure. However, a hybrid combination of PSO and DE i.e. DEPSO provides the best accuracy as well as computational efficiency for the proposed model. All device simulations are performed in Synopsis TCAD tool (S.I. Association 2015). The optimization algorithms are implemented in MATLAB 2015 version to achieve the target design parameters. This paper has been structured as follows: Sect. 2 describes the device architecture, Sect. 3 illustrates the optimization process, Sect. 4 explains the model derivation, Sect. 5 discusses the results and finally Sect. 6 draws the conclusion.

2 Device Structure

This section illustrates the proposed structure shown in Fig. 1. The structure depicts an n-type Si channel hetero-dielectric double gate Junctionless TFET. A uniform doping concentration of 1×10^{19} cm^{-3} is used throughout the device, thus making a Junctionless TFET easier to fabricate (Bal et al. 2014). The device structure consists of two isolated gates: Polar gate nearer to the source for generating P + region and control gate in middle to create channel.

The polar gate is biased at 0 V (Bal et al. 2014). A triple material configuration is used for controlling the gate with different metal M1 (auxiliary), M2 (control), and M3 (tunnel). Each metal gate has different work function Φ_1, Φ_2 *and* Φ_3 and length L1, L2 and L3. Proper tuning of control gate work function will result in better

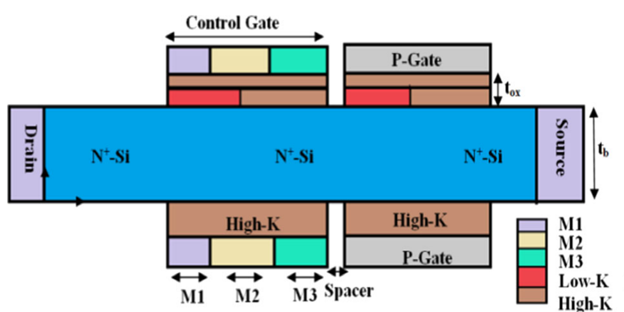

Fig. 1 Proposed structure for AHD-TMG-JLTFET

current ratio. The inclusion of spacer between two gates helps in reducing the coupling between the two gates (Akram et al. 2014). The dielectric of both polar and control gates is of two different types: high-k (HfO_2) near the source and low-k (SiO_2) near the drain in two different layers. The use of asymmetric HD layer across front and back gate resulted in improved current characteristics. The effective oxide thickness is calculated as in (Bentrcia et al. 2012). All simulations are performed in Synopsis TCAD tool.

3 Optimization problem formulation

The main concern associated with TFET design is to improve the current ratio and this opens to many novel device structures. A structure can provide its best performance if properly optimized. Thus, optimizing the structure plays a crucial role. This paper makes use of various evolutionary computational algorithms. The algorithms are chosen in such a way that they improve computational efficiency as well as accuracy without compromising the device inherent characteristics. This technique of device optimization requires an objective function. The model for surface potential is derived for the proposed structure. Since, the surface potential based model is quite close to physical prototype and takes into account various physical effects occurring in TFET, it is used as an objective function. Thereby, improving surface potential across the junction will help improving the electric field and, in turn, the ON current also increases. The optimization process is divided into three steps:

3.1 Preprocess

The sensitivity analysis is performed in this process so that the parameters which significantly affect device performance can be sorted. As the device model consists of a large number of parameters, it becomes difficult to handle significant amount of variables. Thus, preprocess aids in data reduction and thereby in limiting the computational complexity. The selection of design variables is divided into certain sections and is done by performing sensitivity analysis. The sensitivity analysis can facilitate understanding the impact of various parameters on the device performance. A set of parameters (say, L1, L2, and L3), are adjusted while others are fixed at certain values to assess the impact on device performance. The device parameters are divided into certain groups and the sensitivity analysis is performed. The parameters which significantly influence the device performance are then selected as design variables and the other least significant parameters are considered as constant. Tables 1 and 2 list out the various

Table 1 Design constants

Parameter	Symbol	Dimension
Absolute permittivity	€_o	8.854*10^(12) F/m
Relative permittivity of SiO_2	€_sio2	3.9*€_o
Relative permittivity of Si	€si	11.4*€_o
Relative permittivity of HfO_2	€hfo2	25*€_o
Charge	q.	1.6*10^(− 19) cm^{-3}
Electron affinity of Si	χ	4.05 eV
Energy gap of Si	E_{g2}	1.1
Uniform doping		1*10^(19) cm^{-3}
Temperature	T	300 k
Intrinsic conc of Si	n_i	1.5*10^(10) cm^{-3}
Boltzmann constant	k	1.380649×10^{-23} J/K

Table 2 Design variables

Variables	Range
L1 (nm)	0 < L1 < 5
L2 (nm)	2 < L2 < 20
L3 (nm)	0 < L3 < 7
t_{oxf} (nm)	1–4
t_s (nm)	1–7
t_{oxb} (nm)	1–5
V_{gs}	0–1.2

design constants and variables used in the optimization process. The choice of material and doping concentrations are kept fixed.

3.2 Parameter extraction/algorithm parameters

A number of modern optimization algorithms such as DEPSO, human behavior based particle swarm optimization (HBPSO) (Liu et al. 2014), particle swarm optimization (PSO) and Whale Optimization Algorithm (WOA) are used to optimize the structure. The effectiveness of different optimization algorithms are evaluated by performing 20 independent runs of each algorithm. This technique is used to evaluate the robustness of the algorithms by considering the best achieved value of the objective function. A comparative analysis reflects that the performance of DEPSO is superior in terms of efficiency and accuracy. The working principle of DEPSO algorithm is explained in the subsequent section.

Hybrid DEPSO: The DEPSO algorithm (Zhang et al. 2009) is the hybrid version of the DE and PSO algorithm. The DE has some pros, and it includes its capacity to preserve the diversity of the population and the ability to explore local search. But the algorithm has no means to memorize the preceding process and utilize the global information regarding the search space. Therefore, there will be wastage of computing power and there is a risk for the algorithm to be trapped in local optima. The differential information can be useful for the search ability, but it also leads to instability in some solutions. To get the advantages of both PSO and DE, the hybrid DEPSO algorithm has been designed. Here the PSO algorithm is integrated into DE and thus it results in fast convergence and higher population diversity (Zhang et al. 2009). The algorithm parameters are listed in Table 3 (Fig. 2).

3.3 Post process

Post process involves the validation of the results obtained by optimization algorithm by simulating the results in TCAD simulator.

4 Mathematical Model for the proposed structure

The 2-D Poisson's equation for potential distribution of channel can be represented as

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = \frac{-qN_{ch}}{\varepsilon_{si}} \quad (0 \le x \le L; 0 \le y \le t_{si}) \tag{1}$$

where, N_{ch} is the channel doping concentration, ε_{si} represents the dielectric constant of Si, L represents the total length of the control gate, $\phi(x,y)$ is the potential at any point in the channel, q is the charge of electron, and t_{si} is the thickness of the device.

A parabolic function by Young's approximation is used to represent potential profile across the channel with A_0 being the surface potential which is a function of x and,$A_1(x)$, $A_2(x)$ are arbitrary constants:

$$\phi(x,y) = A_0 + A_1(x)y + A_2(x)y^2. \tag{2}$$

As three different metals are used M1, M2, M3, thus, the surface potential under each metal can be expressed as

Table 3 Optimization algorithm parameters

Algorithm	Parameters	Value
DEPSO	Social learning rate (c_1)	0.12
	Cognitive learning rate (c_2)	1.2
	Dimension	7
	Swarm size	50
	Mutation factor (F)	0.5
	Crossover rate	0.9

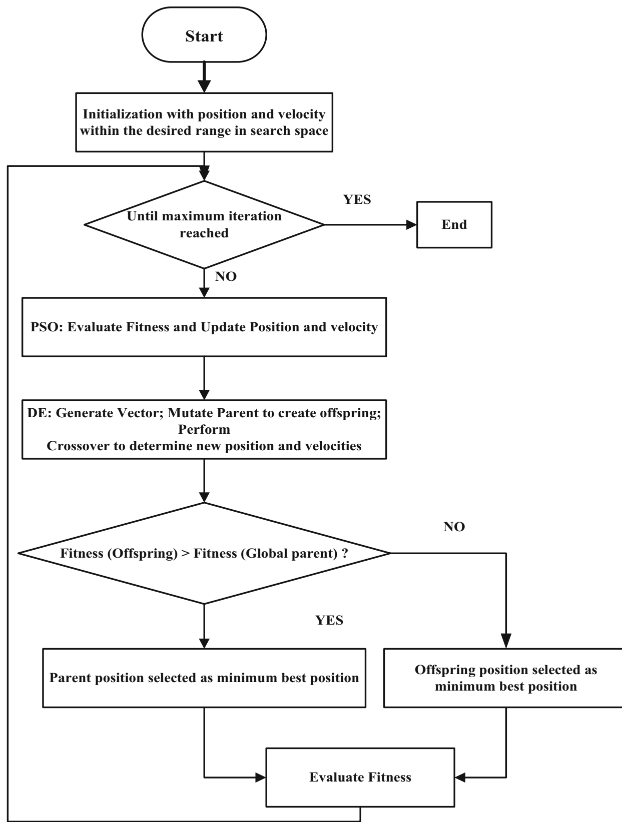

Fig. 2 The DEPSO algorithm

$$\phi_j(x,y) = A_{0j} + A_{j1}(x)y + A_{j2}(x)y^2. \quad (3)$$

For $L_{j-1} \le x \le L_j$ and $0 \le y \le t_{si}$, where j = 1, 2, 3 for M1, M2, M3 and ϕ_j is the corresponding potential. L_0 is the starting point of the channel i.e. $L_0 = 0$.

As three different materials were used in the gate, they will have different work function and subsequently different flat band where, χ is the electron affinity, E_g is the band gap of Silicon at room temperature and Φ_B is the bulk potential voltage:

$$V_{FB,L1} = \Phi_{\mathrm{M1}} - \Phi_{\mathrm{Si}}, \quad V_{FB,L2} = \Phi_{\mathrm{M2}} - \Phi_{\mathrm{Si}}, \quad V_{FB,L3} = \Phi_{\mathrm{M3}} - \Phi_{\mathrm{Si}} \quad (4)$$

$\Phi_{\mathrm{M1}}, \Phi_{\mathrm{M2}}, \Phi_{\mathrm{M3}}$ are the work function of M1, M2, M3 and Φ_{Si} is the silicon work function:

$$\Phi_{\mathrm{Si}} = \chi + \frac{E_g}{2q} + \Phi_B \quad (5)$$

$$\Phi_B = \mathrm{V_T} \ln\left(\frac{\mathrm{N_{ch}}}{\mathrm{n_i}}\right), \quad (6)$$

where, thermal voltage, $V_T = \frac{kT}{q}$ and $\mathrm{n_i}$ is the intrinsic concentration of silicon.

1. In case of TMG the electric field at the front and back gate is continuous

$$\left.\frac{d\phi_1(x,y)}{dy}\right|_{y=0} = -\frac{C_{ox1f}}{C_s}\frac{V_{gs1} - A_{01(x)}}{t_{si}}, \quad V_{gs1} = V_{gs} - V_{FB,L1}, \quad C_s = \frac{\varepsilon_{Si}}{t_{Si}}$$
$$\left.\frac{d\phi_2(x,y)}{dy}\right|_{y=0} = -\frac{C_{ox2f}}{C_s}\frac{V_{gs2} - A_{02(x)}}{t_{si}}, \quad V_{gs2} = V_{gs} - V_{FB,L2}$$
$$\left.\frac{d\phi_3(x,y)}{dy}\right|_{y=0} = -\frac{C_{ox3f}}{C_s}\frac{V_{gs3} - A_{03(x)}}{t_{si}}, \quad V_{gs3} = V_{gs} - V_{FB,L3}. \quad (7)$$

Again for metal M1, the dielectric layer 1 consists of HfO_2 and layer 2 consists of SiO_2, so the equivalent capacitance can be calculated as

$$C_{ox1f} = \frac{C_{oxH}.C_{oxs}}{C_{oxH} + C_{oxs}}, \text{ where layer 1}, C_{oxH} = \frac{\varepsilon_{HfO_2}}{t_{oxf}} \text{ and layer 2}, C_{oxs} = \frac{\varepsilon_{SiO_2}}{t_{oxf}}.$$

Similarly, for M2, the dielectric layer 1 consists of HfO_2 and SiO_2 and layer 2 consists of HfO_2 only, so the equivalent capacitance can be calculated as

$$C_{ox2f} = \frac{C_{ox2}.C_{ox22}}{C_{ox2} + C_{ox22}},$$

where layer 1, $C_{ox2} = \frac{\varepsilon_{HfO_2+\varepsilon_{SiO_2}}}{t_{oxf}}$

and layer 2, $C_{ox22} = \frac{\varepsilon_{HfO_2}}{t_{oxf}}$.

For M3, the entire dielectric layer consists of HfO_2

$$C_{ox3f} = \frac{\varepsilon_{HfO_2}}{2t_{oxf}}$$

where, t_{oxf}, is the front oxide layer thickness and is equal to layer 2 thickness. Also ε_{HfO_2} *and* ε_{SiO_2} are permittivity of HfO_2 and SiO_2.

2. Electric field at the back gate is also continuous at $y = t_{si}$,

$$\left.\frac{d\phi_1(x,y)}{dy}\right|_{y=t_{si}} = -\frac{C_{oxb}}{C_s}\frac{\phi_{B1}(x) - V_{gs1}}{t_{si}}$$
$$\left.\frac{d\phi_2(x,y)}{dy}\right|_{y=t_{si}} = -\frac{C_{oxb}}{C_s}\frac{\phi_{B2}(x) - V_{gs2}}{t_{si}}$$
$$\left.\frac{d\phi_3(x,y)}{dy}\right|_{y=t_{si}} = -\frac{C_{oxb}}{C_s}\frac{\phi_{B3}(x) - V_{gs3}}{t_{si}} \quad (8)$$

$C_{oxb} = \frac{\varepsilon_{HfO_2}}{t_{oxb}}$, ϕ_B is the potential along the back gate oxide, which is same as front gate potential. $\phi_B(x,y) = \phi(x,y)|_{y=t_{si}}$.

$\phi_{Bj}(x,y)$ is the corresponding back gate potential and can be expressed as

$$\phi_{Bj}(x,y) = A_{0j}(x) + A_{j1}(x)t_{Si} + A_{j2}(x)t_{Si}^2, \quad \text{for M1, M2, M3}$$

$\phi_j(x, y = 0) = A_{0j}$, the potential of the channel is the surface potential.

3. Surface potential is similar and continuous at interface

$$\begin{aligned} \phi_1(L_1,0) &= \phi_2(L_1,0) \\ \phi_2(L_2,0) &= \phi_3(L_2,0). \end{aligned} \tag{9}$$

4. Electric field is similar and continuous at interface

$$\begin{aligned} \left.\frac{d\phi_1(x,y)}{dy}\right|_{x=L_1} &= \left.\frac{d\phi_2(x,y)}{dy}\right|_{x=L_1} \\ \left.\frac{d\phi_2(x,y)}{dy}\right|_{x=L_2} &= \left.\frac{d\phi_3(x,y)}{dy}\right|_{x=L_2}. \end{aligned} \tag{10}$$

5. $\phi_1(0,0) = V_{bipot} = V_T \ln\left(\frac{N_a N_{ch}}{n_i^2}\right)$, where, V_{bipot} is the built in potential and V_{DS} is the drain to source voltage. $N_a = N_d = N_{ch}$ as device is uniformly doped.
6.

$$\phi_3(L_3,0) = V_{bipot} + V_{DS} = V_T \ln\left(\frac{N_d N_{ch}}{n_i^2}\right) \tag{11}$$

Solving Eq. (3) the constants can be found and are represented below

$$A_{11}(x) = -\frac{C_{ox1f}}{C_s}\frac{V_{gs1} - A_{01(x)}}{t_{si}}$$

$$A_{21}(x) = -\frac{C_{ox2f}}{C_s}\frac{V_{gs2} - A_{02(x)}}{t_{si}}$$

$$A_{31}(x) = -\frac{C_{ox3f}}{C_s}\frac{V_{gs3} - A_{03(x)}}{t_{si}}$$

$$A_{12}(x) = \frac{\frac{C_{oxb}}{C_s t_{si}}\left(1 + \frac{C_{ox1f}}{C_s} + \frac{C_{ox1f}}{C_{oxb}}\right)}{t_{si}\left(2 + \frac{C_{ox1f}}{C_s}\right)}\left[V_{gs1} - A_{01(x)}\right]$$

$$A_{22}(x) = \frac{\frac{C_{oxb}}{C_s t_{si}}\left(1 + \frac{C_{ox2f}}{C_s} + \frac{C_{ox2f}}{C_{oxb}}\right)}{t_{si}\left(2 + \frac{C_{ox2f}}{C_s}\right)}\left[V_{gs2} - A_{02(x)}\right]$$

$$A_{12}(x) = \frac{\frac{C_{oxb}}{C_s t_{si}}\left(1 + \frac{C_{ox3f}}{C_s} + \frac{C_{ox3f}}{C_{oxb}}\right)}{t_{si}\left(2 + \frac{C_{ox3f}}{C_s}\right)}\left[V_{gs3} - A_{03(x)}\right].$$

Putting the values of the above constants in Eq. (3) and comparing with Eq. (1), we get

$$\frac{\partial^2\phi_j(x)}{\partial x^2} - m_j\phi_j(x) = n_j$$

where, $m_j = \frac{2C_{oxb}}{C_s t_{si}}\left(1 + \frac{C_{oxfj}}{C_s} + \frac{C_{oxfj}}{C_{oxb}}\right)$

$$n_j = \frac{-qN_{ch}}{\varepsilon_{si}} - \frac{2C_{oxb}}{C_s t_{si}}V_{gsj}\left(1 + \frac{C_{oxfj}}{C_s} + \frac{C_{oxfj}}{C_{oxb}}\right). \tag{12}$$

The surface potential under three regions

$$\phi_1(x) = U\exp(\lambda_1 x) + V\exp(-\lambda_1 x) - \frac{n_1}{m_1} \tag{13}$$

$$\phi_2(x) = W\exp(\lambda_2(x - L_1)) + X\exp(-\lambda_2(x - L_1)) - \frac{n_2}{m_2} \tag{14}$$

$$\begin{aligned} \phi_3(x) = {} & Y\exp(\lambda_3(x - L_1 - L_2)) \\ & + Z\exp(-\lambda_3(x - L_1 - L_2)) - \frac{n_3}{m_3} \end{aligned} \tag{15}$$

where, $\lambda_j = \sqrt{m_j}$, j = 1, 2, 3.

The constants U, V, W, X, Y, and Z can be solved by using boundary conditions (6)–…

$$U = V_{bipot} - V + \frac{n_1}{m_1}$$

$$W = U\exp(\lambda_1 L_1) + \frac{n_2}{m_2} - \frac{n_1}{m_1}$$

$$X = V\exp(-\lambda_1 L_1) + \frac{n_2}{m_2} - \frac{n_1}{m_1}$$

$$Y = \exp(-\lambda_3 L_3) + (V_{bipot} + V_{DS}) + \frac{n_3}{\alpha_3} - Z\exp(-\lambda_3 L_3)$$

$$P_1 = -\frac{n_1}{m_1}, P_2 = -\frac{n_2}{m_2}, P_3 = -\frac{n_3}{m_3}$$

$$D = \frac{C_1}{C_2},$$

$$C_1 = \exp(-\lambda_1 L_1 + 2\lambda_3 L_3) + \exp(\lambda_1 L_1)$$

$$C_2 = \exp(-\lambda_1 L_1 + 2\lambda_3 L_3) - \exp(\lambda_1 L_1)$$

$$E = 2D\cosh(\lambda_2 L_2) - 2\sinh(\lambda_2 L_2)$$

$$\begin{aligned} V = {} & \frac{(V_{bipot} + V_{DS}) + \exp(-(\lambda_1 L_1 + \lambda_3 L_3)(1 - D)}{E} + \frac{D(P_3 - P_2)}{E} \\ & + \frac{P_3\exp(-(\lambda_1 L_1 + \lambda_3 L_3)(D - 1) + V_{bipot} + \exp(\lambda_2 L_2)(1 - D) + P_1\exp(\lambda_2 L_2)(1 - D)}{E} \\ & + \frac{(D(P_1 - P_2)\cosh(\lambda_2 L_2 - \lambda_1 L_1) - \sinh(\lambda_2 L_2 - \lambda_1 L_1))}{E} \end{aligned}$$

$$\begin{aligned} Z = {} & \frac{2V\sinh(\lambda_2 L_2)}{C_2} + \frac{P_1\exp(\lambda_2 L_2)}{C_2} + \frac{(V_{bipot} + V_{DS}) + \exp(-(\lambda_1 L_1 + \lambda_3 L_3)}{C_2} \\ & + \frac{(P_2 - P_3)}{C_2} \\ & + \frac{V_{bipot}\exp(\lambda_2 L_2) - [(P_1 - P_2)\cosh(\lambda_2 L_2 - \lambda_1 L_1)] - P_3\exp(-(\lambda_1 L_1 + \lambda_3 L_3)}{C_2}. \end{aligned}$$

5 Results validation and discussion

5.1 Device characteristics

Figure 3 depicts the characteristics of the projected device. It illustrates that AHD-TMG-JLTEFT can produce higher ON current compared to conventional JLTFET (Ghosh and Akram 2013) and DMGJLTFET (Bal et al. 2014) if proper work function is chosen. Table 4 reflects the comparison among various JL-TFET.

The OFF current and SS value also shows much improvement compared to conventional device. The impact of polar gate work function variation is portrayed in Fig. 4. The transconductance is also an essential parameter to assess the analog performance of devices, which is

defined as the first derivative of drain current (I_{ds}) with respect to V_{GS}, the formula of g_m is given by Eq. (16): as shown in Fig. 5, the g_m of the AHD-TMG-JLTEFT is found to be 1×10^{-3} S/µm which is much higher as compared to other reported JLTFET:

$$g_m = \frac{dI_D}{dV_{gs}}. \tag{16}$$

Figure 6 shows the surface potential plot of simulated and modeled surface potential. The close matching between the plots validates the accuracy of the proposed model. The deviation is little higher in the drain side due to assumption considered while deriving the model. Figure 7 depicts the comparison between the existing structures and the proposed one. The use of triple material gate improves the surface potential across the channel. The use of three gate materials resulted in the step change in surface potential at the metal interface. This increase in surface potential is due to increase in carrier velocity as well as transport efficiency.

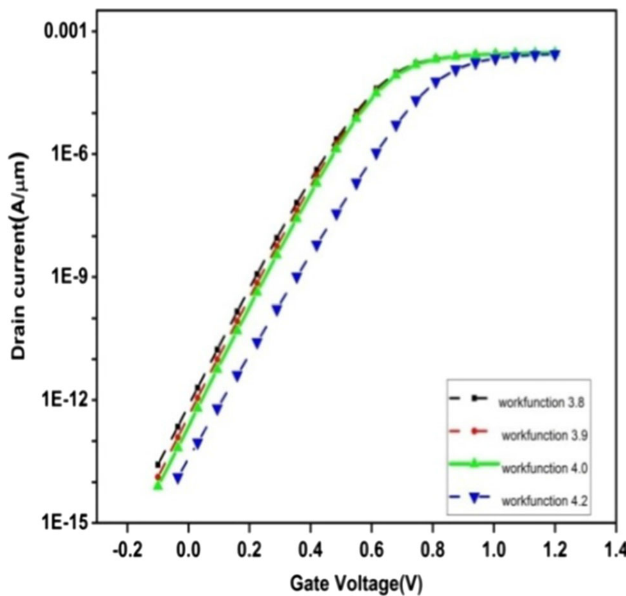

Fig. 3 $I_D - V_{GS}$ as function of various control gate work function

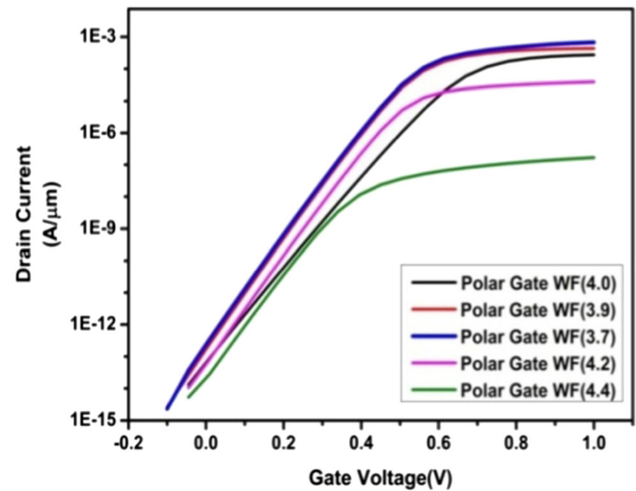

Fig. 4 $I_D - V_{GS}$ as function of polar gate work function

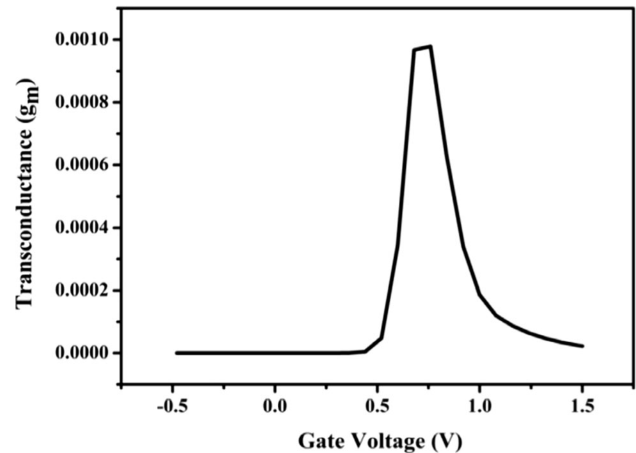

Fig. 5 Transconductance plot

5.2 Convergence analysis and optimization results validation

The mathematical model of the proposed structure discussed in Sect. 4 Eq. (15) is optimized using a variety of algorithms such as DEPSO, DE, PSO, HBPSO, and WOA. The main purpose is to maximize the surface potential at the tunnel junction by optimizing the variables in Table 2. All optimization algorithms are implemented in the MATLAB software for obtaining the best values for process parameters and they are listed out in Table 5. The

Table 4 Comparison table for various existing work

Ref	I_{ON} (A/µm)	I_{OFF} (A/µm)	Ratio	V_{th} (V)	SS (aver.)	SS (Pts)
Ghosh and Akram (2013)	36×10^{-6}	5×10^{-14}	6×10^{8}	0.4	70	38
Bal et al. (2014)	18×10^{-5}	3×10^{-13}	6×10^{8}	0.4	–	17
Gupta and Kumar (2019)	1×10^{-6}	1×10^{-13}	6×10^{7}	0.8	48	–
This work	3×10^{-4}	2.4×10^{-14}	1.2×10^{10}	0.3	48	9

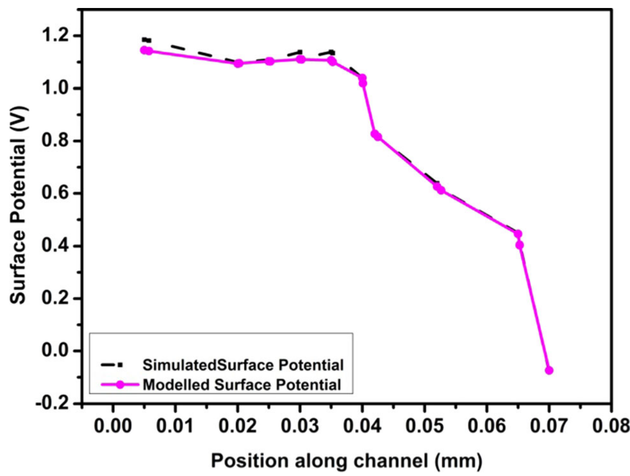

Fig. 6 Simulated and modeled surface potential

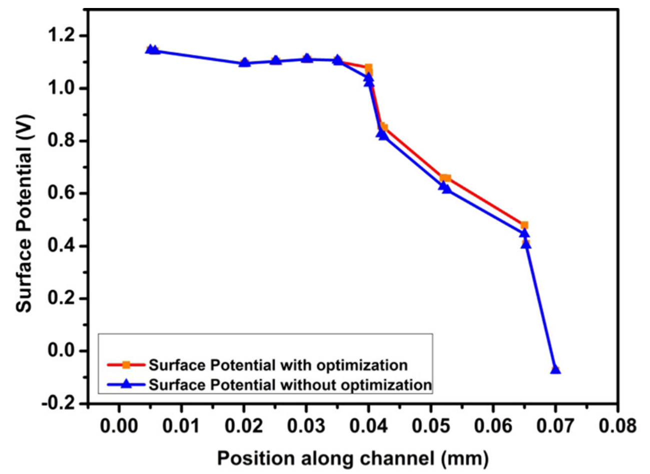

Fig. 8 Surface potential after optimization

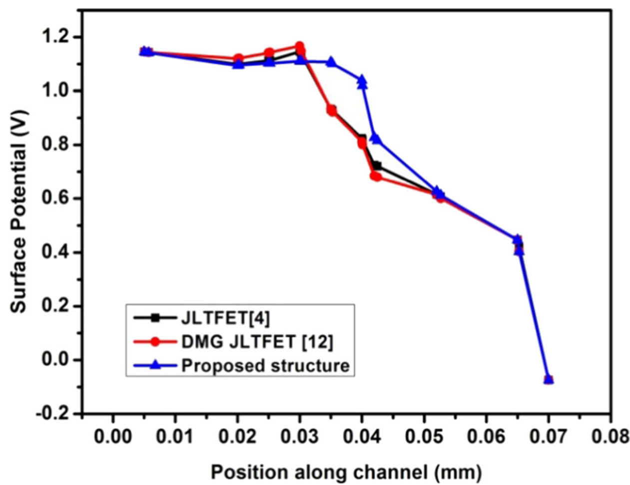

Fig. 7 Comparison plot of surface potential of various structures

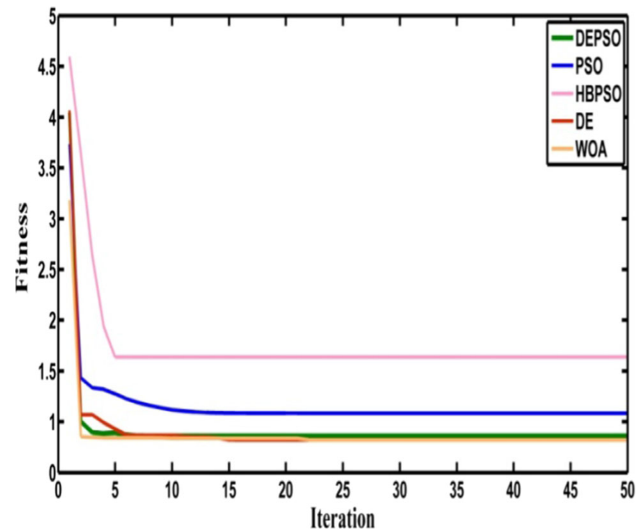

Fig. 9 Sensitivity analysis for fitness evaluation

results in Table 5 depict that DEPSO can achieve the most accurate result compared to TCAD simulated result. A comparison plot of surface potential derived from optimization of analytical model by DEPSO algorithm and TCAD simulated model is plotted in Fig. 8. The comparison plot reflects that DEPSO algorithm based optimized structure can achieve higher values of surface potential compared to the values obtained by hit and trail based optimization in TCAD. Thus, use of optimization algorithm can be useful in optimizing device parameters. Further, the convergence plot depicted Fig. 9 reflects that

Table 5 The optimized design variables obtained from different algorithms

Design variables	Range	DEPSO	DE	PSO	HBPSO	WOA
L1 (nm)	0 < L1 < 10	5	8	3	7.5	4.5
L2 (nm)	2 < L2 < 20	10	11	8	6	3.3
L3 (nm)	0 < L3 < 7	5	7	3	5	0
t_{oxf} (nm)	1–5	4	5	5	2.5	1
t_s (nm)	1–7	5	7	6	3	1.5
t_{oxb} (nm)	1–5	4	3	5	2	1
V_{gs}	0–1.8	1.2	1.5	1.2	1.2	1.1
Surface potential	–	0.7	0.5	0.6	0.55	0.7

DEPSO algorithm amongst all has better performance with best convergence in surface potential computation. The optimized dimensions achieved via algorithmic technique can be validated by designing the proposed structure with optimized dimension in TCAD software. The small deviation between results obtained from MATLAB and TCAD simulation is due to the rounding of the parameters. The simulated device reports an ON-current of 3×10^{-4} A and OFF-current of 2.4×10^{-14} A.

6 Conclusion

This paper provides a fresh concept to accelerate the tuning process parameters and help in benefiting design process of nano-devices. Finally, the validity of the proposed analytical model is compared with numerical solution simulation data results, which are obtained by using TCAD device simulator. In this article, we have successfully used DEPSO algorithm for surface-potential-based model parameter extraction for proposed TFET structure. Comparison reflects that measured surface potential and the optimized values are quite accurate.

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