Microsystem Technologies (2020) 26:2793–2799
https://doi.org/10.1007/s00542-020-04846-1

TECHNICAL PAPER

DC and analog/RF performance analysis of gate extended U-shaped channel tunnel field effect transistor

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Received: 6 October 2019 / Accepted: 7 April 2020 / Published online: 15 April 2020

Abstract
The DC and Analog/RF performance of Gate Extended-U-shaped channel tunneling field-effect transistors (GE-UTFET) was examined in this study. The performance of the device was investigated through technology computer added design in terms of transconductance (g_m), intrinsic capacitances (C_{gg}, C_{gs}, and C_{gd}), cut-off frequency (f_T), and gain-bandwidth product (f_A). Simulation results show that GE-UTFET has an improved DC characteristic than UTFET. Also, the better RF performance of GE-UTFET than UTFET makes it more suitable for high-frequency application which is attributed to the reduced miller capacitance (C_{gd}) and enhanced g_m.

1 Introduction

Tunneling FET is considered as the most promising device to substitute the MOSFET device due to its sub 60 mV/decade subthreshold swing (*SS*) and low leakage current. TFET is superior to MOSFET in terms of short channel effects (Wang et al. 2004; Choi et al. 2007; Avci et al. 2015). The major drawbacks faced by TFET devices are low ON-state current and intrinsic ambipolarity (Fuketa et al. 2015; Wang et al. 2016; Chen et al. 2014; Datta et al. 2014; Strangio et al. 2015; Dash et al. 2016). Unlike MOSFET, the working mechanism of TFET is Band to Band tunneling (BTBT). In n-TFET carriers injection depends on electrons BTBT from the valance band (VB) of degenerate p + source to the conduction band (CB) of the channel in presence of positive gate voltage (Bhuwalka et al. 2004; Ionescu 2008; Agarwal et al. 2010; Asra et al. 2011; Ionescu and Riel 2011; Verhulst et al. 2012). In this framework, we modify the SOI structure of U-shaped channel TFET (UTFET) (Wang et al. 2014) by extending the gate over the source pocket and propose a Gate-Extended-U-shaped channel TFET (GE-UTFET) structure. The proposed structure was simulated by means of santaurus technology computer added design (TCAD) (Sentaurus 2014) to investigate the DC and analog/RF performance. The performance of the UTFET and GE-UTFET are examined in terms of various parameter such as drain current (I_d), transconductance (g_m), subthreshold swing (*SS*), total gate capacitance (C_{gg}), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and RF FOMs like f_T and f_A.

The device structure and the methodology adopted for this study are elaborated in Sect. 2. The results of the investigation are present in Sect. 3. Finally, Sect. 4 concludes the study by summarizing important findings.

2 Device structure and methodology

The 2D schematic SOI structure of UTFET and GE-UTFET are shown in Fig. 1a, b respectively. Both the structures are identical except the extended gate over the source pocket region for GE-UTFET. Germanium source was used in the devices to improve the drive current due to its narrower bandgap as compared to silicon (Kim et al. 2009). Unlike planner TFET, the recessed gate is used in UTFET to increase the channel effective length. The line tunneling was incorporated in both the structures by introducing an L-shaped n + pocket region between the source and gate oxide (Wang et al. 2017; Cao et al. 2011; Abdi and Kumar 2014). The presence of both point tunneling (perpendicular to gate field) and line tunneling (parallel to gate field) enhance the ON-state current of GE-UTFET. Due to the extended gate over the pocket region the electric field increases in the region which induce

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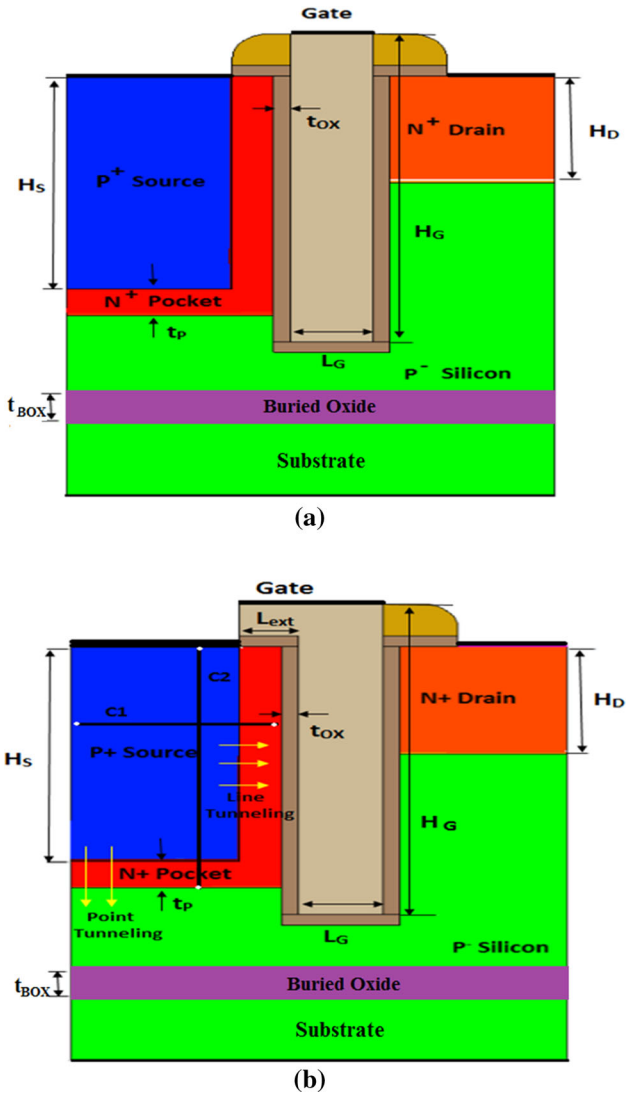


Fig. 1 2D schematic structure of **a** UTFET **b** GE-TFET

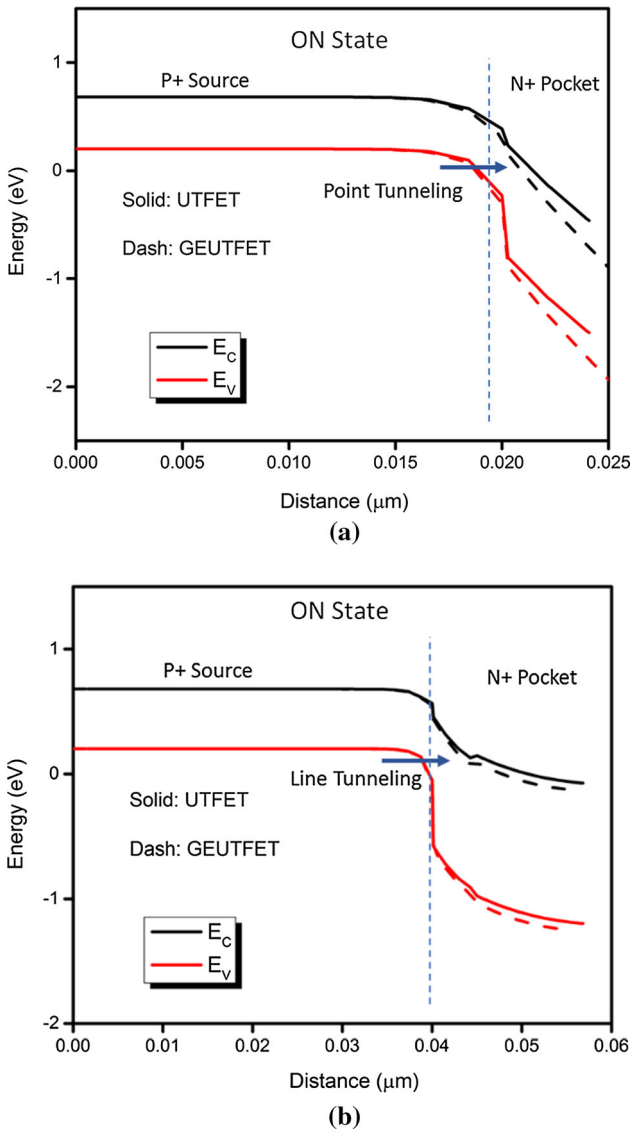


Fig. 2 Energy Band profile of GE-UTFET and UTFET along **a** C1 cutline and **b** C2 cutline at ON state

higher BTBT generation rate, and helps in increasing the drain current at ON-state for GE-UTFET. Figure 2a, b show the energy band profile of GE-UTFET and UTFET at ON-state. In GE-UTFET the gate length is extended up to L_{ext} in the source side so that it overlaps on the small n + pocket region. All the device parameters along with its dimensions are mentioned in Table 1. Gate material used in the structure was TiN with a work function of 4.66 eV. The drain doping ($N_d = 1 \times 10^{18}$ cm^{-3}) was kept lower than source doping ($N_a = 1 \times 10^{20}$ cm^{-3}) to restrain the ambipolar behavior (Narang et al. 2012). We studied the device performance of GE-UTFET for change in device geometric parameters like gate extension length (L_{ext}), pocket doping (N_p) and back gate voltage (V_{BG}) applied at the substrate.

Different physical models used in the simulation for this study were Dynamic non-local BTBT model, Fermi–Dirac

Table 1 Device parameter and dimension

Parameter	Dimensions
Gate length (L_G)	10 nm
Gate height (H_G)	60 nm
Source height (H_S)	40 nm
Drain height (H_D)	20 nm
Pocket thickness (t_P)	5 nm
Gate oxide (HfO_2) thickness (t_{OX})	3 nm
Substrate doping concentration	1×10^{19} cm^{-3}
Pocket doping concentration (N_p)	1×10^{15} cm^{-3}
Buried oxide (SiO_2) thickness (t_{BOX})	5 nm
Extended gate length (L_{ext})	7 nm

model, and doping dependent mobility model. Dynamic Non-local BTBT model with default parameter was included in the simulation for the non-local generation of electrons and holes and for a more accurate model of the tunneling process. Bandgap narrowing (BNG) model was used to incorporate the reduction in bandgap due to the high doping concentration in the semiconductor material.

Two cut-line C1 and C2 are considered at the source and pocket regions along the horizontal and vertical direction respectively to observe the tunneling phenomenon of the devices. The supply voltages used for this study were V_{DS} = 0.8 V, V_{GS} = 1.5 V. The back-gate voltage (V_{BG}) of 0 V is considered for the analysis unless stated differently. At OFF-state (V_{GS} = 0 V, V_{ds} = 0.8 V) there are no vacant states available in the CB of the pocket region i.e. the VB of the source region is lying above the CB of the pocket region. Hence, no BTBT occurs from source to pocket. Whereas, at ON-state (V_{GS} = 1.5 V, V_{DS} = 0.8 V) as evident in Fig. 2, the positive gate voltage shifts conduction band of pocket region downward. Thus conduction band crosses the valance band of the source region and electron starts tunneling from source to pocket. It is clearly visible from the band diagram that the tunneling is more in case of GE UTFET as compared to the UTFET as the vacant state available in the former is more due to enhanced band banding. The gate extension over the pocket region in GE-UTFET increases the electric field at the tunneling interface which leads to the enhancement in band banding and subsequently reduces the tunneling width. The electron BTBT from source to channel through the pocket region for GE-UTFET is shown in Fig. 3.

The Average SS was extracted using the following expression,

$$AvgSS = \frac{VT - Voff}{\log(IT - Ioff)} \tag{1}$$

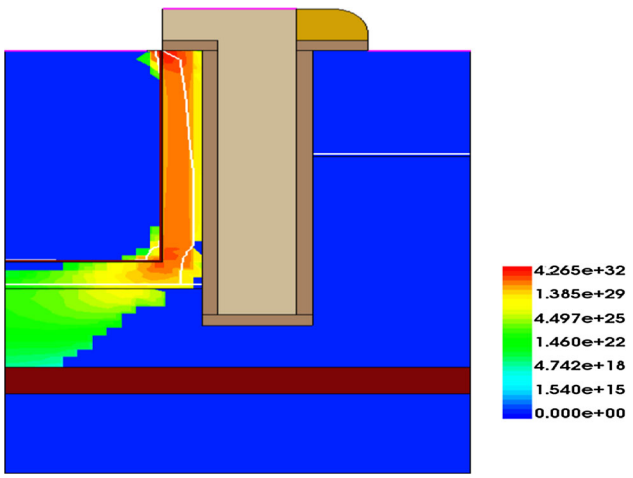


Fig. 3 Electron band to band tunneling (cm^{-3} s^{-1}) for GE-UTFET

where V_{off} signifies the gate voltage at I_{off}. The threshold voltage, V_T was extracted using the constant current method at $I_T = 1 \times 10^{-7}$ A. The important RF parameters f_T and f_A was extracted by performing small-signal analysis at 1 MHz. The frequency of unity current gain (f_A) and gain-bandwidth product or GBW (f_A) are expressed as (Vijayvargiya and Vishvakarma 2014),

$$fT = \frac{gm}{2\pi(Cgd + Cgs)} \tag{2}$$

$$fA = \frac{gm}{2\pi 10Cgd} \tag{3}$$

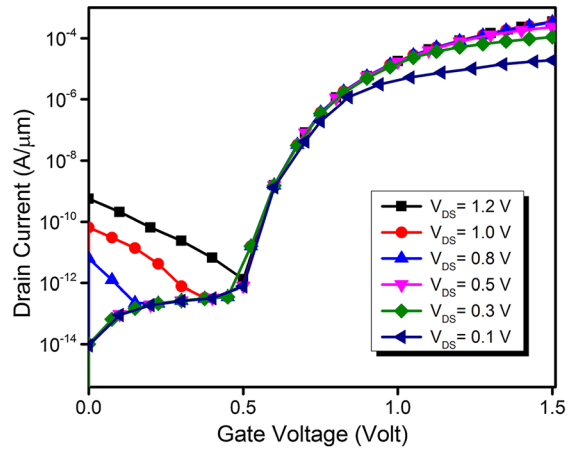
3 Results and analysis

The performance evaluation is done by both DC and analog performance analysis of the devices. The DC performance of UTFET and GE-UTFET are discussed in Sect. 3.1. The analog/RF performance in terms of C_{gg}, C_{gs}, C_{gd}, $f_{T,}$ and f_A is examined in Sect. 3.2.

3.1 DC performance of GE-UTFET

Transfer characteristics curve for different drain voltages ranging from 0.1 V to 1.2 V is depicted in Fig. 4a. It is observed that both the ON and OFF-state current increases with an increase in drain voltage. The ambipolar current increases with drain voltage due to increase in drain to source tunneling. It is observed from Fig. 4b that as the extended gate length (L_{ext}) over the pocket region increases, the ON current also increases. It is attributed to the increase in electric field at source pocket interface which in turn enhance the band banding at the tunneling interface. The variation of transfer characteristics with the n^+ pocket doping concentrations (1×10^{17} cm^{-3} to 1×10^{19} cm^{-3}) keeping other parameters constant for GE-UTFET is shown in Fig. 4c. It is evident that the increase in the doping concentration of n^+ pocket increases I_{on} of the device due to easier formation of inversion at the pocket region. But the off-state leakage current almost remains same with changing pocket doping concentration.

The effect of back-gate voltage (V_{BG}) on the transfer characteristics are studied for Bulk (Yang 2016) and SOI structure of GE-UTFET. It is clear from Fig. 5 that back gate voltage (V_{BG}) has no impact on the SOI structure because of the BOX layer at the device. But for bulk structure it affects the OFF-state leakage current as well as threshold voltage of the device. However, it does not influence the ON-state of the device. For $V_{BG} = -1$ V, the I_{off} degraded to the order of 10^{-9} A/μm as compare with the $\sim 10^{-13}$ A/μm at V_{BG} = 0 V. While, in case of



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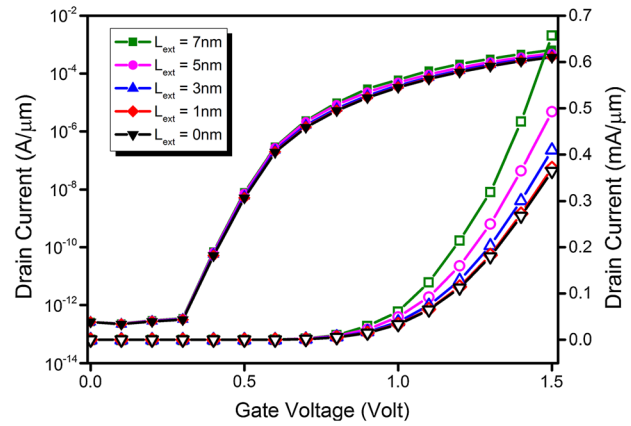

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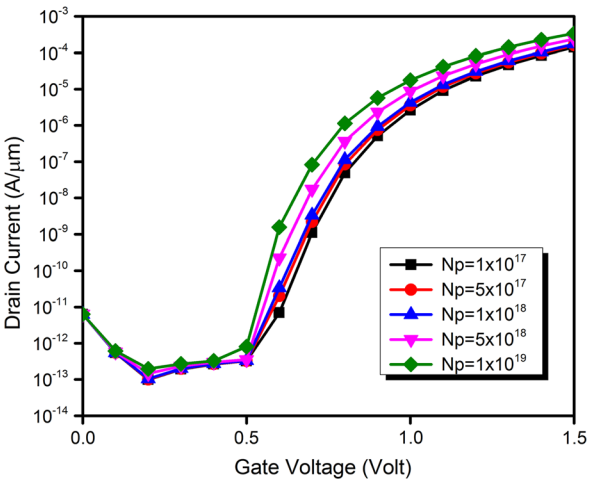
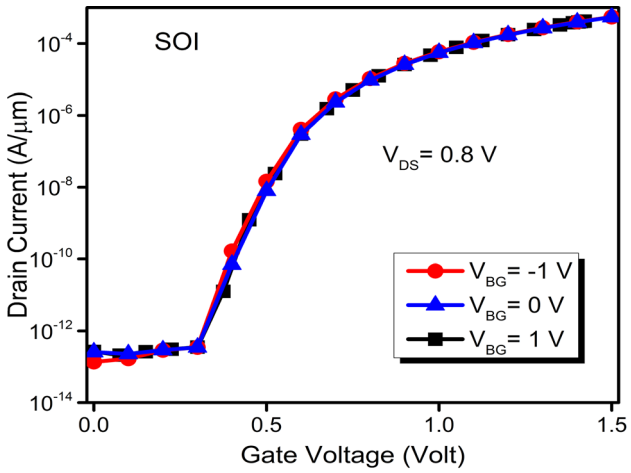


(c)

Fig. 4 I_D–V_G characteristics of GE-UTFET with a variation in **a** V_{DS}, **b** L_{ext}, **c** N_P



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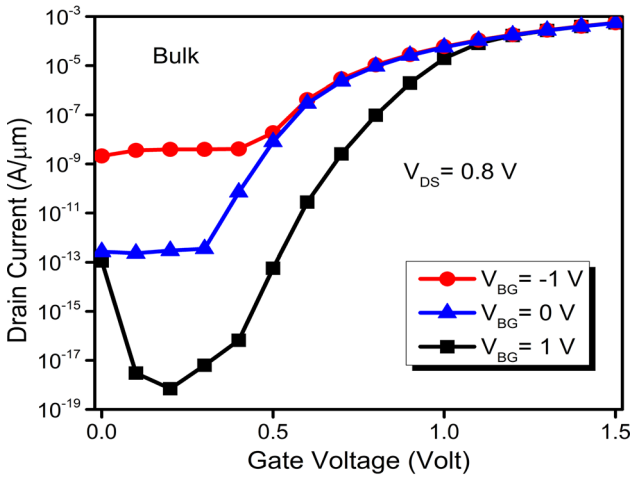


(b)

Fig. 5 Impact of back-gate voltage on **a** SOI GE-UTFET, **b** bulk GE-UTFET

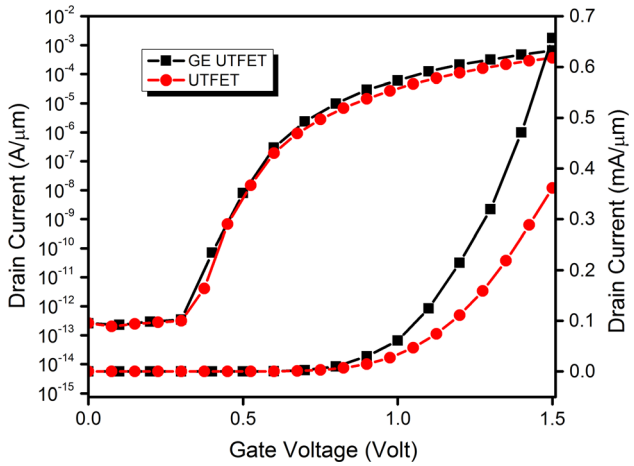


Fig. 6 Transfer characteristics for GE-UTFET and UTFET

V_{BG} = 1 V, the threshold voltage increases to 0.8 V from 0.55 V at V_{BG} = 0 V.

The transfer characteristics of GE-UTFET and UTFET is shown in Fig. 6 for both linear and logarithmic scale. On current of 6.57 × 10^{-4} A/μm is observed for GE-UTFET while UTFET gives an I_{on} of 3.61 × 10^{-4} A/μm. The

switching ratio, I_{off}, I_{on}, and average SS of UTFET and GE-UTFET are compared and listed in Table 2. An improved ON-state current and sub-threshold swing are observed in case of GE-UTFET as compared with the UTFET.

The variation of transconductance with V_{GS} at V_{DS} = 0.8 V has been analyzed for both the devices. A better result of g_m for the proposed structure as compared to UTFET is clearly visible from Fig. 7. The output characteristic of GE-UTFET and UTFET at different gate voltage (V_{GS} = 0.8 V and 1.0 V) is depicted in Fig. 8. In GE-UTFET due to the extended gate over the pocket, the tunneling junction area experience more electric field result in more band bending and more current compared to UTFET.

3.2 Analog/RF performance of GE-UTFET

In this section, the analog/RF performances of the devices are examined in terms of C_{gg}, C_{gd}, C_{gs}, f_T, and f_A. The dependence of the total gate capacitance C_{gg} on the supply voltage leads to the difference in RF performances of the devices under consideration. C_{gg} which is a combination of C_{gd} and C_{gs} is extracted using small-signal AC simulation at 1 MHz (Yang et al. 2010).

At low gate bias, gate capacitance comprises of parasitic capacitance due to lack of inversion layer. But as the gate voltage increases the inversion takes place from drain to source side which enhances the gate capacitance with gate bias (Paill et al. 2004). C_{gd} constitutes a larger fraction of total capacitance in TFET due to high source-channel potential barrier. The reduction in the potential barrier at channel-drain interface with gate voltage increases the C_{gd} exponentially. The gate capacitance is dominated by C_{gd} at higher gate voltage. Figure 9 shows the variation of intrinsic capacitances (C_{gg}, C_{gs}, and C_{gd}) for GE-UTFET and UTFET with the gate voltage. It is clear from Fig. 9 that due to the extended gate over the pocket region C_{gs} increases which reduce the miller capacitance C_{gd} of GE-UTFET.

Figures 10 and 11 shows the variation of f_T and f_A characteristics of GE-UTFET and UTFET with gate voltage. The f_T which is a function of g_m and C_{gg} has been extracted using (2). It is evident from Fig. 10 that f_T increases with gate bias. It is attributed to the increased transconductance with the gate voltage as discussed earlier. f_T attains the maximum and then falls with gate voltage due to the mobility degradation (Hoyniak et al. 2013). A higher value of f_T is observed due to reduced C_{gd} in case of GEUTFET.

As evident from (3) another RF figure of merit f_A is proportional to the ratio g_m/C_{gd}. Hence, f_A increases with gate voltage because of the enhanced g_m and reduced C_{gd} as shown in Fig. 11. As the transconductance of GE-UTFET ($\sim 1.45 \times 10^{-3}$ S/μm) is higher than UTFET ($\sim 9 \times 10^{-4}$ S/μm), the f_A is larger in GE-UTFET. After attaining the peak, GBW decreases with higher gate voltage due to mobility degradation and parasitic capacitance.

Table 2 Performance comparison between GE-UTFET and UTFET

Performance parameters	GE-UTFET	UTFET
ON-state current (A/μm)	6.57×10^{-4}	3.61×10^{-4}
Off-state current (A/μm)	2.57×10^{-13}	2.61×10^{-13}
On/off ratio	2.5×10^{9}	1.3×10^{9}
Average SS (mV/dec)	50	52

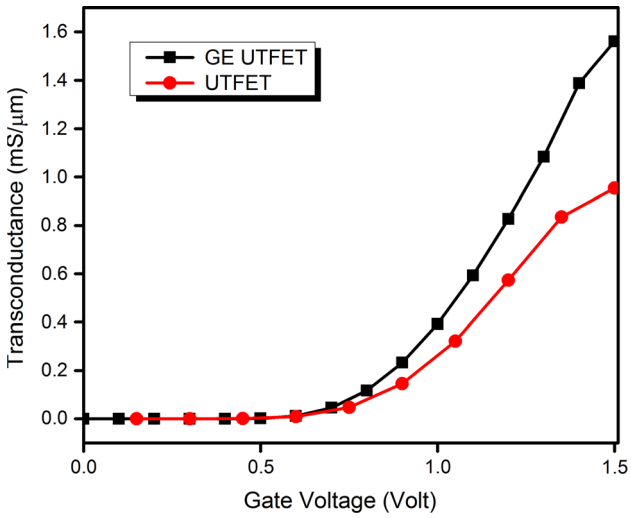


Fig. 7 Transconductance variation with gate voltage for GE-UTFET and UTFET

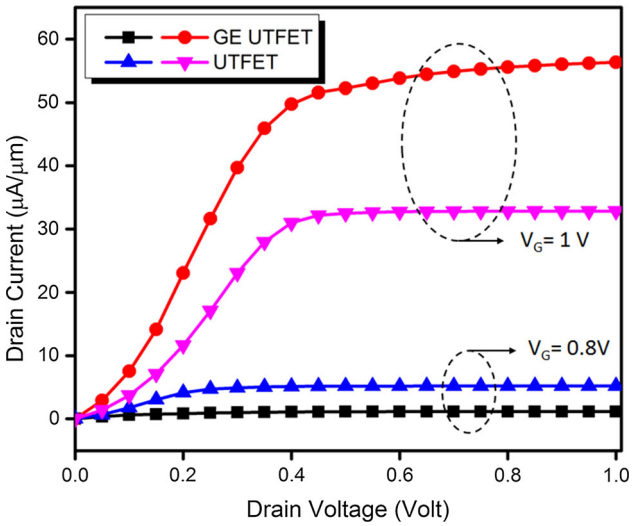
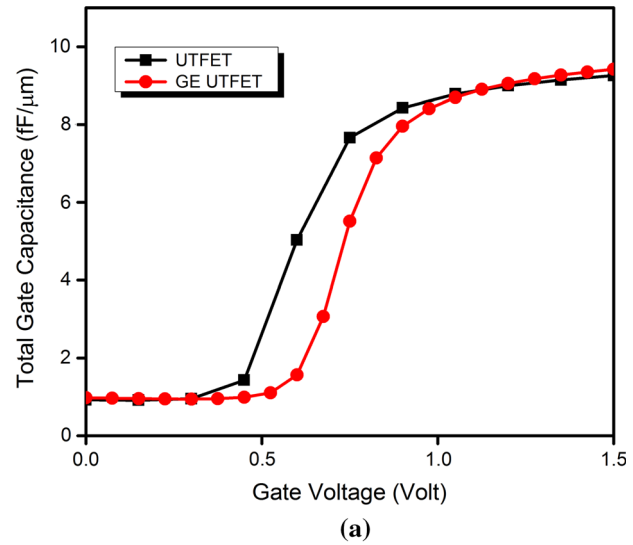


Fig. 8 Output characteristics of GE-UTFET and UTFET



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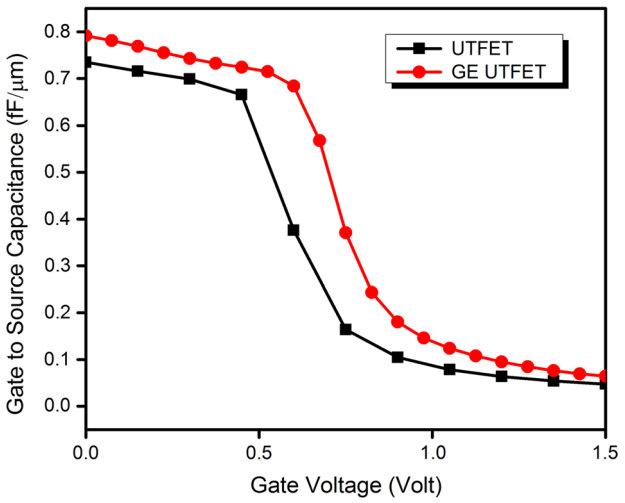

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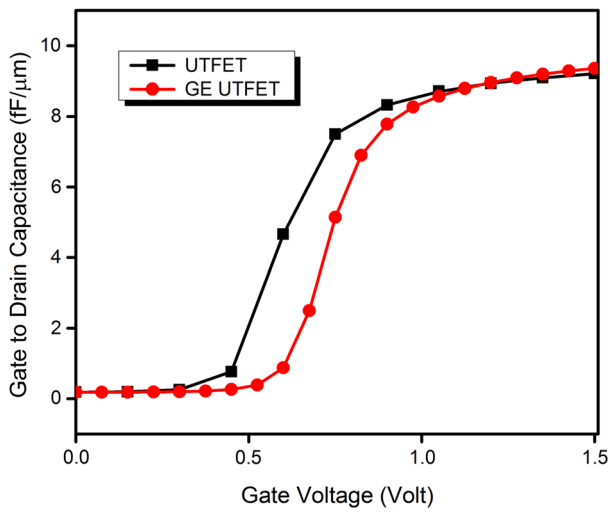

(c)

Fig. 9 Variation of **a** C_{gg}, **b** C_{gs} and **c** C_{gd} with gate voltage for GE-UTFET and UTFET

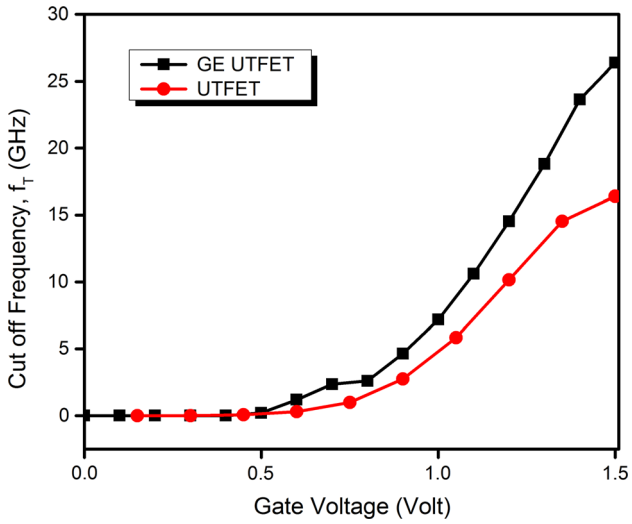

Fig. 10 Variation of f_T with gate voltage

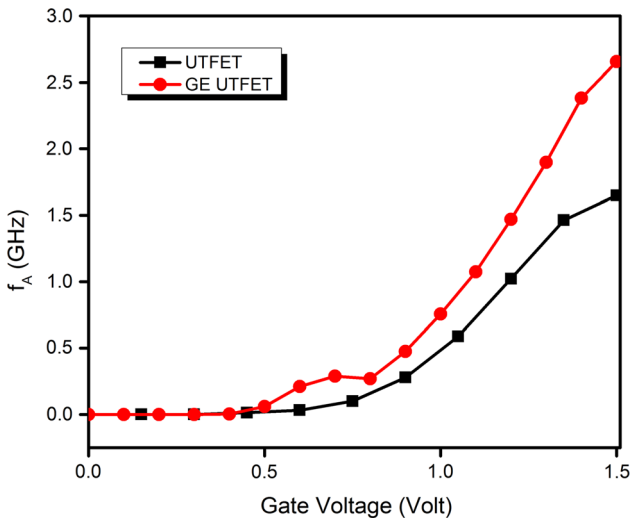

Fig. 11 Gain Bandwidth products (f_A) as functions of gate voltage

A significantly improved result of GBW is obtained for GE-UTFET.

4 Conclusion

The DC and RF performance comparisons of proposed structure GE-UTFET and UTFET are examined in this study by using Sentaurus TCAD tool. The simulation results reveal that a good average *SS* of 50 mV/decade and a switching ratio of the order of 10^9 are witnessed for GE-UTFET. Meanwhile, GEUTFET and UTFET show almost similar DC characteristics up to the gate voltage of 0.8 V. However, gradual differences are observed in their transfer characteristics for V_{GS} above 0.8 V due to the different electric field experienced by the pocket region. Due to the

lower miller capacitance and higher value of transconductance, the GE-UTFET have better frequency characteristics showing almost 62% more f_T and f_A than its counterpart UTFET. All the simulation results above demonstrate GE-UTFET is more suitable for a high-frequency application while comparing with UTFET. Furthermore, the role of back gate voltage on the electrical characteristics also demonstrated briefly in this paper.

It can be concluded from the results obtained in this study that the structural modification technique like gate overlap on source pocket can also be implemented to any TFET device with source pocket to enhance its analog and RF performance.

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