



# Investigation of electrical/analog performance and reliability of gate metal and source pocket engineered DG-TFET

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## Abstract

Although Tunnel Field Effect Transistors (TFET) offer low leakage current and allow good scalability, but they suffer from low ON-current. Present research paper focuses on the designing of an industry ready TFET that can operate efficiently at nano-scales allowing the fabrication of a smaller and more energy efficient overall device. To achieve the same, the Gate Metal Engineering (GME) and  $n^+$  Source Pocket (SP) schemes have been integrated on Double-Gate TFET (DG-TFET). For a distinct examination of the merits of GME and SP, 4 types of TFET architectures, namely the DG-TFET, GME-DG-TFET, SP-DG-TFET and GME-SP-DG-TFET (which amalgamates the merits of both GME and SP engineering) are investigated. All these device architectures are examined in terms of their electrical characteristics and analog parameters. GME-SP-DG-TFET (being superior among the four) is further analyzed under the presence of interface fixed charges (FC) of different polarity to affirm its reliability. Investigations of this device structure reveal that the positive FC are more noxious for the device as compared to negative FC. However, the enhanced flatband voltage under the negative FC translates to the high gate bias requirement to turn the device ON. Observance of only marginal variations in the parasitic capacitances and efficiency of the GME-SP-DG-TFET device in the presence of FC (both positive/negative) signifies its immunity and promises enhanced reliability. A remarkable improvement of the  $I_{ON}/I_{OFF}$  by two order of magnitude (from  $10^{10}$  to  $10^{12}$ ) and a decrease in  $V_{th}$  by 27.71% observed for GME-SP-DG-TFET as compared to DG-TFET along with the improved reliability makes the former an efficient candidate for low power analog/RF applications.

## 1 Introduction

Over the years, driven by industry for “smarter” products, engineers have continued to pack an ever-increasing number of transistors onto a single chip. In this process, engineers have had to not only develop novel fabrication techniques, but also make MOSFETs smaller. At the same

time, the demand to make CMOS devices smaller has led to a reduction in the physical size of the chip. This two-fold crunch necessitates the design of transistors with dimensions well within nano-scales. Shrinking of MOSFETs beyond a certain point, however, gives rise to certain phenomena referred to as Short Channel Effects (SCEs) that degrade the performance of the transistor (Madan et al. 2017b; Villalon et al. 2014). There is also an increase in the leakage current through the device, which adversely affects the use of such transistors in low-power applications. As these shortcomings of the MOSFET came to the foray, researchers began to look at new paradigms of transistor construction that are suitable for nano-scale operation. Among the devices proposed, the Tunnel FET (TFET) has emerged as a promising device attracting much research. This success of TFETs can be attributed to the fact that the primary source of drive current in TFETs is quantum mechanical Band-to-Band Tunneling (BTBT), which, being a quantum phenomenon, is prevalent at nano-scales (Biswal et al. 2017; Kumar and Raman 2019). This is contrasting to thermal carrier injection in MOSFETs which

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itself imposes certain physical limitations on the operation of the transistor. The construction of TFETs is similar to that of a MOSFET. A basic TFET is a four-region device with a source, channel, gate and drain. The source and drain are doped opposite to each other. TFETs work on the principle of BTBT of charged particles through the potential barrier at the source-channel interface. This mechanism makes the operation of TFETs at low supply voltages possible leading to lower static and dynamic power dissipation (Joshi et al. 2020). The key merits of the TFET are the low off current ( $I_{OFF}$ ), steeper subthreshold slope and process compatibility with the standard CMOS process flow (Choi et al. 2007; Nirschl et al. 2006).

As promising as the TFET may seem as a transistor candidate, it is far from being employable in modern electronics due to inherent complications in the device and the lack of focused R&D in the direction. A significant roadblock in such use of TFETs is the lower ON-state current ( $I_{ON}$ ) and considerably large miller capacitance as compared to MOSFETs because of inefficient BTBT. Several researchers have reported various device/material engineering schemes to overcome the challenges of TFET. To reduce the miller capacitance and simultaneously to enhance the  $I_{ON}$ , Lu et al. explored a drain current and capacitance model of hetero gate dielectric TFET (Lu et al. 2018). The tunneling current can be enhanced by greater overlapping of the valence band on the source side and conduction band on the channel side (Wei et al. 2018). Kim et al., have fabricated a DG TFET with vertical channel inserted between lightly doped Si and reported a SS of 17 mV/decade with  $I_{ON}/I_{OFF}$  ratio of  $10^4$  (Kim et al. 2019). Li et al., have also fabricated a vertical TFET with a p-type SiGe pocket near the source side and reported  $I_{OFF}$  of 100 pA/ $\mu\text{m}$  (Li and Woo 2020). Besides, currently, the temperature dependence of analog performance, linearity and harmonic distortion for a Ge-Source Tunnel FET has been investigated by Datta et al. (2020). In their work, they have incorporated the source bandgap engineering to conquer the challenges of TFET, and have also reported the temperature robustness comprehensively. Additionally, Joshi et al. have proposed an extended source DG TFET intending to enhance the analog/RF performance of TFET. Their work reports threshold voltage of 0.42 V, subthreshold swing of 12.24 mV/decade,  $I_{ON}/I_{OFF}$  of  $2.57 \times 10^{12}$ , cut off frequency 37.7 GHz, and gain-bandwidth product of 3.4 GHz (Joshi et al. 2020). Among all, the source pocket in the channel near source side is the most effective engineering to enhance the band bending at the tunneling junction in TFET (Nagavarapu et al. 2008). The source pocket is a region of highly doped semiconductor between the source and channel that causes abrupt band bending at the source-channel interface. As a result, the energy levels of the conduction band of the channel are

pulled closer to those in the valence band of the source, increasing the probability of electron tunneling through the device (Madan and Chaujar 2017b). The source pocket, along with gate stacking and gate underlapping engineering has been amalgamated on cylindrical gate TFET by Singh et al., to improve the electrical/RF performance of TFET (Singh et al. 2020). However, in this work, an  $n^+$  source-pocket is used for this purpose, resulting in an  $n^+$  Source Pocket TFET (SP-TFET). The  $n^+$  pocket causes improvement of  $I_{ON}$ , reduction in  $V_{th}$  and enhancement of the current switching ratio (Madan and Chaujar 2017a).

Another bottleneck of TFET is caused by the asymmetrical source/drain doping, which results in severe ambipolar conductivity, allowing TFETs to conduct current under both positive/negative gate bias (Wang et al. 2004). Solution to this problem is to engineer the gate in such a fashion that the band bending must be smaller (larger tunneling barrier) near the drain side. The large tunneling width at the drain channel junction makes it more difficult for electrons to tunnel at a negative gate bias, subsequently lowering the ambipolar current. To accomplish this, an engineering technique referred to as Gate Metal Engineering (GME) has been reported (Cui et al. 2011; Madan et al. 2017b). In GME, a metal with low/high value of work function is used near the source/drain side. The lower work function of metal reduces the flat band voltage ( $V_{fb} = \phi_M - \phi_S$ ) and thereby enhances the effective gate bias ( $V_{eff} = V_{gs} - V_{fb}$ ) at the tunneling junction. The enhanced  $V_{eff}$  increases the  $I_{ON}$  (due to reduction in tunneling barrier width at the source-channel interface) and also reduces the  $V_{th}$ . Likewise, the metal towards the drain side with comparatively higher work function controls the  $I_{OFF}$  and ambipolar conduction by broadening the barrier width at the drain-channel interface (Madan et al. 2017a).

Generally, in most of the research work, the Si/SiO<sub>2</sub> interface is treated as ideal (with no defects), however during the fabrication (owing to the stress and radiation induced damages) the interface is caused by mobile/fixed trapped charges. These charges effectively act as positive/negative fixed charges (FC) depending on their energy levels in the semiconductor bandgap. If a defect state is neutral and becomes positive/negative after donating/accepting an electron it is considered as a donor/acceptor state or a positive/negative FC (Madan and Chaujar 2017b, 2018; Qiu et al. 2014). The modification caused by the FC in the characteristics of the device will affect the functioning of the integrated circuit. Thus, to ensure the immunity of device against FC it is essential to investigate the characteristics of device under the presence of FC. Furthermore, GME confers another benefit on the TFET that is not immediately visible in the utopian scenario presented by simulation environments. It has been earlier seen that the application of the GME scheme makes the

transistor more immune to the presence of Interface Fixed Charges (IFCs) at the SiO<sub>2</sub>–Si interface at the tunneling interface (Madan et al. 2017c). This improved immunity against IFCs directly translates to improved reliability of the device. Often the reliability of transistors is simply associated with certain physical phenomena like electromigration that play a role only after the device comes into operation. The appearance of IFCs at the SiO<sub>2</sub>–Si interface begins right at the time of fabrication and adversely impacts device reliability by creating intermediate energy levels that serve as transient states for tunneling electrons (Cao et al. 2011). Improved fabrication techniques have led to a significant reduction in the density of IFCs, but their elimination appears to be a physical impossibility. In any realistic device, it becomes essential to minimize the impact of FCs on the performance of the transistor by means of device design and engineering (Sant et al. 2016). Therefore, much like figuratively hitting two birds with one arrow, the GME scheme incorporated in this work helps to control both drain current and device reliability.

This work attempts to remedy the aforementioned shortcomings of TFETs without depriving the device of the improvements it had achieved over the other transistor candidates, often even improving upon its overall performance. The primary motivation behind this work is to design a transistor that is an inch closer to an industry ready transistor candidate and can simultaneously operate efficiently at nano-scales allowing the fabrication of smaller, more energy efficient devices. The paper is ordered as: Section II describes the device structure, simulation methodology and the calibration of our simulation setup (models), section III deals with results obtained by numerical simulations, and the explanations thereof. A number of performance parameters and industry standard FOMs have been used to analyze the viability of the use of the proposed devices for practical applications. Broadly, the result section is divided into two subsections: the first analyzing the electrical/analog performance of DG-TFET by integrating SP and GME engineering schemes, and the second investigating the device reliability in terms of FC. Finally, conclusions drawn in section IV indicate that the proposed Gate Material Engineered Source Pocket DG TFET (GME-SP-DG-TFET) is a viable device for low power, high-frequency operations.

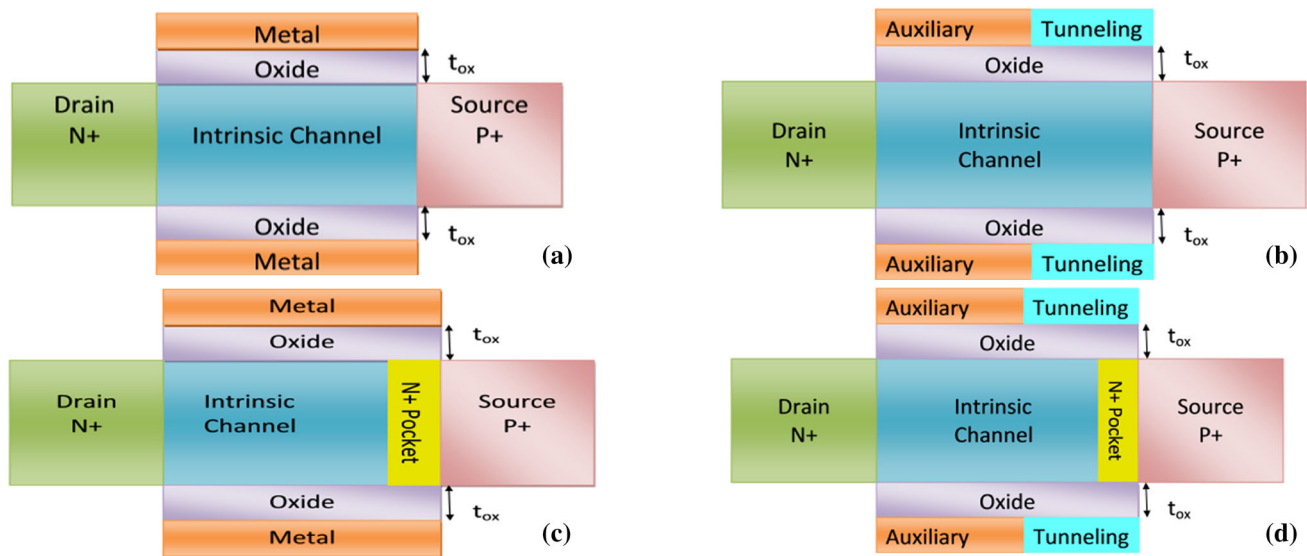
## 2 Device architecture and simulation methodology

In this work, four different architectures of double gate Tunnel-FET (DG-TFET) have been considered for performance comparison. The four different structures are Double Gate TFET (DG-TFET), Gate Material Engineered

DG TFET (GME-DG-TFET), n<sup>+</sup> Source Pocket DG TFET (SP-DG-TFET) and Gate Material Engineered Source Pocket DG TFET (GME-SP-DG-TFET). These devices are referred to as D1, D2, D3, and D4 respectively in this paper, and their schematic architectures are shown in Fig. 1a–d. In GME-DG-TFET, i.e., D2, both the gate metals (top and bottom) are engineered with dual material, i.e., with different metal work functions. Precisely, the GME scheme incorporates the lower metal work function near source side (tunneling gate) and comparatively higher metal work function near the drain side (auxiliary gate). Additionally, the SP-DG-TFET, i.e., D3 implants, a n<sup>+</sup> pocket near source side in the channel. Subsequently, the architecture that integrates the merits of GME and SP, i.e., GME-SP-DG-TFET referred as D4 comprises both, gate material engineering and also n<sup>+</sup> source pocket engineering. The source pocket width and doping concentration, in the n<sup>+</sup> source pocket engineering, are optimized for optimum I<sub>ON</sub>/I<sub>OFF</sub>, to 4 nm and  $2 \times 10^{19} \text{ cm}^{-3}$  respectively (Madan and Chaujar 2017b). Further, the work function for tunneling gate (gate near the source) is 4.1 eV and that for the auxiliary gate is 4.3 eV in case of GME, again tuned to achieve an optimized I<sub>ON</sub>/I<sub>OFF</sub> ratio (Shekhar et al. 2018). Additionally, for GME, the tunneling and the auxiliary metal gate length is 10 nm and 40 nm respectively. Furthermore, source (p<sup>+</sup>) and drain doping (n<sup>+</sup>) has been kept  $1 \times 10^{20} \text{ cm}^{-3}$  and  $5 \times 10^{18} \text{ cm}^{-3}$  respectively, for each of the proposed structures (D1 to D4). The thickness of the oxide (SiO<sub>2</sub>) layer is 2 nm for all the devices.

Further, to account the influence of FC, equivalent positive/negative charges are considered at the Si/SiO<sub>2</sub> interface in the simulated device architecture. The value of FC density, i.e., N<sub>f</sub> is selected on the basis of several experimental reported data that incorporates process damage and radiation damage (Madan and Chaujar 2016; Pala et al. 2012; Sant et al. 2016). The literature shows that the FC density varies in the range of  $10^{11}$ – $10^{13} \text{ cm}^{-2}$  (Jiao 2009; Lho and Kim 2005; Poindexter 1989; Trabzon and Awadelkarim 1998). Thereby, to investigate the influence of FC, the FC of different polarity (positive/negative) is considered in the channel region only near the source side (up to 10 nm from source side), as the FC are generated majorly at the region where there is a high electric field (Madan and Chaujar 2017b, 2018). Additionally, in the simulation setup, the INTERFACE statement is used to specify the FC density and position (at the Si/SiO<sub>2</sub> interface) of the FC.

All the simulations have been carried out using the TCAD SILVACO ATLAS device simulator (SILVACO 2011). The models incorporated in simulations are nonlocal BTBT model, bandgap narrowing model (BGN), Shockley–Read–Hall (SRH) recombination model, concentration and field dependent mobility model (CONMOB). Further,

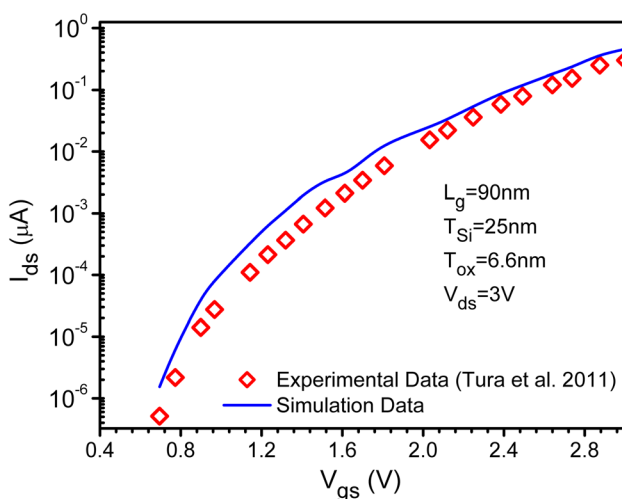


**Fig. 1** 2D device structure used in simulation **a** double gate TFET (DG-TFET) D1, **b** gate metal engineered double gate TFET (GME-DG-TFET) D2, **c** source pocket double gate TFET (SP-DG-TFET) D3, and **d** GME-SP-DG-TFET, D4

the Fermi–Dirac statistics and the conventional drift–diffusion model have been used. To perform the realistic study, models used during simulations are calibrated with experimentally reported work (Tura et al. 2011), i.e., a vertical DG-PNPN-TFET. To validate the simulation models the parameters of the nonlocal BTBT model (i.e., the prime essential model for TFET) is calibrated. In order to fine match the transfer characteristics of the simulated data with the experimentally reported data (Tura et al. 2011), the electron and hole effective mass are tuned to  $0.22m_0$  and  $0.51m_0$  from their defaults values of  $0.322m_0$  and  $0.549m_0$  respectively; where  $m_0$  indicates the electron rest mass. Figure 2 depicts the calibrated transfer characteristics of our simulated setup with the published

experimental work of (Tura et al. 2011) and thereby validates the simulation setup.

The proposed device, i.e., Gate metal and source pocket engineered DG-TFET, can be realized experimentally. However, none of the literature reports the fabrication of the discussed device solely. Therefore, the proposed device can be realized as per the techniques mentioned in the literature. The  $n^+$  source pocket DG TFET can be fabricated as discussed by Tura et al., where authors utilized molecular beam epitaxial (MBE) growth with a low thermal budget vertical process flow (Tura et al. 2011). After MBE, the hard mask of nitride is deposited and patterned for silicon wall etching to define the vertical channel, followed by gate oxidation using plasma-assisted oxidation. After that, the poly gate is deposited and etched along with the removal of the nitride spacer. Thereafter, an isolation oxide is deposited and planarized, followed by the deposition and patterning of the polysilicon gate metal. Besides the formation of  $n^+$  source pocket in the proposed device i.e., Gate metal and source pocket engineered DG-TFET, a hetero material gate has to be deposited. Thus, to process the gate metal engineering (or to deposit the auxiliary and tunneling gate), the metal interdiffusion technique (Polishchuk et al. 2001), or the fully silicide metal gate structure (Liu et al. 2005), or metal wet etching process (Zhang et al. 2005), or the laterally joined two metal gate structure (Long et al. 1999) or the chemical mechanical processing technique (Guillaumot 2002) can be used.



**Fig. 2** Transfer characteristics calibration with experimental data reported in Tura et al. (2011)

### 3 Results and discussion

#### 3.1 Device comparison: electrical/analog performance

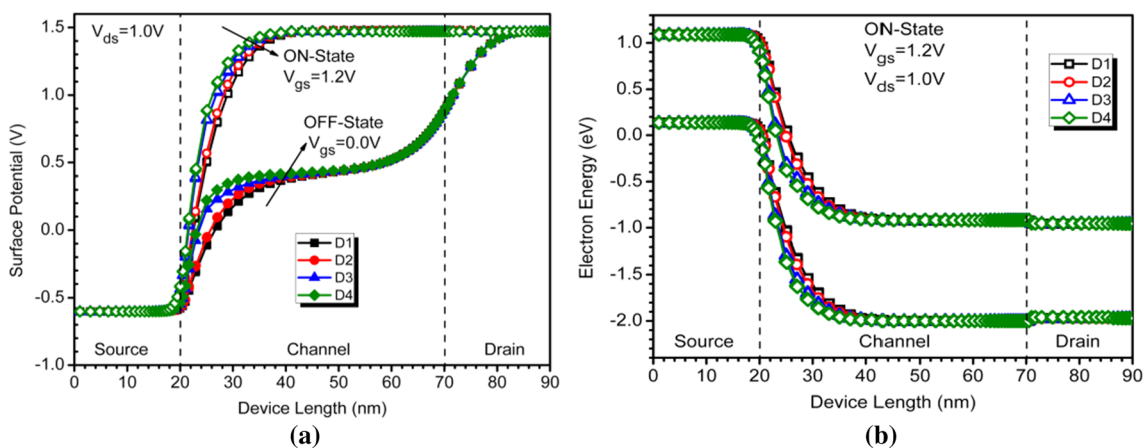
In this subsection, the electrical and analog performance of the devices under considerations labeled as D1, D2, D3, and D4 are analyzed. To examine the electrical/analog performance of the devices, surface potential, energy bands, electric field, transfer characteristics, output characteristics, threshold voltage, Subthreshold swing, current switching ratio, and device efficiency are investigated.

The surface potential of the four devices under consideration, i.e., D1, D2, D3 and D4 in both ON and OFF states are depicted in Fig. 3a. It is evident that the surface potential of all the devices (in the channel region) is higher in the ON state. Further, the D4 has a higher potential at the tunneling junction followed by D3, D2, and D1. The higher potential of D2, i.e., GME-DG-TFET is attributed to the existence of tunneling gate metal (lower work function metal) near the tunneling junction. This lower workfunction of the tunneling gate reduces the  $V_{fb}$  and thereby enhances the  $V_{eff}$  under it, i.e. at the tunneling junction (Saurabh and Kumar 2011). The increase in  $V_{eff}$  results in the higher surface potential of D2 as compared to D1. Moreover, for D3, i.e., SP-DG-TFET, the implantation of  $n^+$  source pocket in the channel near source side results in thin depletion layer at the source pocket junction (Nagavarapu et al. 2008). Thereby, the surface potential increases for D3 in comparison with D1. Furthermore, the integration of GME and SP collectively, i.e., GME-SP-DG-TFET (D4) shows superior surface potential among the 4 devices. The superior surface potential of D4 is mainly offered by the aggregated effect of GME and SP.

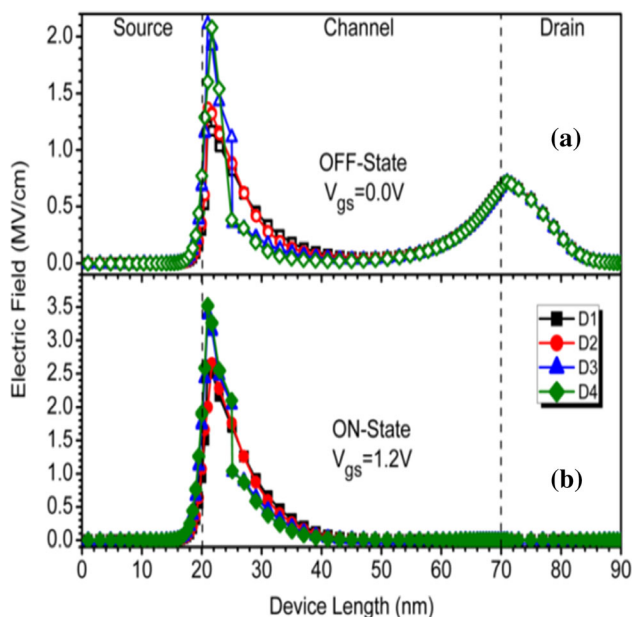
Figure 3b represent the energy of the electron along the length of the channel when the device is in the ‘ON’ state

for all the four devices. It is analyzed from the plot shown in Fig. 3b that all the devices under consideration have narrow tunneling barrier. The graph also depicts that the band bending is steepest in case of D4, followed by D3, D2 and lastly D1. The steeper band bending in D2 is offered by the tunneling metal gate that is of low metal work function. The low work function of tunneling gate enhances the surface potential and thereby results in steeper band bending as depicted in Fig. 3b. Further, in D3, it is the  $n^+$  SP that allows steeper band bending, between the source and source-pocket. Subsequently, in D4, there is the collective effect of GME and SP, that translates to the steepest band-bending as compared to all other devices.

Figure 4a, b depicts the electric field for the four considered devices D1, D2, D3 and D4 along the length of the channel in the OFF ( $@V_{gs} = 0.0 \text{ V}$  and  $V_{ds} = 1.0 \text{ V}$ ) and ON-state ( $@V_{gs} = 1.2 \text{ V}$  and  $V_{ds} = 1.0 \text{ V}$ ) respectively. It is clearly illustrated in Fig. 4a and b, that for each device at the tunneling junction, the electric field in the ON-state is higher than the OFF state. The high value of an electric field in the ON state is due to the contribution of the external electric field coming into existence due to gate bias that adds to the internal existing electric field (across the source-channel interface for D1, D2 or source-pocket interface for D3, D4). As such it results in a more strong electric field  $\sim 3.5 \text{ MV/cm}$ , whereas, in the absence of the gate bias, the diffusion of charged particles due to the concentration gradient results in the comparatively low internal electric field. Furthermore, in the ON as well as OFF state, the electric field is maximum in case of device D4, followed by D3, D2, and D1. The highest electric field in D4 is due to the steeper bending (discussed in Fig. 3b) offered by the collective effect of SP and the low work function of the tunneling gate. Moreover, it is also illustrated that the electric field at the drain channel junction is lower in case of ON state as compared to OFF state. The



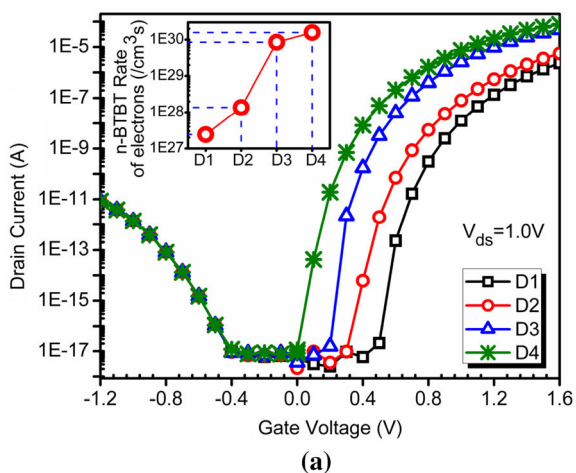
**Fig. 3** **a** Surface Potential along the device length at  $V_{gs} = 0.0 \text{ V}$  (OFF-state) and  $V_{gs} = 1.2 \text{ V}$  (ON-state) at  $V_{ds} = 1.0 \text{ V}$ . **b** Energy band diagram along the device length at  $V_{gs} = 1.2 \text{ V}$  (ON-state) at  $V_{ds} = 1.0 \text{ V}$  for all the devices under consideration



**Fig. 4** Electric field along the device length at **a**  $V_{gs} = 0.0$  V (OFF-state) and **b**  $V_{gs} = 1.2$  V (ON-state) at  $V_{ds} = 1.0$  V for all the devices under consideration

lower electric field at the drain-channel interface in ON state is attributed to the reduced drain channel potential barrier with rising  $V_{gs}$  (Boucart and Ionescu 2007).

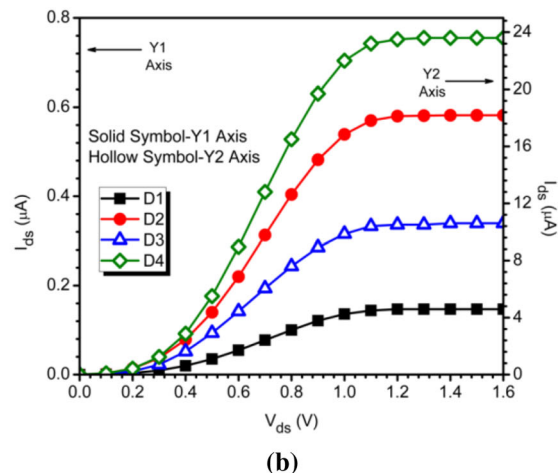
The number of electrons tunneling at the source channel (D1/D2) or the source pocket junction (D3/D4) per cubic volume per second is plotted in the Inset of Fig. 5a for all the devices under consideration in the ON-state. It is clearly presented that the BTBT rate of electrons for D4 ( $10^{30}/\text{cm}^3 \text{ s}$ ) is remarkably higher than D1 ( $10^{27}/\text{cm}^3 \text{ s}$ ). The higher BTBT rate of electrons of D4 is facilitated by the narrower barrier width (offered by the source pocket



**Fig. 5 a** Transfer characteristics of all the devices under concern, i.e., D1, D2, D3 and D4 at  $V_{ds} = 1.0$  V. INSET: Band to band tunneling rate of electrons ( $/\text{cm}^3 \text{ s}$ ) at the tunneling junction for D1, D2, D3 and

and lower metal work function of tunneling gate) that permits large number of electrons to tunnel at the tunneling junction. Further, it must be noted that the BTBT rate of D2 and D3 is lower than D4 by many orders. Figure 5a also represents drain current as a function of gate voltage for all the four n-channel devices under consideration keeping the drain-to-source voltage at 1.0 V. Primarily, as the gate voltage is gradually increased the band bending at the tunneling junction leads to narrowing of tunneling barrier width. This narrowing of the tunneling barrier (less than 5 nm) eventually enhances the drain current.

Furthermore, the graph depicts that at a particular value of positive gate bias, device D4 has the highest current followed by D3, D2 and then D1. The higher drain current of D4 is due to higher tunneling rate of electrons as depicted in the Inset of Fig. 5a. It is evaluated that the  $I_{ON}$  of D1 increases from  $10^{-7}$  A to  $10^{-5}$  A with the incorporation of GME and source pocket, i.e., for D4. Moreover, when the gate is negatively biased, there is band bending at the drain/channel interface causing ambipolar conduction. Furthermore, the ambipolar current is same for all the four considered devices and is also tabulated in Table 1. The similar ambipolar conduction is attributed to the fact that the drain/channel junction (that principally controls the ambipolar conduction) is same for all the devices (Wang et al. 2004). Since ambipolar current depends upon the effect of negative gate bias on the drain-channel interface (for n-TFET) which is same for all the four devices, this leads to more constant values of ambipolar current. Moreover, comparing with the existing literature, where a III–V staggered hetero-junction nanowire (NW) TFET is used to improve the ON-state current. It is investigated that the  $I_{ON}/I_{OFF}$  ratio of the device reported by Biswal et al. is only  $10^4$  (for Si) whereas, in our work (by integrating the



D4 in ON-state @  $V_{gs} = 1.2$  V and  $V_{ds} = 1.0$  V. **b** Output characteristics of D1, D2, D3, and D4 at  $V_{gs} = 1.2$  V

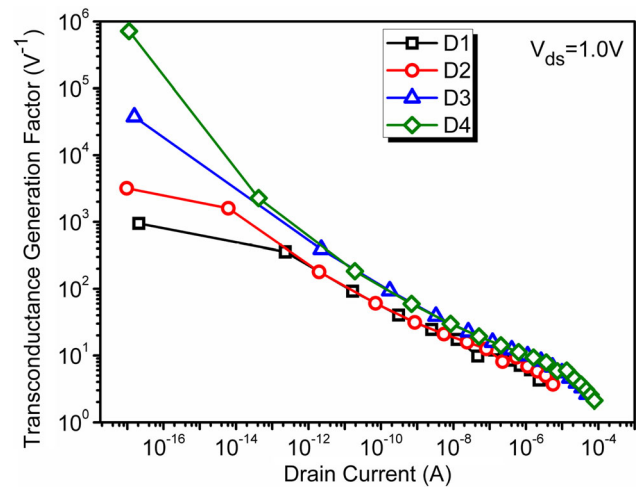
**Table 1**  $V_{th}$ , SS,  $I_{ON}/I_{OFF}$  and  $I_{AMB}$  of D1, D2, D3, and D4

Parameters device	$V_{th}$ (V)	SS (mV/decade)	$I_{ON}/I_{OFF}$	$I_{AMB}$ (A)
D1	0.86	24.74	$2.25 \times 10^{10}$	$8.53 \times 10^{-12}$
D2	0.82	35.64	$7.66 \times 10^{10}$	$8.53 \times 10^{-12}$
D3	0.71	19.39	$1.20 \times 10^{12}$	$8.49 \times 10^{-12}$
D4	0.62	27.96	$2.63 \times 10^{12}$	$8.49 \times 10^{-12}$

device engineerings) the  $I_{ON}/I_{OFF}$  ratio of  $10^{12}$  is achieved (Biswal et al. 2017). Figure 5b represents the output characteristics of all the devices at  $V_{gs} = 1.2$  V. To highlight the significant changes in  $I_{ds}$ , the values of D1 and D2 have been shown on Y1 axis while the same has been shown on Y2 axis for D3 and D4. The proposed D4 provides a drain current of the order of  $10^{-5}$  A in comparison to  $10^{-7}$  A being provided by D1 when both the devices have been put into similar operating conditions. This significantly large drain current of D4 (almost 2 order of magnitude greater than other conventional techniques) may have far-reaching positive consequences to circumvent the challenges faced by TFET.

Important electrical parameters, i.e., the threshold voltage ( $V_{th}$ ), current switching ratio ( $I_{ON}/I_{OFF}$ ) and the sub-threshold swing (SS), extracted from the transfer characteristics, have been tabulated in Table 1 for all the devices under considerations. In this work,  $V_{th}$  is evaluated as the  $V_{gs}$  at  $I_{ds} = 10^{-7}$  A, i.e., by the constant current method. It is clearly observed that the  $V_{th}$  of D4 is minimum. This minimum  $V_{th}$  of D4 is obtained by the higher tunneling rate that switches ON the device at lower gate bias. Further, the D3 provides the minimum SS among all the devices. However, the SS of D4 is still appreciably lower than the fundamental limit of MOSFET on the SS. Since  $I_{OFF}$  is almost same for all the four devices, the current ratio therefore predominantly depends on the  $I_{ON}$ .  $I_{ON}$  is found to be maximum in case of D4, leading to maximum current switching ratio in the case of D4, followed by D3, D2, and D1.

To provide an insight for the improvement of analog performance by a device in the sub-threshold region, device efficiency also known as transconductance generation factor (TGF) is one of the key figure of merit (FOMs) (Mallik and Chattopadhyay 2012). This device efficiency or TGF, defined as the ratio of transconductance ( $\partial I_D / \partial V_{GS}$ ) to drain current (i.e.,  $g_m/I_D$ ), is used to achieve the desired value of transconductance (speed) by effectively utilizing the current (power). Figure 6 illustrates the TGF of all the devices under consideration. It is clearly shown in Fig. 6 that the device efficiency of D3/D4 is considerably higher than that of D1/D2. It is evaluated that the device efficiency of D3/D4 is 2.31 times higher than D1/D2 @  $I_{ds} = 10^{-8}$  A. This enhanced device efficiency of D3/D4



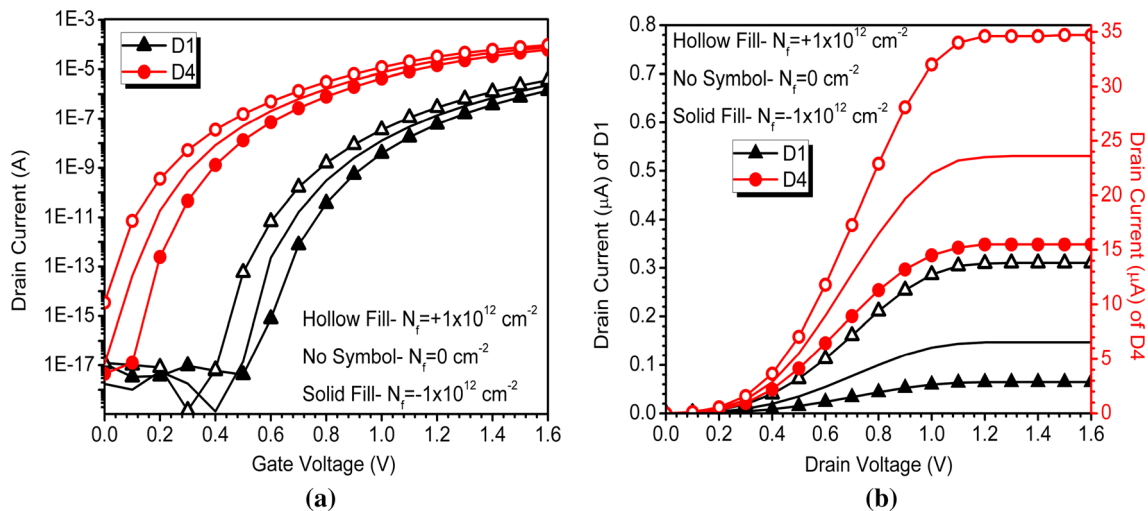
**Fig. 6** Transconductance generation factor of all the devices i.e., D1, D2, D3 and D4 at  $V_{ds} = 1.0$  V

is offered by the improved  $g_m$  and  $I_{ds}$  by integration of SP and GME engineering.

### 3.2 Influence of interface fixed charges (FC)

From Sect. 3.1, it is examined that the D4, i.e., the device with integrated SP and GME on DG-TFET, delivers the superior analog performance in comparison with its conventional counterparts, thus, in this subsection, the impact of FC on the device, D1 and D4, in terms of analog/RF performance has been investigated.

The BTBT at the source and channel/pocket junction for D1/D4 followed by the drift–diffusion of electrons results in drain current in TFET. Further, the band bending at the source and channel/pocket junction for D1/D4 becomes steeper with gate bias. To analyze the impact of interface FC on transfer characteristics, drain current of D1 and D4 under the presence of different polarity (negative/positive) FC is investigated and is depicted in Fig. 7a. Results clearly show that the presence of FC alters the device characteristics from their ideal expected values, i.e. for  $N_f = 0 \text{ cm}^{-2}$ . It is obtained that the positive/negative FCs increases/decreases the drive current. This variation in drain current with FC is due to the fact that the presence of positive/negative polarity FC reduces/enhances the flatband voltage ( $V_{fb}$ ) (in accordance with Eq. (1)), and thereby



**Fig. 7** **a** Transfer characteristics and **b** output characteristics of D1 and D4 depicting the impact of positive, negative and absence of FC

enhances/reduces the effective gate bias ( $V_{eff} = V_{gs} - V_{fb}$ ) in the channel.

$$\Delta V_{fb} = \frac{qN_f}{C_{ox}} \quad (1)$$

This enhanced/reduced  $V_{eff}$  at the tunneling junction enhances/reduces the drain current in DG-TFET. Moreover, it is obtained that the subthreshold current is highly impacted with these FCs as compared to the superthreshold regime for both the devices. It is evaluated that positive FC enhances the subthreshold current by many orders i.e., from an order of  $10^{-17}$  A to  $10^{-15}$  A. This considerably high increase in subthreshold drain current due to the positive FC degrades the device performance significantly. Further, it is clearly shown in Fig. 7a that the variations in drain current due to the positive/negative FC is appreciably reduced in D4 as compared to D1. This improved reliability in the superthreshold regime of D4 is attributed to the integration of GME and SP. The GME utilizes the lower work function metal near the source side and thus have a lower flatband voltage ( $V_{fb}$ ). This reduced  $V_{fb}$  with GME improves the device reliability of D1. Furthermore, the variations in output characteristics with FC for both the devices is shown in Fig. 7b. Results shows that the drain current decreases/increases for negative/positive FC. Its main reason is due to the positive FC reduces the  $V_{fb}$  and thereby enhances the effective gate bias in the channel. Further, it is evaluated for D1 that the drain current increases/decrease by 2.10/2.28 times with positive/negative FC. Additionally, the increase/decrease is 1.46/1.52 times for D4, this reduced variations in drain current is offered by the GME and SP engineering. Thus, the reduced variation in drain current for D4 signifies D4 as more reliable device against FC. Thus, along with improved analog/RF performance, D4 offers better reliability. The

impact of the presence of interface FC on the threshold voltage ( $V_{th}$ ), subthreshold swing (SS) and current switching ratio on D1 and D4 is tabulated in Table 2. As already discussed, that the  $V_{th}$  of D1 is considerably reduced with the integration of SP and GME, i.e., for D4. Further, the positive/negative FC reduces/enhances the  $V_{th}$  for both D1 and D4. This decrease/increase in  $V_{th}$  is attributed to the corresponding enhancement/reduction of drain current as described in Fig. 7a.

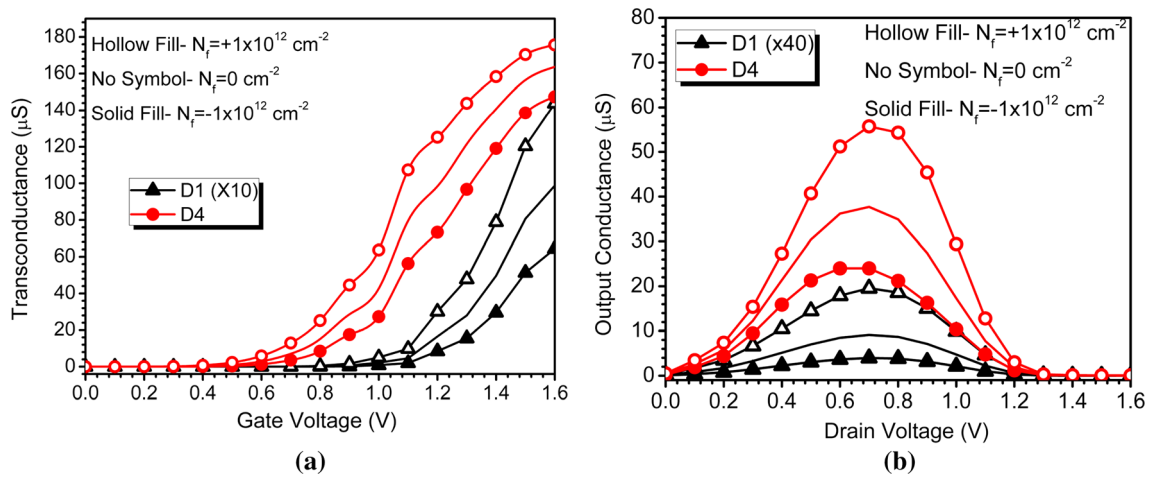
Further, it is analyzed that the positive FC degrades the SS significantly, owing to the increasing OFF-state current of the device as discussed in Fig. 7a. Further, the current switching ratio, i.e., evaluated as  $I_{ON}/I_{OFF}$ , increases/decreases for negative/positive IFC in the case of D4. For D4, the positive FC reduces the  $I_{ON}/I_{OFF}$  ratio by many orders owing to the considerably high degradation in the subthreshold region. However, the  $I_{OFF}$  in D4 is marginally reduced with negative FC that is translated in marginally enhancement in the  $I_{ON}/I_{OFF}$  ratio.

Figure 8a apparently depicts the variations in transconductance ( $g_m$ ) due to positive/negative FC in comparison with the case where there are no trap charges, for both the devices D1 and D4. It is evident from the plot that the  $g_m$  of D1 is considerably small than D4, that is essentially the reason that  $g_m$  of D1 is multiplied by 10 so as to display on the same scale. Further, the  $g_m$  of both D1 and D4 increases/decreases with the presence of positive/negative FC. This variation in  $g_m$  is similar to the drain current, as the  $g_m$  is the first order derivative of the drain current. Figure 8b depicts the variations in output conductance due to the presence of FC of different polarity on both D1 and D4. The higher drain current of output characteristics, in turn, makes the output conductance  $g_d$  higher for D4 in comparison with D1. However, the analog circuit designers demand low  $g_d$  device, to account for the higher intrinsic

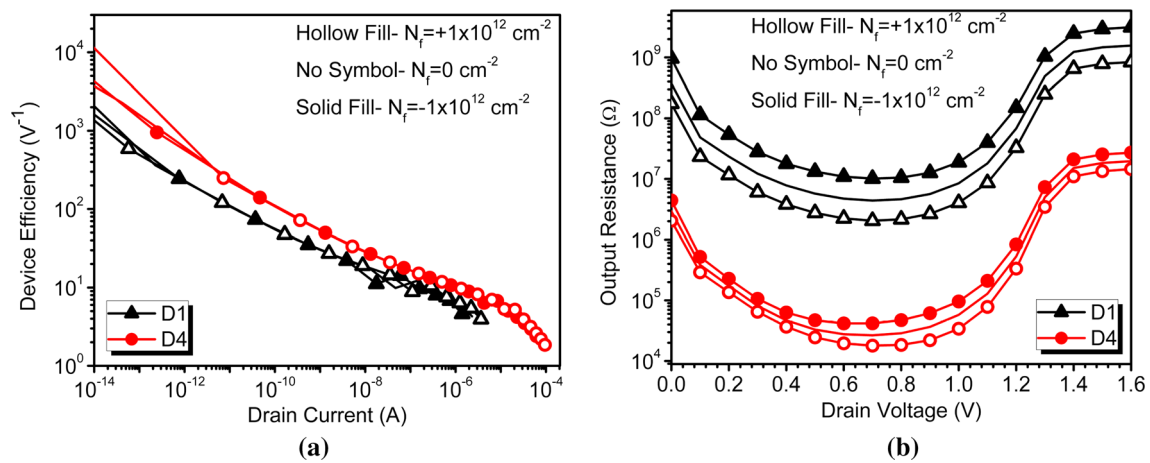


**Table 2** Variations in  $V_{th}$ , SS, and  $I_{ON}/I_{OFF}$  of D1, and D4 due to FC

Interface FC	Negative FC $N_f = -1 \times 10^{12} \text{ cm}^{-2}$	No FC $N_f = 0 \text{ cm}^{-2}$	Positive FC $N_f = +1 \times 10^{12} \text{ cm}^{-2}$
$V_{th}$ (V)			
D1	1.24	1.16	1.08
D4	0.61	0.53	0.45
SS (mV/decade)			
D1	33.37	14.57	25.32
D4	13.43	27.96	30.14
$I_{ON}/I_{OFF}$			
D1	$5.27 \times 10^9$	$7.79 \times 10^{10}$	$2.32 \times 10^{10}$
D4	$3.23 \times 10^{12}$	$1.97 \times 10^{12}$	$9.16 \times 10^9$



**Fig. 8** a Transconductance and b output conductance of D1 and D4 depicting the impact of positive, negative and absence of FC



**Fig. 9** a Device efficiency and b output resistance of D1 and D4, depicting the impact of positive, negative and absence of FC

gain  $A_v$ . Further, as described beforehand for output characteristics the  $g_d$  of both the devices increases/decreases for positive/negative FC.

Figure 9a shows the variations in device efficiency (i.e., the ratio of  $g_m$  and  $I_{ds}$ ), also known as transconductance

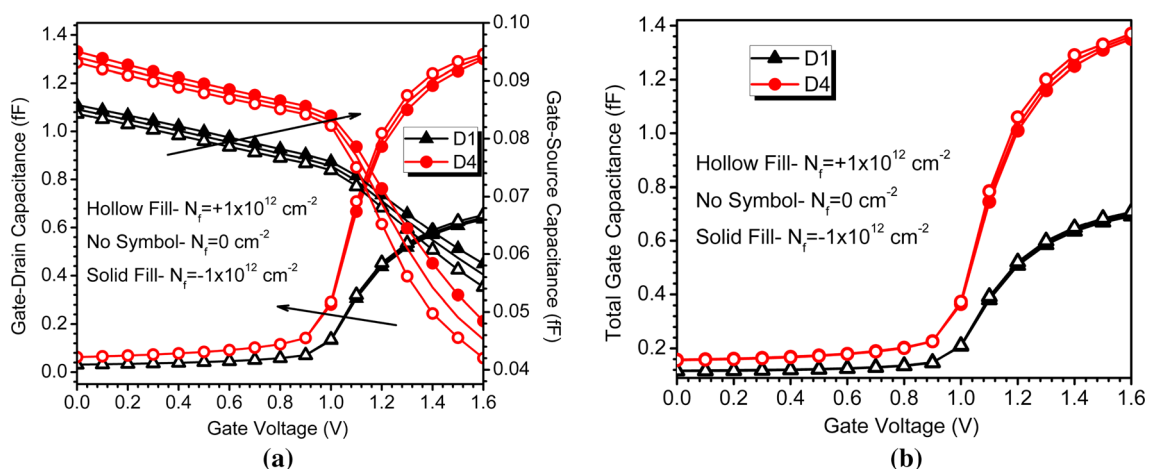
generation factor (TGF), of D1 and D4 due to the presence of FC. From the plot shown in Fig. 9a it is evident that at lower values of drain current, i.e. in the subthreshold region, TGF for D4 is high as compared to D1. This is because TGF has inverse reliance with the drain current

and in the sub-threshold region drain current is significantly small. So, initially, TGF is having its peak value and with an increase in drain current its value starts decreasing. Also, due to the increase/decrease in  $g_m$  and  $I_{ds}$  with positive/negative FC, discussed beforehand, device efficiency of both the devices increases/decreases with positive/negative FC. It must be noted that the impact of FC is only marginally on device efficiency. Apparently, from the plot, it is evident that TGF of both D1 and D4 TFET is very high of the order of  $\approx 10^4$  at the sub-threshold region, that is much higher as compared to MOSFET, with TGF limited to  $40 \text{ V}^{-1}$ . The plot in Fig. 9b, shows the impact of FC on the drain resistance or output resistance ( $R_{out}$ ) as a function of drain voltage. Output resistance is inverse of the output conductance ( $g_d = \partial I_D / \partial V_{DS}$ ). It is apparent from the plot that  $R_{out}$  of D4 is smaller in order as compared to D1. This is due to the fact that the conduction is higher in D4 as compared to D1 and output resistance is inverse of  $g_d$ . Additionally, the intrinsic gain ( $A_v = g_m / g_d$ ) directly depends on the transconductance which is directly related to TGF. So, higher value of TGF will compensate for lower value of output resistance in order to achieve high intrinsic gain. Further, the inverse reliance of  $g_d$  with  $R_{out}$  is responsible for the increase/decrease of  $R_{out}$  under the presence of negative/positive FC.

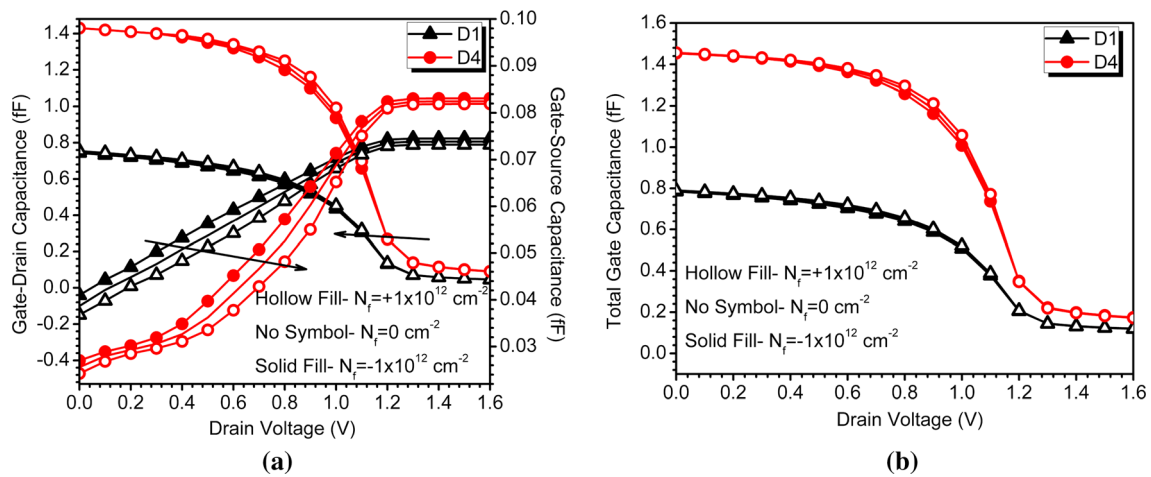
The impact of FC on the parasitic gate capacitances as a function of gate voltage is depicted in the plot shown in Fig. 10a, b. It is apparent from the results that the gate-source capacitance increase/decreases only slightly for negative/positive FC. Further, the parasitic capacitances of D4 are much higher than D1. This higher parasitic capacitance of D4 is due to the heavily doped SP. The low parasitic capacitance of any device is desirable as the parasitic capacitance has an inverse relation with the device speed and also with power dissipation (Mookerjea et al.

2009). Thus, the marginal variation in parasitic capacitances with FC signifies the immunity of devices against FC, and thereby indicates their reliability. Additionally, the plot indicates that initially gate-source capacitance ( $C_{gs}$ ) is dominant up to the threshold voltage and then gate-drain capacitance ( $C_{gd}$ ) takes the lead. This is because the formation of inversion layer will appear at the drain first and then it is extended towards the source region, which results in the reduction of coupling between the gate and source (Gnani et al. 2015). So, with increase in  $V_{gs}$ , the gate-source capacitance decreases. Further, the total gate capacitance ( $C_{gg}$ ) is the sum of the  $C_{gd}$  and the  $C_{gs}$ . From the plot shown in Fig. 10b it is evident that the attributes of total gate parasitic capacitance as a function of gate voltage is similar to the gate-drain capacitance. The similar plot of  $C_{gd}$  and  $C_{gg}$  is attributed to the dominant contribution of  $C_{gd}$  in case of TFET in comparison with  $C_{gs}$  (Mookerjea et al. 2010). This is clearly inferred from Fig. 10b that the parasitic capacitance changes marginally under the presence of FC, thereby signifies the device reliability.

The plot shown in Fig. 11a, b depicts the impact of the FC on the parasitic capacitances as a function of drain voltage. It is evident from the plots that the gate parasitic capacitances increase/decrease only minuscule with the positive/negative FC. For any device, these parasitic capacitances should be as minimum as possible because they lead to more power dissipation and also affects the speed of operation. Apparently, it is evident from the plot that the parasitic capacitance increases in D4 as compared to D1 due to the formation of channel/pocket junction, that add on to the total gate capacitance. At the lower values of drain voltage,  $C_{gs}$  is significantly small and increases with increase in the drain voltage. This is because for higher value of drain voltage the pinch-off of the channel occurs towards the source region. Vice versa is for  $C_{gd}$ , i.e.;



**Fig. 10** a Gate-drain capacitance, gate-source capacitance and b total gate capacitance of D1 and D4 as a function of gate bias, depicting the impact of positive, negative and absence of FC



**Fig. 11** **a** Gate-drain capacitance, gate-source capacitance and **b** total gate capacitance of D1 and D4 as a function of drain bias, depicting the impact of positive, negative and absence of FC

initially it has high value, and with increase in drain voltage it decreases (Mookerjea et al. 2009). This is due to the fact that with increasing drain voltage the coupling towards the drain also diminishes. Further, the total gate capacitance  $C_{gg}$  is analyzed for both the devices, under the presence of different FC and is shown in Fig. 11b. It is evident that the attributes of total gate parasitic capacitance as a function of drain voltage is similar to the gate-drain capacitance, owing to the considerably small  $C_{gs}$ . Further, the impact of FC is negligibly small on the parasitic capacitances showing the immunity of device against the FC.

For high-speed RF applications, the cut off frequency ( $f_T$ ) of device is the most desired design parameter which is directly related to the transconductance and inversely to the parasitic capacitances.  $f_T$  of the device is an important parameter to analyze the RF performance of any device and is evaluated by (Marjani and Hosseini 2015)

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2}$$

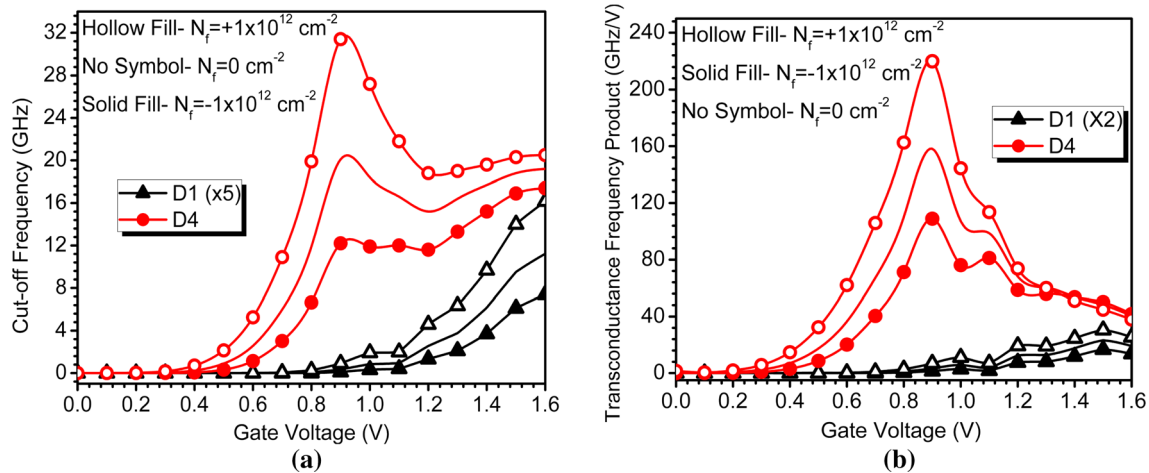
It is inferred from Eq. (2) that the higher parasitic capacitances may degrade the  $f_T$  of the device. In our study, it is realized that the integration of SP and GME engineering degrades the  $C_{gg}$  as discussed in Figs. 10 and 11, however, it also enhances the drain current considerably and thereby the  $g_m$  (depicted in Fig. 8a). The plot of  $f_T$  evidently shows that the degradation in  $C_{gg}$  (of D4 as compared to D1) is overpowered by the enhanced drain current (of D4 as compared to D1). This results in the considerable enhancement in  $f_T$  of D4 as compared to D1. Further, the impact of FC on  $f_T$  is also depicted in Fig. 12a that reveals that for both the devices the  $f_T$  increases/decreases due to the presence of positive/negative FC. This variation in  $f_T$  is similar to the variation in  $g_m$ , as

enhancement in  $g_m$  overpowers the variations in  $C_{gg}$ . It is evaluated that the increase/decrease in  $f_T$  is 79.89%/48.02% (in D1) and only 23.85%/23.89% (in D4) with positive/negative FC at  $V_{gs} = 1.2$  V. The reduced variations in  $f_T$  in D4 implies the better reliability of D4 in comparison with D1.

Another important parameter to inspect the device RF performance is the transconductance frequency product (TFP) i.e. primarily the product of  $f_T$  and the device efficiency ( $g_m/I_{ds}$ ). The variations in TFP for both the devices under presence of FC of different polarity is depicted in Fig. 12b. It is clearly shown in the Fig. 12b that the TFP of D4 is appreciably higher than D1 by many orders, attributed to the enhanced  $f_T$  and device efficiency of D4. This higher TFP possessed by D4 can be beneficial for moderate to high-speed device designs and is simultaneously good to maintain the linearity of the device (Pradhan et al. 2014). Moreover, the impact of FC on TFP is the communal effect of both device efficiency and the  $f_T$ . Thus, the TFP increases/decreases with the presence of positive/negative FC.

### 4 Conclusions and future work

In this work, the integrated merits of gate metal engineering and source pocket have been incorporated on DG-TFET to obtain GME-SP-DG-TFET. To insight the device physics the electrical/analog performance of GME-SP-DG-TFET along with its conventional counterparts, i.e., GME-DG-TFET, SP-DG-TFET, and DG-TFET have been examined by calibrated SILVACO TCAD setup. The investigation reveals that the collective merits of SP and GME outperforms its conventional counterparts and simultaneously considerably overcome the major



**Fig. 12** **a** Cut-off frequency and **b** transconductance frequency product of D1 and D4 as a function of drain bias, depicting the impact of positive, negative and absence of FC

roadblock of TFET. It is evaluated that the  $I_{ON}/I_{OFF}$  ratio improves from an order of  $10^{10}$  to  $10^{12}$  for GME-SP-DG-TFET that makes it an appropriate candidate for high switching applications. Subsequently, the reliability of the GME-SP-DG-TFET is examined and is simultaneously compared with the conventional DG-TFET. In this respect, the device analog/RF performance is inspected in the presence of FC. It is revealed that the presence of positive FC enhances the subthreshold current considerably by many orders and thus are more noxious than the negative FC. Further, it is obtained that the FC dominantly alters the device characteristics in the subthreshold regime as compared to the superthreshold regime. It is assessed in the ON state, that the increase/decrease in  $f_T$  is 79.89%/48.02% (in D1) and only 23.85%/23.89% (in D4) with positive/negative FC. The significant reduction in variations in  $f_T$  in GME-SP-DG-TFET implies its better reliability. Thereby, the study reveals better reliability of the GME-SP-DG-TFET along with its improved analog/RF performance. Thus, the lower  $I_{OFF}$  ( $10^{-17}$  A), higher  $I_{ON}/I_{OFF}$  ratio ( $10^{12}$ ), lower SS (27 mV/decade), lower  $V_{th}$  (0.62 V) of GME-SP-DG-TFET will effectively meet the need of low power and high switching speed applications. This detailed analysis would be beneficial for designing and optimizing a reliable TFET for low power analog/RF applications.

In the future, one can utilize the proposed GME-SP-DG-TFET as a label-free biosensor, by etching the oxide layer that will act as the binding site for the biomolecules. The biomolecules will bind in the oxide cavity and will thereby alter the device characteristics. The altered device characteristics under the presence of biomolecules in comparison with the case when there is no biomolecule present may be calibrated for detection of biomolecules.

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