Microsystem Technologies (2019) 25:2011–2018
https://doi.org/10.1007/s00542-018-4066-0

TECHNICAL PAPER

Towards modular binary to gray converter design using LTEx module of quantum-dot cellular automata

Chiradeep Mukherjee[1] · Saradindu Panda[2] · Asish Kumar Mukhopadhyay[3] · Bansibadan Maji[1]

Received: 25 July 2017 / Accepted: 21 July 2018 / Published online: 6 August 2018

Abstract
A modular approach to realize the ultra-fast quantum-dot cellular automata (QCA) generic binary to gray converter is presented in this paper. The novel designs here validated fully exploit the intrinsic repetitive capabilities of the Layered T Exclusive OR (LTEx) module in the QCA domain. An efficient logic formulation of QCA design metrics like O-Cost and delay is proposed for the n-bit QCA binary to gray converter designs. The QCA implementation of n-bit LTEx binary to gray converter is compared with the conventional converters. An attempt has been made to enhance the speed of modular binary to gray converter designs. The proposed 4, 8, 16, 32, 64-bit binary to gray converters need 4.35, 15.88, 15.96, 15.7, 16.68% less O-cost and 11.57, 2.61, 9.32, 12.64, 29.25% less effective area, respectively. Thus the proposed layouts offer the smaller feature size, reduced circuit complexity exploiting the modular based design approach. The simulation results have been carried out in the renowned computer aided design tool, namely QCADesigner 2.0.3 with gallium arsenide heterostructure based parameter environment.

1 Introduction

The binary to gray converters are significant quantum-dot cellular automata (QCA) circuit components because they are likely to be used for Gray Code Addressing (Mehta et al. 1996) and Error Control coding schemes (Lin and Costello 2011). Several QCA Binary to Gray converter designs exist but none of them are actually modular. For the first time, this work proposes a modular based approach of n-bit Binary to Gray converters. Firstly a 2-bit exclusive-or module is developed using four elemental Layered T NAND Gates Mukherjee et al. (2015), hence the term LTEx module is given. Then a 4-bit Binary to Gray Code Converter is built cautiously using the proposed LTEx module so that the methodology becomes scalable up to n-bit Binary to Gray Converter. The proposed LTEx module is also used in this work in the realization of 8, 16 and 32-bit Binary to Gray Converter designs. Specific importance has been given to the layout design stability by keeping the design rules of QCA (Liu et al. 2011; Niemier and Kogge 2004) in mind. These design rules and their concerns reduce the kink probability to occur.

The QCA is an emerging nanotechnology in which the information is stored as the configurations of the electron pairs in a quantum cell. The quantum cell is a square structure which consists of four quantum dots located at the four corners. The two electrons within a square would accommodate themselves at the furthest corners due to the electrostatic repulsions between them. These electrons are confined within the quantum cell by high potential barriers and hence the electrons cannot be tunneled to the neighbor quantum cells. The configurations of electron pairs are interpreted as either '+1' or '−1' depending upon two possible orientations of electron pairs within a cell as given in Fig. 1.

The QCA can build multilevel digital circuits in the form of quantum arrays (Lent et al. 1993; Lent and Tougaw 1997). Instead of conventional voltage and current flow, QCA considers the information flow by means of columbic interactions of the electrons of cascaded quantum cells (Smith 1999). The quantum tunneling effect makes QCA the better alternative to conventional CMOS (complementary MOSFETs) in terms of size, power dissipation and speed (Zhang et al. 2004).

✉ Chiradeep Mukherjee
chiradeep.1234321@gmail.com

[1] Department of Electronics and Communication Engineering, National Institute of Technology, Durgapur, India

[2] Department of Electronics and Communication Engineering, Narula Institute of Technology, Kolkata, India

[3] Budge Budge Institute of Technology, Kolkata, India

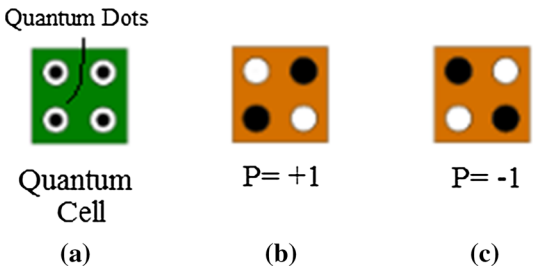

Fig. 1 **a** Quantum cell, polarization P, **b** $P = +1$, **c** $P = -1$

All multilevel architectures and digital circuits have been implemented so that one cell influences the polarization of its immediate neighbour. The relevant literature survey reports several logic gates such as binary wire, majority gate (Zhang et al. 2004), AOI Gate (Momenzadeh et al. 2005), UQCALG gate (Sen et al. 2010), Layered T gate Mukherjee et al. (2015) and computational devices like adders (Mukherjee et al. 2015; Abedi and Jaberipur 2018; Ramesh et al. 2016; Waje and Dakhole 2016; Sasamal et al. 2016) multipliers (Liu et al. 2010; Abedi and Jaberipur 2015; Chudasama and Sasamal 2016), multiplexers (Thakur et al. 2016), comparators (Perri et al. 2014; Roy et al. 2017), Exclusive OR gate (Mukherjee et al. 2017), memories (Berzon and Fountain 1999; Heikalabad et al. 2016) and arithmetic logic units (Fazzion et al. 2014).

The QCA finds four ways for its probable implementations as semiconductor QCA (Dilabio et al. 2015), Molecular QCA (Lent 2000), Magnetic QCA (Imre et al. 2006) and metallic QCA (Toth and Lent 1999). From its invention (Lent et al. 1993; Lent and Tougaw 1997; Smith 1999), QCA remains at the focus as it had been operated at cryogenic temperature. But the recent advent of semiconductor QCA has demonstrated that semiconductor based QCA can operate at a room temperature (Dilabio et al. 2015). Moreover the XPS and spectrographic studies of magnetic QCA, molecular QCA are performed to support the room temperature operability. The last of its type which confines its workability at absolute zero temperature (Toth and Lent 1999) is metallic QCA. As the semiconductor QCA and molecular QCA are more promising, so the QCA Binary to Gray Converter counterparts can be proposed, implemented and verified using semiconductor QCA and molecular QCA as well.

The organization of the paper is given as follows: Sect. 2 presents the design of elemental 2-bit LTEx module, focused on endurance, reproducibility and robustness in order to use it for generic (n-bit) binary to gray converter implementations. The 4-bit, 8-bit and 16-bit binary to gray converters based on design of Sect. 2 have been proposed in the Sect. 3. In this section the outputs of the modular QCA converters are specified to verify the operability of the proposed designs. The modular based designs of Gray Code converters are compared with the existing designs (Iqbal et al. 2013; Waje and Dakhole 2014; Ahmed and Bhat 2014; Beigh and Mustafa 2014; Ahmad et al. 2015; Rao et al. 2015; Islam et al. 2015; Karkaj and Heikalabad 2016), summarized the QCA design metrics and highlighted the improvements over previous designs in the Sect. 4. Finally the concluding remarks have been provided in Sect. 6.

2 LTEx module

As the data-transmission on computer networks seems to attain its peak values in coming decades, so the researchers focus their attentions in the design of nano-devices for ultra-fast code converter circuits. In the nano-converter design paradigm, the Binary to Gray converters find their significances in processor based architecture. For example, the error detection and correction of central processing unit employs Binary to Gray Converters as its fundamental part. In general, a Binary to Gray Converter takes binary numbers as input, processes it and generates the equivalent gray code as output. The main objective of this work is to develop a modular based approach that can be used for the design of n-bit QCA binary to gray converter. To build an n-bit binary to gray converter, two-bit implementation of QCA exclusive or gate becomes inevitable (Mukherjee et al. 2017). A high-level synthesis of elemental two-input Exclusive OR module using Layered T gate is shown in Fig. 2. As the exclusive or gate is implemented using Layered T Gate, so the term Layered T Exclusive-OR (LTEx) has been opted.

The LTEx module of Fig. 2a includes four Layered T NAND (LT NAND) gates. The LT NAND1 takes two inputs A1 and A0 to produce intermediary output T1 at clock 0. The inputs A1, A0 coupled separately with the intermediary output T1 have been connected to the input ports of LT NAND2, LT NAND3, respectively to produce second level intermediary outputs T2 and T3 at clock 1. Lastly, the intermediary outputs T2 and T3 are given to get final output Z0. The clock signals are applied to quantum cells in order 0, 1, 2, 3 so that the intermediary outputs get

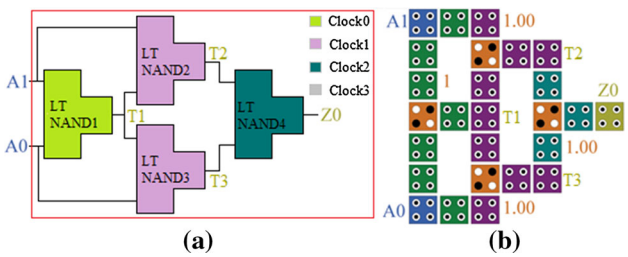

Fig. 2 **a** Block diagram and **b** QCA layout of Two-input LTEx module

evaluated at clock three for proper Exclusive OR output generation. The detailed mathematical interpretations of LTEx block are given in Eq. (1) as follows:

$$\begin{aligned} &T1 = L_T^+(A1,A0),\ T2 = L_T^+(A1,L_T^+(A1,A0)),\\ &T3 = L_T^+(A0,L_T^+(A1,A0))\\ &Z0 = LTEx(A1,A0) = L_T^+(T2,T3)\\ &\quad = L_T^+(L_T^+(A1,L_T^+(A1,A0),L_T^+(A0,L_T^+(A1,A0))) \end{aligned} \tag{1}$$

The researchers in this field require a fast and precise simulation and design layout tool to investigate the functionality of QCA circuits. The QCADesigner tool (QCADesigner 2018) is used for this purpose. The LTEx QCA layout is designed and simulated by QCADesigner with the 18 × 18 nm cell dimension, 5 nm dot diameter, radius of effect 65 nm, layer separation of 11.5 and 2 nm inter-cell distance. The 7 × 7 grid of Fig. 2b acquires 26 cells, 29,346 nm^2 effective area and provides output at negative edge of clock two. The output Z of two-input LTEx module which becomes logic '1′ upon anti-coincidence of the inputs A1 and A0, is evident in Fig. 3. The red-colored box of output Z is start-up time.

The stability of QCA design is very important for the scalability, redesign ability and reproducibility of the QCA circuits. Many times the smaller design becomes advantageous but fails to operate as a part of larger design. In that case, the manufacturer has to tweak the simulation parameters. As a consequence the QCA designs become ineffective. Some design concerns are to be considered all the time for the operable QCA circuits as given below:

1. The input and output quantum cells are to be placed at the border of the circuits to avoid the requirement of unnecessary interconnecting wires (Liu et al. 2011),
2. Minimum two cells (Niemier and Kogge 2004) under a single clock zone is essential in long binary wires. To avoid the large amount of wasted area within a large QCA circuits, the employment of single clock zone with many cells have to be avoided,
3. The use of fixed polarized quantum cell must be increased to have the better stability of the QCA layouts,
4. The outputs must be obtained at the same clocking zone to avoid the race-around information flow within the layouts.

The LTEx module has been designed and simulated with the specific design points in mind. The proposed layout has the input–output cells at the border, same clocking zones are given to minimum two cells and four fixed polarized quantum cells have been employed to build the proposed layout. In subsequent sections, the LTEx module is reused in the designs of 4-bit, 8-bit and 16-bit Binary to Gray Converter circuits.

3 Modular design of generic binary to gray code converters

3.1 4-bit binary to gray converter

The two-input LTEx module has been used in the design of high fan-in Binary to Gray Code converter circuits. Considering the superiority in the design of LTEx module proposed in the preceding section, a novel circuit of a 4-bit Binary to Gray Code converter is presented in this section. The high level block diagram of the proposed circuit is shown in Fig. 4. The block diagram is based on the same

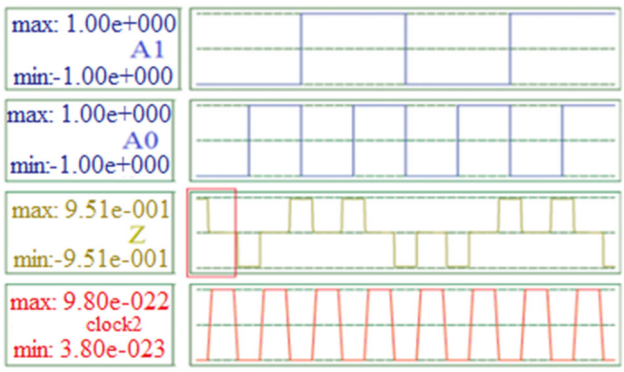

Fig. 3 Output of two-input LTEx module

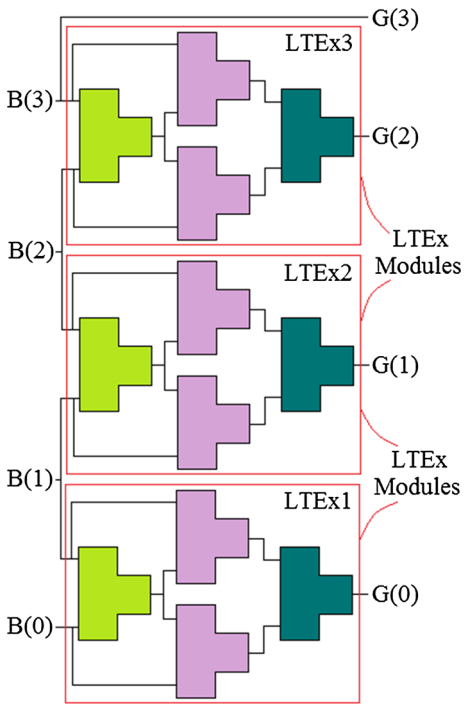

Fig. 4 High level synthesis of 4-bit binary to gray code converter

logic and is composed of three units of LTEx modules as given in Fig. 4. The binary signals B(3), B(2), B(1) and B(0) are the four input signals to the 4-bit Binary to Gray Converter, processed at clock 2 to generate the outputs G(3), G(2), G(1) and G(0). The most significant bit output G(3) equals B(3) whereas G(2) = B(3) ⊕ B(2), G(1) = B(2) ⊕ B(1) and G(0) = B(1) ⊕ B(0) (Iqbal et al. 2013; Moris Mano 2007). From the Fig. 4, it is observed that LTEx3 module takes B(3) and B(2) and produces the output G(2) at clock two and the LTEx2 module processes the inputs B(2) and B(1) to generate the output G(1). The remaining LTEx1 module produces G(0) by taking the two inputs B(1) and B(0). To satisfy the design considerations as specified in the previous section, the high level block diagram of the 4-bit binary to gray converter outputs G(3), G(2), G(1) and G(0) at the clock two. The colored blocks from input side (left) to output side (right) illustrate the QCA pipeline operation in information-flow through the circuit.

The Fig. 5a depicts the layout level synthesis of the 4-bit binary to gray converter. The layout of 4-bit binary to gray converter is implemented using same QCADesigner environment as mentioned before.

According to the QCADesigner tool, the circuit consists of 88 quantum cells marking the value of O-cost (Mukherjee et al. 2017) as 88. The 7 × 25 grid consumes the effective area of 72,376 nm^2, generates the outputs at the negative edge of the clock two as given in Fig. 5b. The coherence vector model is used during the simulation of converter with relaxation time 10^{-15} s, step time 10^{-16} s and radius of effect 65 nm.

The coherence vector simulation engine have been initialized with the Binary input vector {B(3)B(2)B(1)B(0)} as {0010, 0011, 0100, 0111, 0101, 1111}. By its certain operability, the 4-bit LTEx Binary to Gray Converter confirms the output as {G(3)G(2)G(1)G(0)} with the output vector {0011, 0010, 0110, 0100, 0111, 1000}. The output

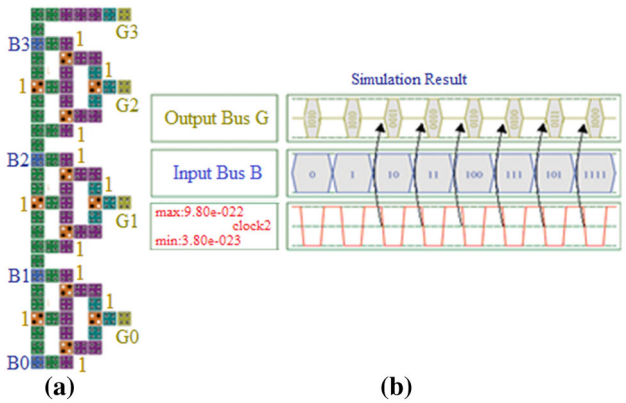

Fig. 5 **a** QCA layout and **b** output of 4-bit binary to gray code converter

has been demonstrated in Fig. 5b. The first arrow of Fig. 5b indicates first valid gray counterpart.

3.2 8-bit binary to gray converter

The higher order QCA binary to gray converter can be designed using the modular approach presented in the previous sections. Here, an 8-bit QCA Binary to Gray converter circuit is proposed, simulated and verified. The modular implementation reports the need of seven two-input LTEx modules as given in Fig. 6. The blocks presented in Fig. 6 are identical to the 4-bit Binary to Gray converter presented in Sect. 3.1.

The information-flow through the circuit is in proper synchronization in every block by the clock signals. The output gray vector {G} is likely to get its value at the falling edge of clock two. The 8-bit binary to gray converter takes the binary input vector {B(7)B(6)B(5)B(4)B(3)B(2)B(1)B(0)}, applies the exclusive or operations on the literals (Moris Mano 2007) and produce its gray counterpart {G(7)G(6)G(5)G(4)G(3)G(2)G(1)G(0)}.

The QCA implementation of 8-bit binary to gray converter is reported in Fig. 7a. The layout consumes 224,581 nm^2 effective area, has the value of O-cost as 196 and achieves the delay of 0.75.

The circuit simulations are shown in Fig. 7b. The input and output buses are indicated by the lower and upper waveforms, respectively in the Fig. 7b.

The 8-bit LTEx converter is tested with binary vector {00101001, 00010110, 01101100, 11011011} as given in Fig. 7b. The arrow highlights the valid gray counterpart as {00111101, 00011101, 01101100, 11011011} which confirms the proper functionality of the binary to gray code converter circuit.

3.3 16-bit binary to gray converter

Starting from the 4-bit binary to gray code converter, this work demonstrates 8-bit and 16-bit binary to gray converters using the 2-input LTEx module as the basic building block. The 16-bit binary to gray converter has been decomposed into smaller parts as given in Fig. 8a. Then these smaller pieces are substituted by cascaded two-input LTEx modules to complete the QCA implementation of 16-bit LTEx converter circuit. The modular approach shows that the output vector {G(15)G(14)…G(1)G(0)} is produced at the clock 2 making the neat input-to-output propagation delay as 0.75. It is obvious to note that the modular synthesis of 16-bit LTEx converter requires (16 − 1) = 15 numbers of two-input LTEx module as well.

The QCA implementation of 16-bit binary to gray code converter is represented in Fig. 8b. The layout covers the

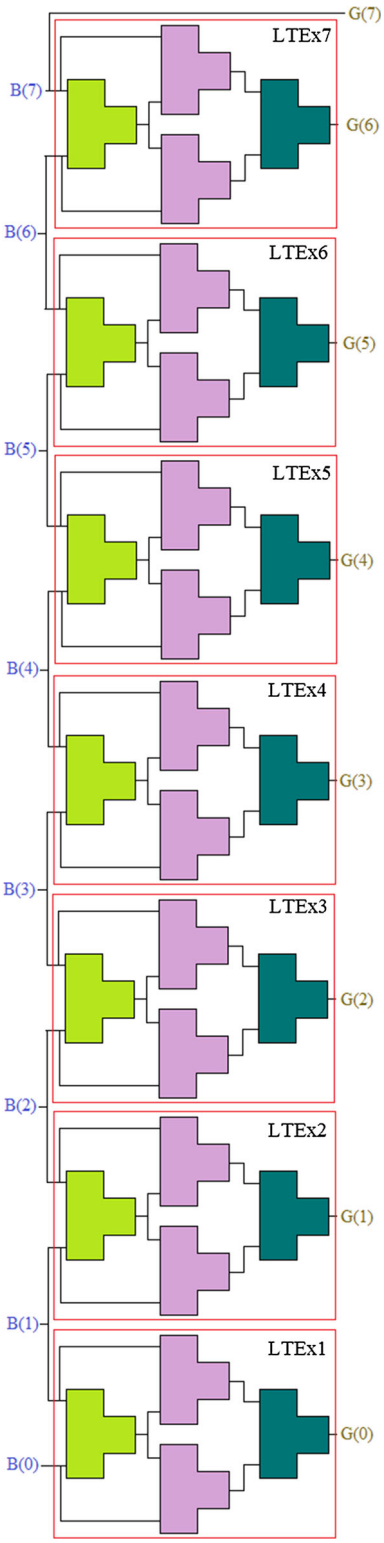

Fig. 6 High level synthesis of 8-bit binary to gray code converter

effective area as 526,784 nm^2, reports O-cost as 412 with the delay of 0.75. The simulation result of Fig. 9 conform the functionality of the 16-bit binary to gray converter.

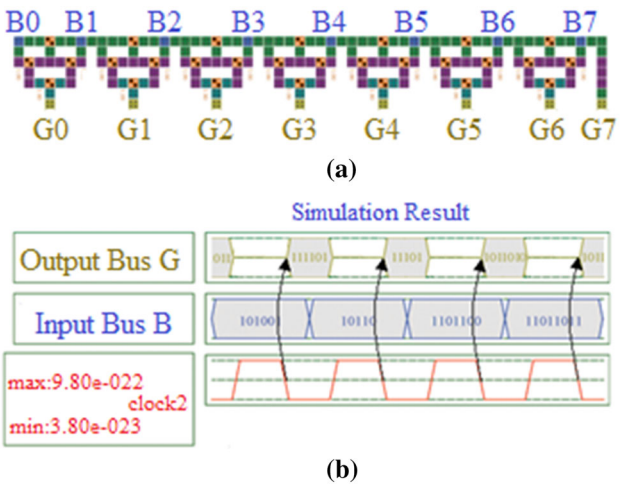

Fig. 7 **a** QCA layout and **b** output of 8-bit binary to gray code converter

The post-implementation design summary of the converters (with n = 4, 8, 16, 32, 64, where n is number of inputs) has been summarized in Tables 1, 2. Various QCA design metrics like O-cost, effective area (in nm^2) and the number of Gate counts have been noted. The comparisons with the previously existing 4-bit designs (Iqbal et al. 2013; Waje and Dakhole 2014; Ahmed and Bhat 2014; Beigh and Mustafa 2014; Ahmad et al. 2015; Rao et al. 2015; Islam et al. 2015; Karkaj and Heikalabad 2016) have been drawn in Table 1. The literature survey in the relevant field pays an attention to the Ahmad converter (Ahmad et al. 2015) that firstly introduced the pathway to design an n-bit converter designs. The Table 2 highlights the statistics of the existing n-bit binary to gray converter (Ahmad et al. 2015) and compares it with generic LTEx counterparts. The researcher can find out the guidelines to design modular n-bit binary to gray converter design the LTEx design becomes highly modular. The n-bit binary to gray converter can be easily be extended to a higher order circuit by (a) taking (n − 1) numbers of cascaded LTEx modules, (b) arranging the delay of the modular blocks so that each outputs get its value after clock two and (c) taking the interconnecting wires from the most significant input to generate most significant bit of the output. This mechanism can be realized by associating the Figs. 4, 6 and 8 in mind.

If the manufacturers wish to instantiate the n-bit binary to gray converter design more precisely, they realize that the modular approach of the LTEx converter consists of (n − 1) two-input LTEx modules which are collectively 4(n − 1) LT NAND gates. The layout is receiving its n-bit inputs to produce 3(n − 1) intermediary outputs. As concurrent information flow through the block is predicted, so all the outputs will get its value exactly after 0.75 clock pulse.

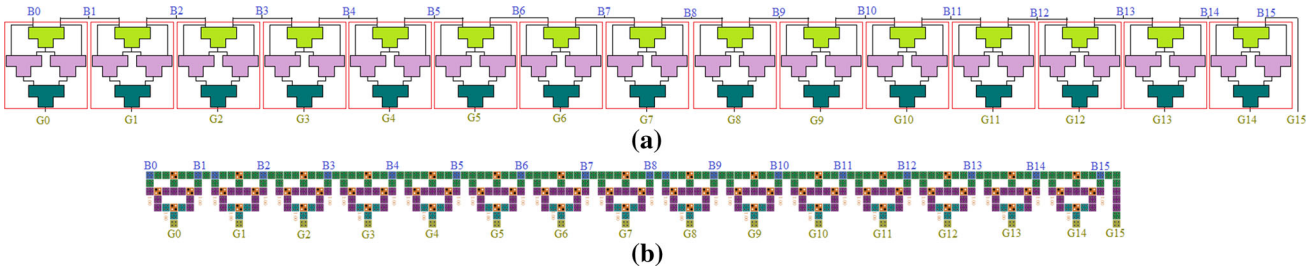

Fig. 8 **a** Modular synthesis and **b** layout of 16-bit binary to gray code converter

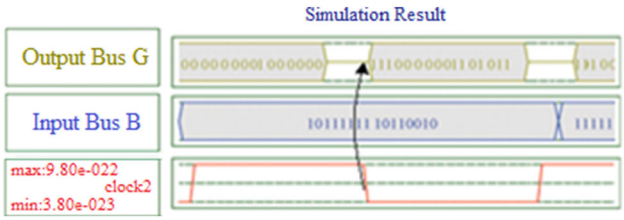

Fig. 9 Output of 16-bit binary to gray code converter

4 Conclusion

A novel approach of efficient modular based n-bit binary to gray code converter has been presented. It is based on two-input LTEx module leading to modular structures able to achieve increased speed performances and reduce size compared to the existing converters. The high level synthesis and design layout of two-input LTEx module is proposed on the basis of NAND realization of exclusive or gate. As minimum four NAND gates are required to

Table 1 Design summary of 4-bit binary to gray converter with existing designs (Iqbal et al. 2013; Waje and Dakhole 2014; Ahmed and Bhat 2014; Beigh and Mustafa 2014; Ahmad et al. 2015; Rao et al. 2015; Islam et al. 2015; Karkaj and Heikalabad 2016)

Sl No.	4-bit binary to gray converter designs proposed	O-cost	Effective area in nm^2	Gate count	Types of wire crossing
1	In Islam et al.(2015)	131	166,344	MV:9	NA
2	In Ahmad et al. (2015)	109	98,604	MV:10	Multilayer
3	In Beigh and Mustafa (2014)	192	269,724	MV:12	NA
4	In Iqbal et al. (2013)	389	> 126,000	MV:9	Coplanar
5	In Karkaj and Heikalabad (2016)	92	81,844	NA	NA
6	In Ahmed and Bhat (2014)	137	120,684	MV:9	NA
7	In Rao et al. (2015)	127	151,844	MV:9	Multilayer
8	In Waje and Dakhole (2014)	133	161,656	MV:9	Multilayer
9	This work	88	72,376	LT:6	Multilayer

Table 2 Comparison of n-bit binary to gray converter (Ahmad et al. 2015) with n-bit LTEx binary to gray converter

n-bit B2G converter structures	n	Effective area (μm^2)	Improvement	O-cost	Improvement	Delay	Improvement
In Ahmad et al. (2015)	8	0.23	–	233	–	1.5	–
	16	0.58		489		3	
	32	1.25		1001		6	
	64	2.77		2050		12	
This work	8	0.224	2.61%	196	15.88%	0.75	50%
	16	0.526	9.32%	412	15.96%	0.75	75%
	32	1.092	12.64%	844	15.7%	0.75	87.5%
	64	1.96	29.25%	1708	16.68%	0.75	93.75%

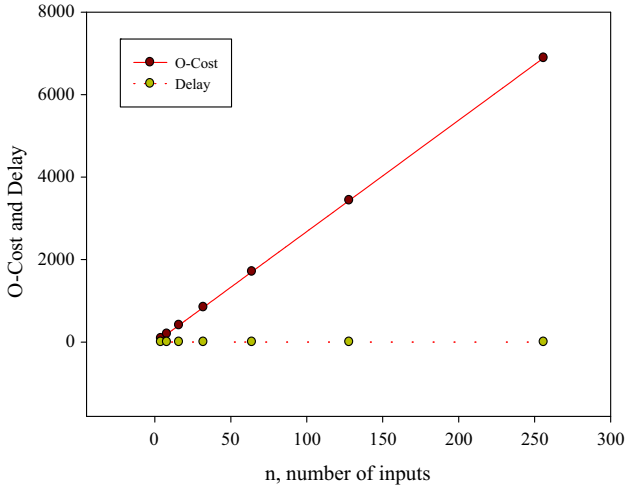

Fig. 10 The Graphs showing the O-cost and delay relationships with input n for a generic LTEx binary to gray code converter

implement exclusive or gate, so four LTEx modules have been instantiated to form layered T exclusive OR Gate, namely LTEx module. The LTEx modules are recursively cascaded to build 4-bit Binary to gray converter as shown in Fig. 5a. The layout of 4-bit converter has been compared with the existing designs in terms of QCA metrics as mentioned in Table 1. The proposed 4-bit binary to gray converter needs ∼ 4.35% less O-cost, 11.57% less effective area, as compared to the best reported design of Karkaj converter (Karkaj and Heikalabad 2016). The proposed converter shows 33.33% less number of gate requirement as compared to the Rao converter (Rao et al. 2015).

For the instances of n-bit binary to gray Converter, the percentage improvement can be noted in every aspect of QCA design parameters compared to Ahmad Counterparts (Ahmad et al. 2015). The proposed 8, 16, 32, 64-bit binary to gray code converters consume 15.88, 15.96, 15.7, 16.68% less O-cost and 2.61, 9.32, 12.64, 29.25% less effective area, respectively. It is interesting to note that the percentage improvement in effective area (in μm^2) increases with the high fan-in counterparts of LTEx Binary to Gray Converter structures. Utmost 29.25% improvement has been noted during the effective area comparison of 64-bit LTEx Converter as reported in Table 2. Additionally the 64-bit LTEx converter reports up to 16.68% improvement in O-cost compared to the 64-bit counterpart of Ahmad converter (Ahmad et al. 2015). As the delay remains independent with the number of inputs for the n-bit LTEx inverter, so 93.75% improvement has been reported for 64-bit layout comparison with Ahmad converter counterpart (Ahmad et al. 2015).

The formulation of O-cost and delay for a generic LTEx binary to gray converter has been done. The O-cost requirement is 27n-20, for an n-bit binary to gray converter which estimates linear dependency on input bit n as demonstrated in Fig. 10. The delay of n-bit binary to gray converters remains constant at 0.75, independent on the input bit resulting an ultra-fast modular approach for generic binary to gray converter design paradigm.

Acknowledgement The authors are highly thankful to Prof. Arindam Chakraborty for insightful views in relevant topics and express special thanks to Prof. Debdatta Banerjee for her literary contributions that help authors in organizing the article.

References

Abedi D, Jaberipur G (2015) Coplanar QCA serial adder and multiplier via clock-zone based crossover. 18th CSI International Symposium on Computer Architecture and Digital Systems (CADS). https://doi.org/10.1109/cads.2015.7377791

Abedi D, Jaberipur G (2018) Decimal full adders specially designed for quantum-dot cellular automata. IEEE Trans Circuits Syst II Express Briefs 65(1):106–110. https://doi.org/10.1109/tcsii.2017.2703942

Ahmad F, Md. Bhat G, Ahmad PZ, Khan HA, Farooq R (2015) Design of N-Bit code converter using quantum-dot cellular automata (QCA). Adv Sci Eng Med 7:1–8. https://doi.org/10.1166/asem.2015.1677

Ahmed F, Bhat GM (2014) Novel code converters based on quantum-dot cellular automata (QCA). Int J Sci Res 3:364–371 **Paper ID: 020131715**

Beigh MR, Mustafa M (2014) Design and simulation of efficient code converter circuits for quantum-dot cellular automata. J Comput Theor Nanosci 11:2564–2569. https://doi.org/10.1166/jctn.2014.3673

Berzon D, Fountain TJ (1999) A memory design in QCAs using the SQUARES formalism, Proceedings of ninth great lakes symposium on VLSI. Ypsilanti, MI, pp 166–169. https://doi.org/10.1109/GLSV.1999.757402

Chudasama A, Sasamal TN (2016) Implementation of 4 × 4 vedic multiplier using carry save adder in quantum-dot cellular automata. Int Conf Commun and Signal Process (ICCSP). https://doi.org/10.1109/iccsp.2016.7754355

Dilabio GA, Wolkow RA, Pitters JL, Piva G (2015) Atomistic quantum dots. USA Patent: US 2015/006071 A1. https://patents.google.com/patent/US20150060771/en. Accessed 19 July 2018

Fazzion E, Fonseca OLHM, Augusto J, Nacif M, Neto OPV, Fernandes AO, Silva DS (2014). A quantum-dot cellular automata processor design. 27th Symposium on Integrated Circuits and Systems Design (SBCCI). pp. 1–7. https://doi.org/10.1145/2660540.2660997

Heikalabad SR, Navin AH, Hosseinzadeh M (2016) Content addressable memory cell in quantum-dot cellular automata. Microelectr Eng 163:140–150. https://doi.org/10.1016/j.mee.2016.06.009

Imre A, Csaba G, Ji L, Orlov A, Bernstein GH, Porod W (2006) Majority logic gate for magnetic quantum-dot cellular automata. Science 311:205–208. https://doi.org/10.1126/science.1120506

Iqbal J, Khanday FA, Shah NA (2013) Efficient quantum dot cellular automata (QCA) implementation of code converters. Commun Inf Sci Manag Eng 3:504–515

Islam S, Abdullah-al Shafi M, Bahar AN (2015) Implementation of binary to gray code converters in quantum dot cellular automata. J Today Ideas Tomorrow Technol 3:145–160. https://doi.org/10.15415/jotitt.2015.32010

Karkaj ET, Heikalabad SR (2016) Binary to gray and gray to binary converter in quantum-dot cellular automata. Opt Int J Light Electron Optic. https://doi.org/10.1016/j.ijleo.2016.11.087

Lent C (2000) Molecular electronics-bypassing the transistor paradigm. Science 288:1597–1599. https://doi.org/10.1126/science.288.5471.1597

Lent C, Tougaw P, Porod W, Bernstein G (1993) Quantum cellular automata. Nanotechnology 4:49–57. https://doi.org/10.1088/0957-4484/4/1/004

Lent C, Tougaw P (1997) A device architecture for computing with quantum dots. Proc IEEE 85:541–557 **PII: S 0018-9219(97)02731-X**

Lin S, Costello Jr DJ (2011) Error control coding. Pearson Education India, New Delhi. ISBN-13:978–8131734407

Liu W, Lu L, O'Neill M, Swartzlander EE Jr (2011) Design rules for quantum-dot cellular automata. IEEE Int Symp Circuits Syst (ISCAS). https://doi.org/10.1109/iscas.2011.5938077

Mehta H, Owens RM, Irwin MJ (1996) Some issues in gray code addressing. In: Proceedings of the sixth great lakes symposium on VLSI, Ames, IA, pp 178–181. https://doi.org/10.1109/GLSV.1996.497616

Momenzadeh M, Huang J, Tahoori MB, Lombardi F (2005) Characterization, test and logic synthesis of and-or-inverter (AOI) gate design for QCA implementation. IEEE Trans Comput Aided Des Integr Circuits Syst 24(12):1881–1893. https://doi.org/10.1109/TCAD.2005.852667

Moris Mano M (2007) Computer system architecture. Pearson Education India, New Delhi. ISBN-13:978–8131700709

Mukherjee C, Sukla SS, Basu SS, Chakraborty R, De D (2015a) Layered T full adder using quantum-dot cellular automata. IEEE Int Conf Electron Comput Commun Technol. https://doi.org/10.1109/conecct.2015.7383867

Mukherjee C, Sukla AS, Basu SS, Chakrabarty R, Khan A, De D (2015b) Layered T full adder using quantum-dot cellular automata. IEEE Int Conf Electron Comput Commun Technologies (CONECCT-2015). https://doi.org/10.1109/conecct.2015.7383867

Mukherjee C, Panda S, Mukhopadhyay AK, Maji B (2017) Synthesis of standard functions and generic Ex-OR module using layered T gate. Int J High Perfor Sys Arch 7(2):70–86

Niemier MT, Kogge PM (2004) Origins and motivations for design rules in QCA nano, quantum and molecular computing. Kluwer Academic Publishers, Netherlands, pp 267–293

Perri S, Corsonello P, Cocorullo G (2014) Design of efficient binary comparators in quantum-dot cellular automata. IEEE Trans Nanotechnol 13(2):192–202. https://doi.org/10.1109/TNANO.2013.2295711

QCADesigner (2018) Available: www.atips.ca/projects/qcadesigner. Accessed 15 July 2017

Ramesh B, Asharani M, Srujana V, Chaithanya P, Rajaiah U (2016) Area efficient BCD adder in Quantum dot Cellular Automata. 2nd Int Conf Contemp Comput Inf (IC3I). https://doi.org/10.1109/ic3i.2016.7917955

Rao NG, Srikanth PC, Sharan P (2015) A novel quantum dot cellular automata for 4-bit code converters. Opt Int J Light Electron Optic. https://doi.org/10.1016/j.ijleo.2015.12.119

Roy SS, Mukherjee C, Panda S, Mukhopadhyay AK, Maji B (2017) Layered T comparator design using quantum-dot cellular automata. In: Presented in 2nd international conference on Devices for Integrated Circuit (DevIC), Kalyani, pp 90–94. https://doi.org/10.1109/DEVIC.2017.8073913

Sasamal TN, Singh AK, Ghanekar U (2016) Design of non-restoring binary array divider in majority logic-based QCA. Electron Lett 52(24):2001–2003. https://doi.org/10.1049/el.2016.3188

Sen B, Sengupta A, Dalui M, Sikdar BK (2010) Design of testable universal logic gate targeting minimum wire-crossings in QCA logic circuit. 2010 13th Euromicro Conference on Digital System Design: Architectures, Methods and Tools, Lille, pp 613–620. https://doi.org/10.1109/dsd.2010.114

Smith CG (1999) Computation without Current. Science 284:274. https://doi.org/10.1126/science.284.5412.274

Thakur G, Gumpe A, Sarvagya M, Sharan P (2016) An area efficient multiplexer for crossbar arbiter design using quantum dot cellular automata. IEEE Int Conf Recent Trends Electr Inf Commun Technol (RTEICT). https://doi.org/10.1109/rteict.2016.7807970

Toth G, Lent CS (1999) Quasi-adiabatic switching for metal-island quantum-dot cellular automata. J Appl Phys 85:2977–2984. https://doi.org/10.1063/1.369063

Waje MG, Dakhole PK (2014) Design and simulation of new XOR gate and code converters using quantum dot cellular automata with reduced number of wire crossings. IEEE Int Conf Circuit Power Comput Technol. https://doi.org/10.1109/iccpct.2014.7054942

Waje MG, Dakhole PK (2016) Analysis of various approaches used for the implementation of QCA based full adder circuit. Int Conf Electr Electron Optim Tech (ICEEOT). https://doi.org/10.1109/iceeot.2016.7755129

Liu W, Lu L, O'Neill M, Swartzlander EE (2010) Montgomery modular multiplier design in quantum-dot cellular automata using cut-set retiming. 10th IEEE Int Conf Nanotechnol. https://doi.org/10.1109/nano.2010.5697740

Zhang R, Walus K, Wang W, Jullien GA (2004) A method of majority logic reduction for quantum cellular automata. IEEE Trans Nanotechnol 3(4):443–450. https://doi.org/10.1109/TNANO.2004.834177