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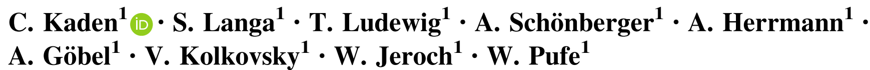
TECHNICAL PAPER

Enhancement of vertical integration density by engineered BSOI wafers



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Abstract The lateral and vertical integration density of bulk microelectromechanical systems (MEMS) using bonded silicon-on-insulator (BSOI) wafers is significantly enhanced if the handle wafer is used as an electrical redistribution layer. Therefore isolated conductive paths should be integrated in the handle wafer, which are connected to the surface of the BSOI-wafer by high aspect ratio contacts (VIAs) through the device layer of the BSOI-wafer. In the present study we report on a fabrication process for customer specific designed BSOI wafers with VIAs from the device to the handle layers. Wafer bonding, wafer edge shaping and thinning of the wafers, which are critical processes for the fabrication of the BSOI-wafers, are discussed. The contacts to the handle wafer through the 75 µm thick device layer are created by 10 µm wide and 75 µm deep trenches filled with highly doped *n*-type polysilicon. From current–voltage measurements an ohmic behaviour of the contacts with a resistance of around 120 Ω is demonstrated.

1 Introduction

System in Package (SiP, Tai 2000) is an effective approach to gain more functionality of devices by integrating several MEMS devices and their controlling units into one functional package. SiP can be implemented as lateral integration (2D), lateral and vertical (2.5D) or pure vertical integration (3D). However, due to the die-level integration of the different components within SiP, the packaging costs can become very high. In this case System on Chip (SoC) (Benini and De Micheli 2002) can be used as an alternative approach. Similarly to SiP, SoC can be realized in three different configurations 2D, 2.5D or 3D. However the integration on wafer-level reduces the packaging costs significantly.

In the present paper an approach to enhance the vertical integration density of MEMS-devices fabricated on the basis of bonded silicon-on-insulator (BSOI) wafers is discussed. BSOI-wafers are widely used e.g. for the fabrication of MOEMS (Grahmann et al. 2015; Langa et al. 2013), pressure sensors (Li et al. 2015; Ngo et al. 2015), inertial sensors (Abdolvand et al. 2007) and energy harvesters (Nimo et al. 2011).

In the past there have been approaches to engineer the BSOI handle or device wafer before bonding, see e.g. PBSOI (patterned BSOI) for vertical transistors (Moriceau et al. 2004; Kim et al. 2005).

A typical BSOI wafer (Fig. 1) consists of three main components: a handle wafer (e.g. 400–700 µm thick), a device wafer (e.g. 5–200 µm thick) and a buried oxide layer (BOX, e.g. 0.1–1 µm thick). The handle and the device wafers are bonded together by fusion bonding, the BOX is used as bonding and isolation interface between the wafers. The MEMS devices are usually structured in the device layer of the BSOI wafer and the handle wafer is only used for mechanical stability purposes.

Our approach is to define conducting paths in the handle wafer before bonding and connect them by VIAs in the device layer to the surface of the BSOI-wafer. In this case the handle wafer can act as an electrical redistribution layer and can replace conducting layers originally placed on the surface of the BSOI wafer. Since the conducting paths are processed before wafer bonding, the applied materials must

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Fig. 1 Schematic view of a BSOI-wafer with shaped wafer edge, the angle α should be between 30° and 60°

be able to resist high temperature processes during further processing. The formation of conducting paths within the handle wafer increases the complexity in signal controlling compared to the standard MEMS technology and enables new and more complex SoC MEMS-architectures and multifunctional systems.

The fabrication of a BSOI wafer includes three critical process steps: wafer bonding, wafer-edge shaping and thinning of the device wafer. Especially for MOEMS-applications the shape of the wafer edge is critical to allow further processing of the BSOI wafers in the cleanroom.

In the present study our results regarding a fabrication process for customer specific designed BSOI wafers are discussed, in the second part we present first results regarding the contacts (VIAs) through the device layer.

2 Wafer bonding

The main requirements for the wafer bonding are a high bonding strength and a void free bond interface. For the fabrication of the BSOI-wafers a 400 µm thick phosphorus doped wafer with a resistivity of 0.9 Ω cm as handle wafer and a 475 µm thick boron doped wafer with a resistivity of 0.015 Ω cm as a device wafer are used. The handle wafer was covered with a 1 µm thick thermal oxide.

The handle wafer was mechanically aligned and hydrophilic pre-bonded to the device wafer. Hydrophilicity was ensured by RCA-cleaning prior to wafer bonding. A subsequent anneal in a batch process at 1025 °C for 4 h defined the final bond strength. Figure 2 shows an infrared picture of a BSOI-wafer with an uniform bond interface without any voids.

The bonding strength was measured using the Maszara model (Maszara et al. 1989) for the double cantilever beam method, also known as razor blade test. One wafer per batch was diced into 1 cm wide stripes, the measurement was performed on 10 stripes per wafer. The razor blade was inserted manually, the crack length was measured 15, 60 and 120 s after the insertion of the razor blade. The measured bonding strength decreases rapidly from more than 3.0 J/m^2 at 15 s to 2.8 J/m^2 at 60 s to 2.7 J/m^2 at 120 s (Fig. 3), each Box-plot contains five measurements. The decrease of the bonding strength can be explained by the crack corrosion phenomenon (Bagdahn et al. 1998; Vallin et al. 2005). The bonding strength is high enough to allow further processing of the wafers.

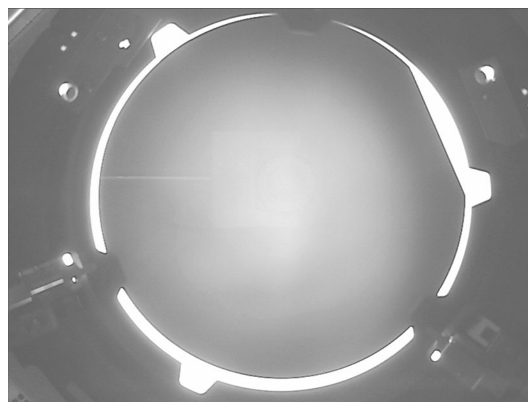

Fig. 2 Infrared picture of a bonded and annealed BSOI-wafer

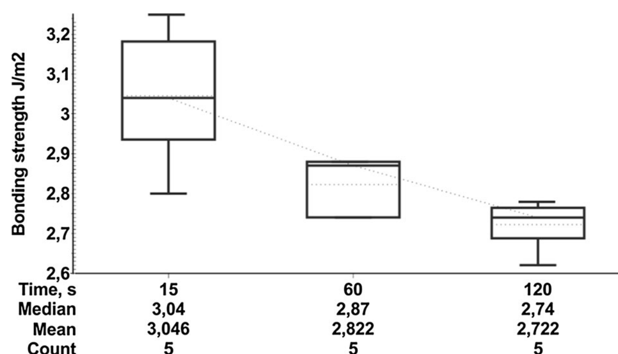

Fig. 3 Box-plots of bonding strength (J/m^2) versus time distance (s) between insertion of the razor blade and measurement

3 Wafer edge shaping

Wafer edge shaping is required to avoid sharp edges of the final BSOI-wafer and to allow an uniform photoresist distribution at the wafer edge during the lithography processes. In addition, especially for the fabrication of MOEMS based on bulk technology, it is important not to damage the oxide of the handle wafer, because this oxide layer is needed during further processing for wafer edge protection (Fig. 1). In our fabrication process the wafer edge was shaped using the Circle Cut Mode of the wafer dicing saw DISCO DAD651 in combination with a subsequent etching process. The process is very flexible and different wafer edge shapes with various angles α (Fig. 1) have been realized by using a trapezoid dicing blade. By changing the dicing blade the angle α at the wafer edge can be varied. In Fig. 4 a typical wafer edge of a BSOI-wafer is

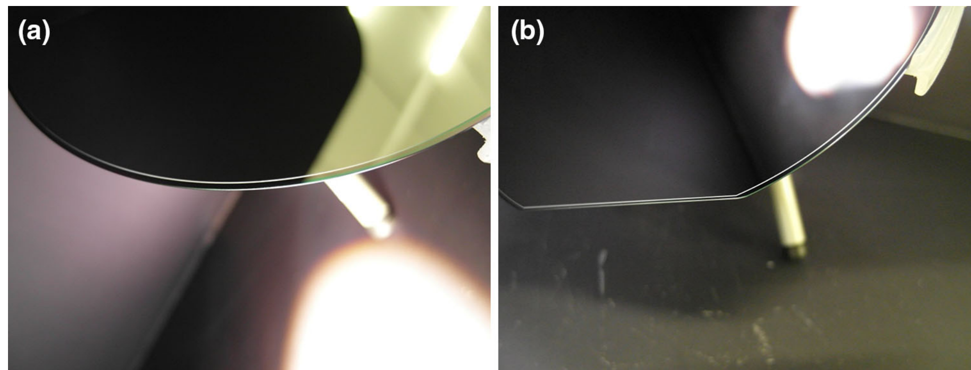

Fig. 4 **a** Wafer edge of a completely finished BSOI-wafer, **b** flat region of the wafer

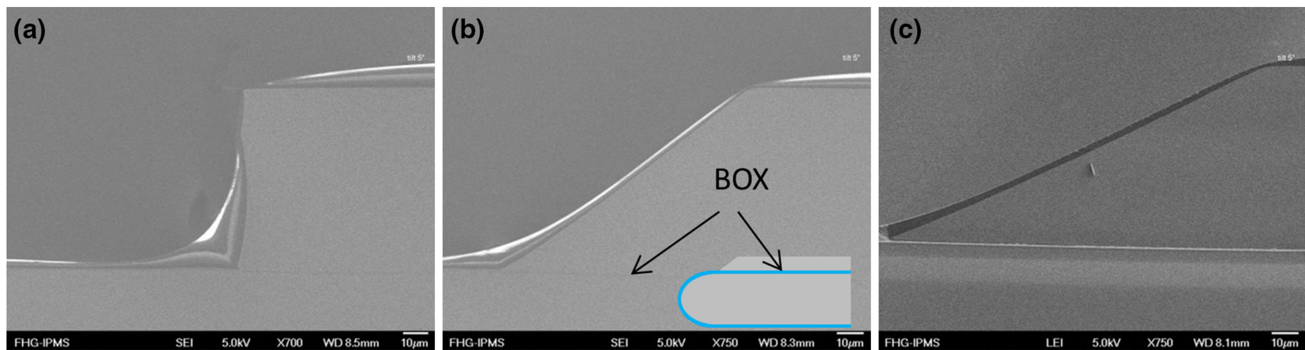

Fig. 5 SEM-views of resist coated BSOI wafers with angles α of **a** 90°, **b** 45° and **c** 30°

shown. The wafer edge is uniform, smooth, no chipping or damage of the handle wafer is visible.

For the further preparation of the wafers, especially edge protection during deep silicon etching, it is important to ensure a smooth resist distribution at the edge of the device wafer.

Figure 5 shows resist coated BSOI wafers with different angles α at the wafer edge. The 90°-angle was created by dry etching and the resist tears at the edge and also on the handle wafer. In contrast a continuous distribution of the resist can be ensured by an angle of 30°.

4 Wafer thinning

After shaping of the wafer edge the device wafers were thinned by a grinding process from 475 to 80 µm. In a subsequent chemical mechanical polishing (CMP) step the surface is smoothed and polished to a target thickness of 75 µm. The CMP-process also removes the damaged Si layer induced by the grinding process.

The obtained BSOI-wafers are suitable for further processing in a cleanroom for the fabrication of MEMS devices.

5 Contacts (VIAs) through the device layer

The next step was to implement a VIA connection between the surface of the BSOI wafer and the handle wafer through the device layer. The following critical steps could be distinguished: trench etching, BOX removal, isolation of the trench walls and filling of the trenches with a conductive material.

The trenches to the handle wafer through the 75 µm thick p-doped device layer were realized by dry etching using the Bosch-process. Different trench widths have been realised from 3 to 10 µm. The BOX on the bottom of the 75 µm trenches was removed be wet etching. Figure 6 shows the process flows, where an isolation of the VIA from the rest of the device layer was obtained by doping, i.e. *pn*-junction (Fig. 6a) or an oxide isolation (Fig. 6b). For the oxide isolation a CVD-oxide followed by a spacer etch was used. While depositing nominally 1500 nm oxide on the sidewalls and the bottom of the trenches a thickness of 200 nm was obtained. In a subsequent nominally 800 nm oxide etch the oxide at the bottom of the trench could be completely removed, while the oxide on the sidewalls was unaffected. It was found that the oxide isolation process is limiting the

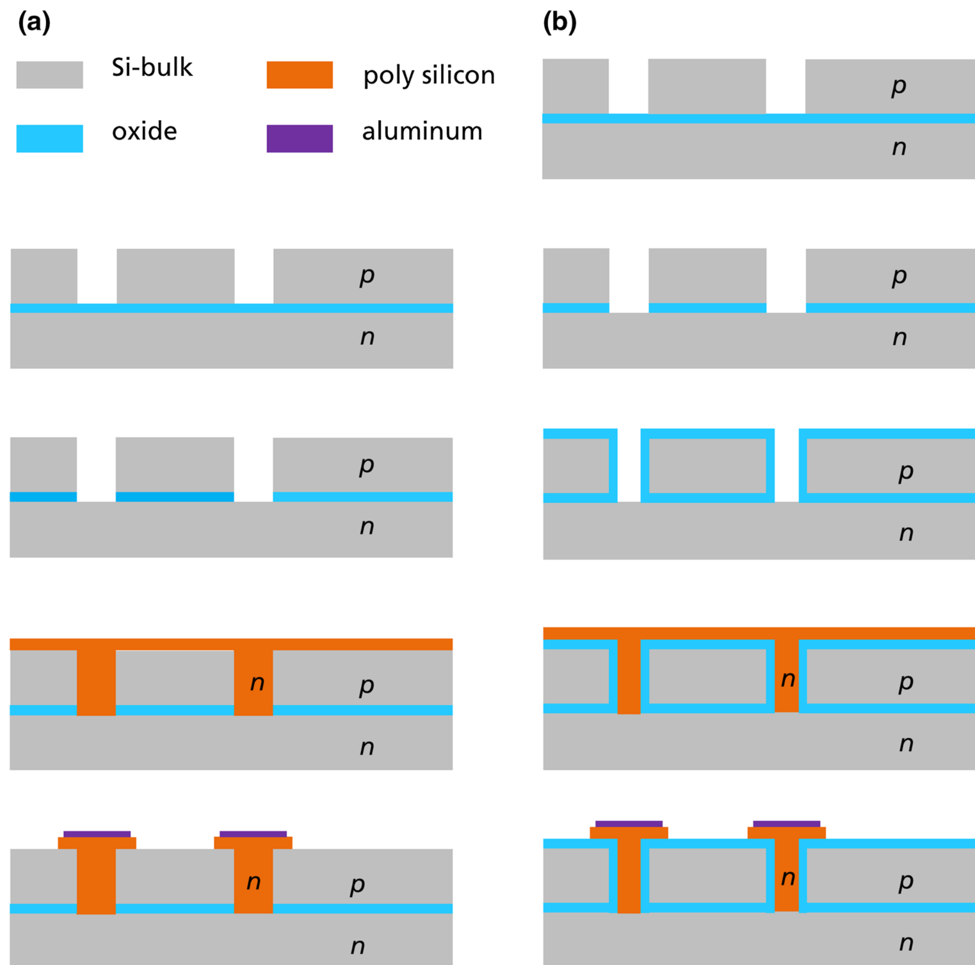

Fig. 6 Process flow defining the contacts through the device layer. The current path isolation was defined either **a** by *pn*-junction or **b** by oxide isolation

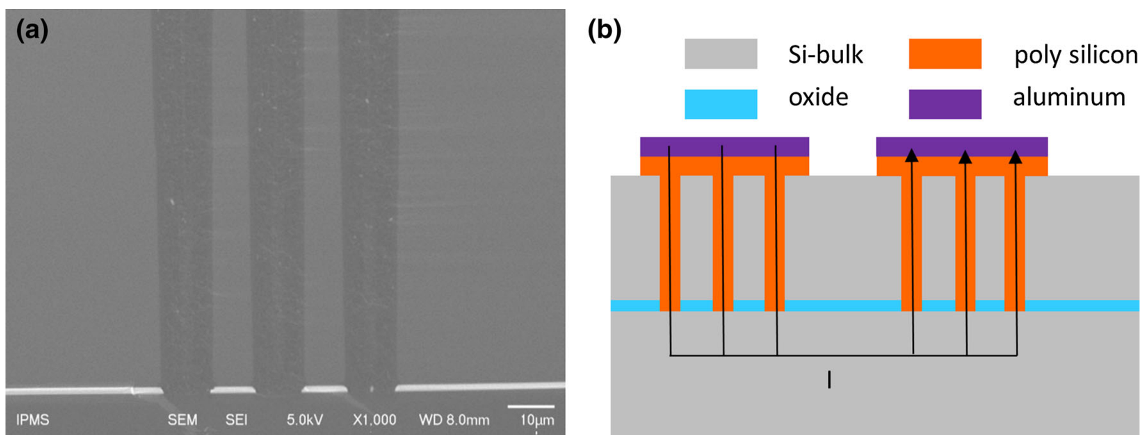

Fig. 7 **a** SEM view of bottom area of contacts, where the current path was defined by doping, **b** schematic view

trench dimension to an aspect ratio of about 8. For smaller trenches the oxide on the bottom of the trench using DRIE could not be removed.

The trenches were filled with highly phosphorus-doped Poly-Si with a resistivity of 6.5 Ω µm. The *pn*-junction for isolation of the VIAs and the device layer was formed by

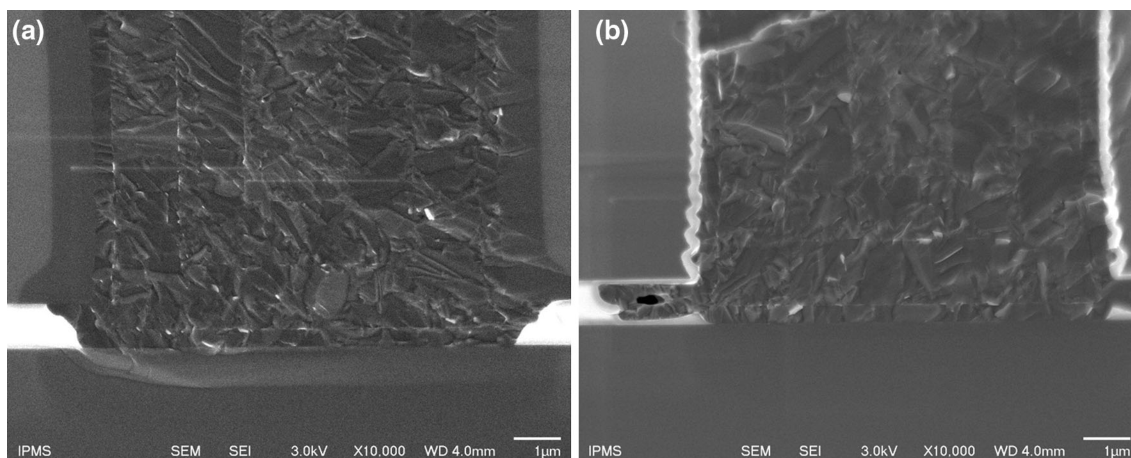

Fig. 8 SEM views of the bottom area of contacts **a** defined by *pn*-junction and **b** by oxide isolation

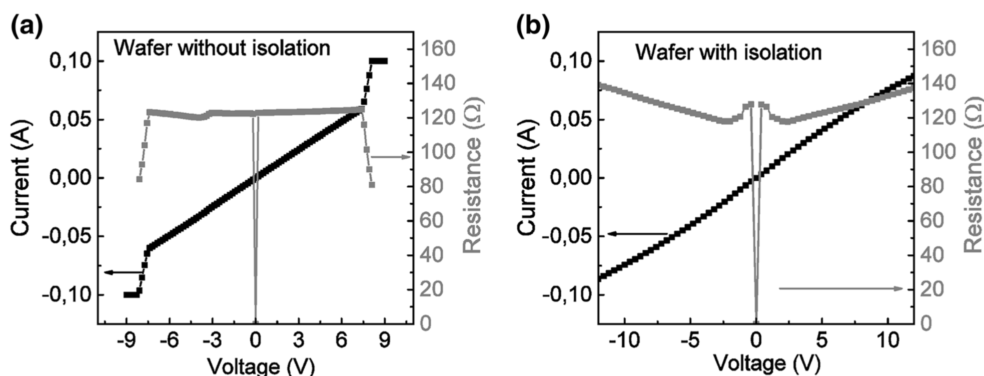

Fig. 9 Current-voltage measurements of contacts with pn-junction (**a**) and oxide isolation (**b**)

an additional annealing step, where the phosphorus dopants from the *n*-type poly-Si are diffusing into the device layer. Subsequently, the poly-Si layer was structured and contacted by aluminum (Al)-pads.

The obtained structures could be easily planarized enabling further processing in a CMOS-line, including high temperature steps.

Figure 7a shows ans SEM-view of the bottom area of a VIA contact to the handle wafer where the isolation was defined by *pn*-junction. In Fig. 7b a schematic view of the VIA contacts including the current path is shown. One VIA-contact is defined by three trenches, the dimension of each individual trench is 10 µm × 140 µm × 75 µm. The distance between the trenches is 10 µm.

Figure 8 presents SEM images of the bottom area of the contacts defined by *pn*-junction (a) and oxide isolation (b). As can be seen the BOX-layer is completely removed, and the isolation oxide on the walls of the trenches can be clearly seen.

The VIA-contacts were characterised by current–voltage measurements. Figure 9 demonstrates the I–V curves (black) and resistance (gray) of contacts with isolation using a *pn*-junction (Fig. 9a) or an oxide isolation (Fig. 9b). In both cases the I–V characteristics are linear with a resistance around 120 Ω from pad to pad, which is a characteristic feature of ohmic contacts. The measured resistance is dominated by the substrate resistivity, at high voltage (about 9 V) the avalanche breakdown effect can be observed in structures isolated by *pn*-junction.

6 Conclusions

In the present study a new approach for the fabrication of BSOI-wafers was demonstrated that allows the fabrication of BSOI wafers with a well-defined wafer edge. The

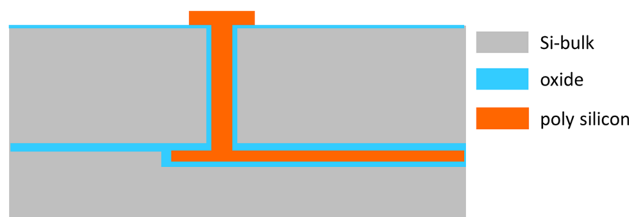

Fig. 10 Schematic representation of the next step, by defining isolation paths in the handle wafer

critical process steps during the formation of the BSOI wafer, wafer bonding, wafer-edge shaping, thinning of the device wafer, and the contact formation from the surface to the handle wafer were discussed.

The results allow the next step, which will be the realization of current paths also in the handle wafer either by doping or oxide isolation (Fig. 10).

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