

High quality factor RF MEMS tunable capacitor

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Abstract This paper presents the design of a tunable capacitor that integrates two vertical comb-drive tunable capacitors and a parallel plate tunable capacitor. The parallel plate tunable capacitor is in the middle of the comb-drive tunable capacitors. The vertical comb-drive part has sets of fixed and moving fingers while the parallel plate has fixed and moving plates. The capacitor is fabricated using the MetalMUMPs microfabrication process, which has only one thick structural layer i.e. metal (20 μm nickel and 0.5 μm gold). The nickel of the metal layer is subject to residual stress gradients along its thickness. After release of the metal layer, the stress gradients bend the curve-up beams to raise the moving fingers and the moving plate of the capacitor above the substrate and the fixed plate. Hence, one structural layer (i.e. the metal) is used to form the moving and the fixed comb fingers without requiring two structural layers. Vertical comb-driven tunable capacitors offer high capacitance density when a large number of fingers with narrow gap are used. Therefore, high capacitance ratio and high quality factors can be achieved by using vertical comb-drives with in a relatively small device area compared to lateral comb-drives. The parallel plate driving part increases the displacement and capacitance ratio while reducing the actuation voltage required for driving the capacitor. The quality factor and tuning ratio of the fabricated tunable capacitor are 118.5 and 101% at 0.8 GHz; respectively at a driving voltage of 100 V. Based on the experimental results of the fabricated tunable capacitor, an optimized design is presented for both high tuning ratio and

high quality factor. The tuning ratio of the optimized capacitor is found to be 143.1% at a “pull-in” displacement of 9.5 μm and a “pull-in” voltage of 90 V. The quality factors of the optimized capacitor are 520 at 0 V and 363.5 at 90 V, respectively at 0.8 GHz. The tunable capacitor achieves a displacement of more than one-half of the gap between the parallel plates without “pull-in” effect.

1 Introduction

Quality factor of tunable capacitors is an important figure of merit in the transfer of power of a signal in RF circuits. Of the most commonly used tuning elements are the capacitors realized by using the pn-diodes and semiconductor capacitors. It is obvious that the pn-diodes and semiconductor tunable devices offer high tuning ratio (Rebeiz et al. 2009). However, these devices are known for high power consumption even though the driving voltage is low. Also these device possess non-linearity at high RF frequencies which limits their function (Sze and Ng 2005). Dielectric varactors, which operate via the tunability of the permittivity, have a high tuning ratio and the quality factor may be improved by modifications on design characteristic and the material properties used in the fabrication (Sze and Ng 2005). Various Barium-Strontium-Titanate (BST) dielectric based tunable capacitors were presented in Jakoby et al. (2004), Vicki Chen et al. (2004), Pervez et al. (2004), Vorobiev et al. (2005), Ayguavives et al. (2000), Auciello et al. (2004) and (Schafranek et al. 2009) at 1 MHz exhibiting a quality factor of nearly 300. Recently, STM microelectronics have a BST dielectric tunable capacitors having a quality factor of 60 (<http://www.st.com/en/emi-filtering-and-signal-conditioning/rf-tunable-capacitors.html?querycriteria=productId=SC1881>) at 1 GHz. However, the resistive

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loss, contact loss and the minimum permittivity, which is above one, degrade the quality factor at higher frequencies. PIN diodes acquire high power dissipation and the quality factors is sacrificed when high tuning ratio is demanded in the ON state. CMOS switches and pHEMT based non-tunable capacitor switching which is used as a capacitor array suffer from ON resistance loss and the coupling capacitance to the substrate that will reduce the quality factor.

On the other hand the power consumption of MEMS tunable capacitor is almost negligible (Rebeiz et al. 2009). Due to the moving parts of the micro-structures (Rebeiz 2003) air (air + thin dielectric film patched on the fixed part) is used to tune the capacitance continuously with small loss of power at high RF frequencies. As a result of low power loss MEMS capacitors are believed to offer high quality factor if a large gap between parallel electrodes is used. MEMS based tunable capacitors have been developed using surface micromachining processes (Young and Boser 1997; Ionis et al. 1998, 2001; Zou et al. 2000; Hoivik et al. 2001; Ehmke et al. 2000) to be used as a functional element in electronic circuits (Rebeiz 2003; Yao 2000). Most designs of tunable capacitors use two parallel plates separated by an air gap with a thin dielectric film attached to the fixed plate. However, the capacitors suffer from “pull-in” effect that limits the maximum travel range to one-third of the gap between the plates of the capacitor (Rebeiz 2003). Various MEMS tunable capacitors had been developed using parallel plates composed of different materials (Rebeiz 2003; Yao 2000; Young and Boser 1997; Dec and Suyama 1998; Jung et al. 2001; Zou et al. 2000; Hoivik et al. 2001; Ehmke et al. 2000; Rijks et al 2004) to enhance the quality factors or to minimize power losses. Switched type MEMS capacitors have been employed to provide discrete capacitances (Rijks et al 2004; Grichener et al. 2006; Grichener and Rebeiz 2010) to increase the travel range of the moving plate while keeping minimum power loss. Cascaded differential multi-fingers capacitor (Ionis et al. 2002) and inter-digital gold electrode zipper capacitors (Mahameed et al. 2010) were developed in an attempt to increase the tuning ratios and quality factors. However, such tunable capacitors can generally be classified as parallel plate based capacitors that always suffer from “pull-in” instability and thus limited to small displacement. Lateral comb-drives were also used to realize tunable capacitors (Rais-Zadeh and Ayazi 2007) for high tuning ratios and quality factors using high conductivity materials with a laboratory-developed fabrication process. Other in-plane comb-drives were also used to develop inter-digital tunable capacitors (Seok et al. 2002; Borwick et al. 2003) that operate at low frequencies. The disadvantage connected with laterally or in-plane driven comb-drive capacitor is the requirement of large gap which tends to increase the space occupied on the chip area (Nguyen et al. 2004). High tuning ratio and quality factor are obtained via different design configurations and high electric conducting materials. High quality factor is

normally obtained through the use of relatively larger size planar capacitor consisting of high conducting plates and lossless electrodes. Yoon and Nguyen (2000) developed a design of MEMS capacitor that moves dielectric between two parallel plates to achieve a tuning ratio of 40% and Q-factor of 218 at 1 GHz. Lee et al. (2008) found a quality factor of 60 at 2 GHz with a tuning ratio of 41% by using a floating top plate and thus avoiding signal passage through the mechanical springs of the capacitor. Angular vertical comb-drive capacitors were reported to have high tuning ratios and quality factors (Nguyen et al. 2004). However, the fabrication cost of vertical comb-driven capacitors and the lengthy fabrication steps are the challenges for the development of such tunable capacitors (Nguyen et al. 2004; Hailu et al. 2014, 2016).

This paper presents the design and performance of a high quality factor capacitor designed by integrating two vertical comb-drive and one parallel-plate tunable capacitors with large gap and thick metal structure. The measured S-parameters of the capacitor are used to calculate the quality factors and the tuning ratio of the fabricated tunable capacitor. The parasitic capacitance is extracted from the measured S-parameters. The parasitic capacitance arises from the RF pads, strips and the substrate of the capacitor and it is larger than the useful tunable capacitance. However, there is a room for increasing the tuning ratio and the quality factor without affecting the area occupied by the capacitor (i.e. optimizing the sizes of the structures of the capacitor). The optimization only affects the number of fingers, the length of fingers, the gap between fingers, the area of the parallel plate, the size of the plate supporting springs and the area of the RF pads and strips. By reducing the parasitic capacitance from the pads and strips the tuning ratio and quality factor are increased. The increased number of fingers, the area of the moving plate and fixed plate also offer large displacement (more than half of the gap between the parallel plates) at low driving voltages. The tunable capacitor can easily be batch fabricated at cheap cost using the standard microfabrication MetalMUMPs process which passed through series of development and optimization over 15 years.

This paper is organized as follows: Sect. 2 describes the design and principle of operation of the capacitor. Modeling and analytical results of the displacement of the capacitor are presented in Sect. 3. In Sect. 4, the quality factor, tuning ratio and power losses are determined from the measured S-parameters. The optimized design, its quality factor and tuning ratio are presented in Sect. 5. The work in the paper is finalized in Sect. 6.

2 Capacitor design and working principle

The capacitor design presented in this paper is developed using vertical comb-driven (VCD) capacitor units and

Fig. 1 Capacitor 3D view

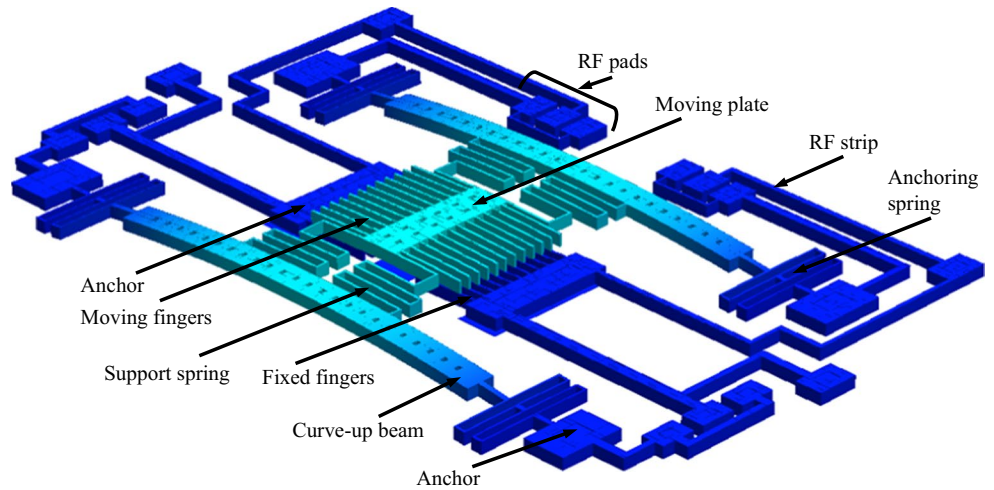
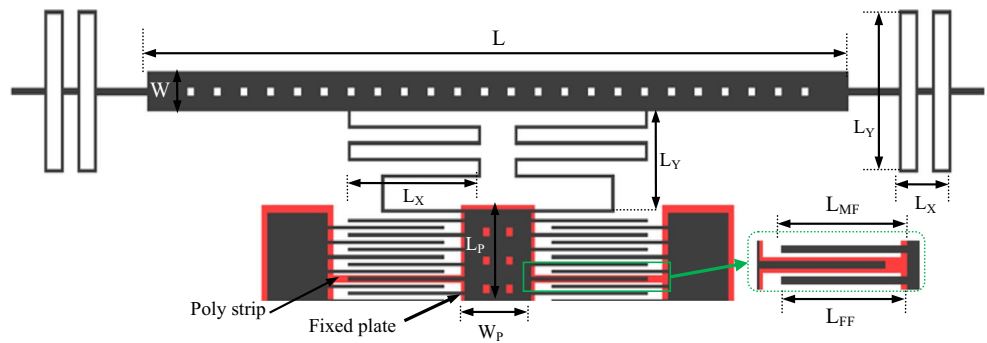


Fig. 2 Capacitor 2D layout (top half view)



a parallel plate-driven (PPD) capacitor unit (Hailu et al. 2016). The 3D view and 2D layouts of the tunable capacitor are shown in Figs. 1 and 2, respectively. The VCD capacitor units have vertically separated arrays of moving and fixed comb fingers. The PPD capacitor unit has two parallel plates: moving plate and fixed plate. The moving fingers are connected to the longer sides of the moving plate while the fixed plate is attached to the substrate underneath the moving plate. The moving plate and the moving fingers are connected to curve-up beams via supporting springs.

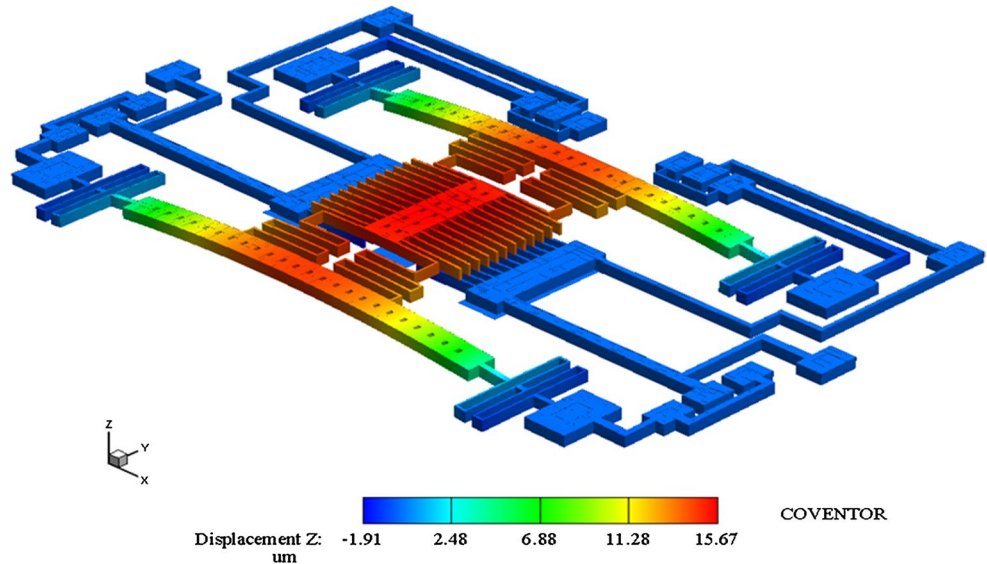
As discussed in (Hailu et al. 2014) the curve-up beams bend upward by the residual stress gradient in the nickel layer to leave a large gap between the moving and the fixed structures of the tunable capacitor. The moving structures of the capacitor are the moving plate and the moving fingers whereas the fixed structures are the fixed fingers and the fixed plate. The fixed plate is an electrode of the polysilicon (Poly) layer of the MetalMUMPs process (Cowen et al. 2002) which is embedded in the middle of silicon–nitride (Si_3N_4) layers, Nitride 1 and Nitride 2. The nickel layer is separated from the Nitride 2 layer by the sacrificial layer (Oxide2) of thickness $1.1 \mu\text{m}$ (Hailu et al. 2016). The fixed fingers and the fixed

Table 1 Capacitor dimensions (μm)

Structure	Length (μm)	Width (μm)	Number
Anchoring springs (L_y/L_x)	408	400	4
Curve-up beam (L)	2100	100	2
Fixed plate	471	220	1
Fixed fingers (L_{FF})	350	9	22
Moving fingers (L_{MF})	350	9	24
Moving plate (L_{FE}/W_F)	451	200	1
Support springs (L_x/L_y)	400	240	4
Release holes	20	20	64

plate are connected by a thin poly strip as shown in Fig. 2. Thus, the VCD and the PPD capacitor units are subjected to the same potential when a voltage is applied. Then, in the presence of driving voltage (a) the capacitance between the moving fingers and the fixed fingers and (b) the capacitance between the parallel plates are tuned simultaneously. The total tunable capacitance is, therefore, the sum of the capacitance between the VCD and the PPD units. Table 1 shows the dimensions of the structures of the tunable capacitor.

Fig. 3 Simulated structure of the capacitor



3 Modeling

3.1 Displacement of tunable capacitor

Before the removal of the sacrificial layer, the gap between the nickel and the Nitride 2 layer is only the thickness of Oxide 2, i.e. $1.1 \mu\text{m}$. At this point there is no vertical separation between the moving and the fixed fingers. After the removal of the sacrificial layer, the residual stress gradient in the Nickel layer bends the curve-up beams upward to lift the moving fingers and the moving plate above the substrate, the fixed fingers and the fixed plate. This upward displacement of the moving structures depends on the dimensions of the curve-up beams and the anchoring springs (Hailu et al. 2014). The displacement due to the bending of the curve-up beams is referred to as the initial displacement. The initial displacement of the moving plate is obtained using CoventorWare (2010) simulations. The average residual stress gradient and the Young's modulus of the nickel layer used in the simulation are $-4.72 \text{ MPa}/\mu\text{m}$ and 159 GPa (He et al. 2009). The deflection at the mid-point of the moving plate at $25 \text{ }^\circ\text{C}$ is found to be $15.67 \mu\text{m}$ from the simulation result. The expected gap between the moving plate and the fixed plate is $15.67 \mu\text{m}$ after fabrication. However, this gap may not necessarily be maintained on the fabricated prototype due to the inconsistency of the stress gradient in the fabricated prototypes (Hailu 2014). Figure 3 shows the initial displacement of the moving structures above the fixed plate without the substrate. The color map of Fig. 3 shows the moving structures (red) and the fixed structures (blue), respectively.

Under the presence of a voltage, the moving plate and the moving fingers move down towards the fixed plate and the fixed fingers. The “pull-in” displacement of the

capacitor is calculated using Eq. (1) (Hailu et al. 2016). The real root of Eq. (1) gives the “pull-in” displacement of the capacitor.

$$\left[\frac{gA}{2} + \frac{2nL}{d}g^3 \right] - 3 \left[\frac{A}{2} + \frac{2nL}{d}g^2 \right] z + \frac{6nL}{d}gz^2 - \frac{2nL}{d}z^3 = 0 \quad (1)$$

where g is the gap between the moving plate and the fixed plate (which is the initial displacement of the moving plate), A is the overlap area of the moving plate and the fixed plate, n is the number of fixed fingers, L is the overlap length between the fixed and the moving fingers, d is the horizontal distance between the fixed and the moving fingers and z is the downward displacement of the moving structures. With the gap $g = 15.67 \mu\text{m}$ and the given values of the geometric parameters in Table 1, the “pull-in” displacement is found to be $8.73 \mu\text{m}$ and the corresponding “pull-in” voltage is 107.2 V .

Figure 4 shows both analytical and measured displacement Vs voltage for the capacitor prototype.

3.2 Tuning capacitance

As illustrated in Fig. 1 the VCD and the PPD units of the capacitor share the same RF input port. Thus, the equivalent capacitance network can be considered as a parallel connection of the two comb capacitors and the parallel plate capacitor. Then, the total capacitance is given as the sum of the capacitances between the comb-drives of the VCD and the parallel-plates of the PPD. Mathematically, the capacitance is expressed as:

$$C = C_{CD} + C_{PP} + C_{fringe} \quad (2)$$

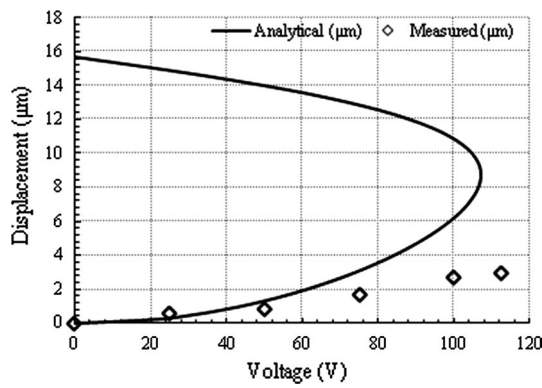


Fig. 4 Analytical and measured displacements vs. voltage

where C represents the total capacitance, C_{CD} is the sum of the capacitance of the two combs on either side of the PPD unit, C_{PP} is the parallel plate capacitance and C_{fringe} is the fringing capacitance. The fringe capacitance, C_{fringe} , includes the fringe capacitances between the comb fingers and the parallel plates through the air. The fringe capacitance in this case is part of the tunable capacitance. When the moving structures are at the highest position (i.e. $g = 15.67 \mu\text{m}$) the fringing field is large whereas it decreases as the downward displacement of the moving structures increases (Rebeiz 2003). Using the geometric parameters of the capacitor Eq. (2) is expressed as:

$$C = \frac{2n\epsilon_0 L(z + z_0)}{d} + \epsilon_0 A \left(g - z + \frac{t_{Si_3N_4}}{\epsilon_r} \right)^{-1} + C_{fringe} \quad (3)$$

where ϵ_0 is the permittivity of air, n is the total number of the fixed fingers, L is the overlap length between the moving fingers and the fixed fingers, d is the horizontal distance between the moving fingers and the fixed fingers, z is the displacement of the moving structures at any driving voltage, z_0 is the initial vertical overlap between the moving fingers and the fixed fingers, A is the area of the PPD unit, g is the initial gap between the moving plate and the fixed plate, $t_{Si_3N_4}$ is the thickness of the Nitride 2 layer and ϵ_r is the relative permittivity of Nitride 2. The Nitride 2 layer has a thickness of $0.35 \mu\text{m}$ and relative permittivity, ϵ_r of 8 (Cowen et al. 2002). Equation (3) is rewritten as:

$$C = \frac{2n\epsilon_0 L(z + z_0)}{d} + \frac{\epsilon_0 A}{g - z + 0.04375} + C_{fringe} \quad (4)$$

However, since there is no mathematical function in closed form that exactly determines the fringing capacitance in Eq. (4), simulation is used to compute the total capacitance C . At zero displacement (i.e. $z = 0$ or just at the initial overlap, z_0), the total capacitance is minimum. The initial overlap is $z_0 = 4.83 \mu\text{m}$ which is obtained by

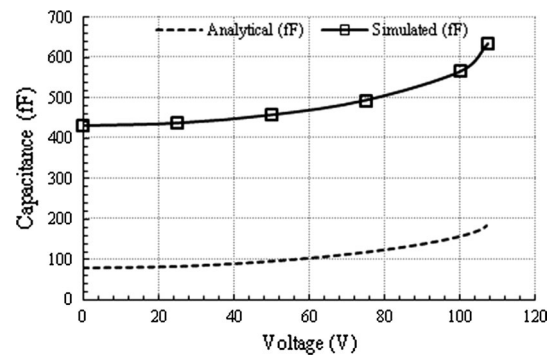


Fig. 5 Capacitance-voltage curve

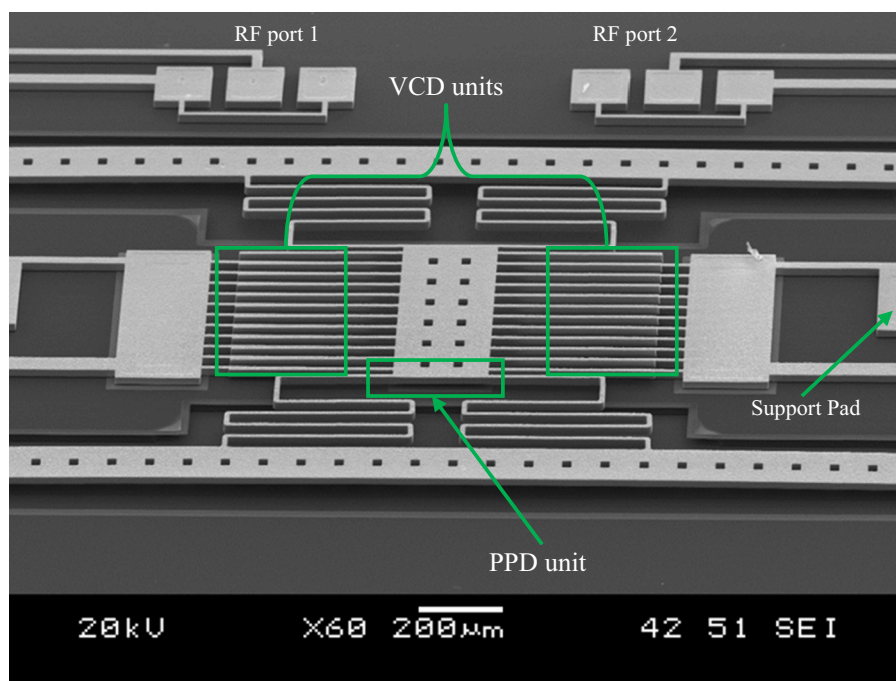
subtracting the initial displacement from the nominal thickness of the Metal layer. With CoventorWare simulation the capacitance is found to be 431.2 fF at $z = 0 \mu\text{m}$ (0 V) and 634.5 fF when the moving plate travelled $8.73 \mu\text{m}$ (107.2 V). The corresponding tuning ratio is 147.1% without parasitic capacitances from strips, pads and substrate. Figure 5 shows the capacitance–voltage plot that compares the simulated capacitance and calculated capacitance.

3.3 Parasitic capacitance

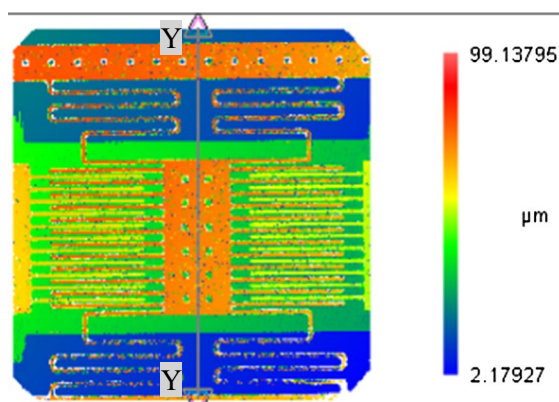
The parasitic capacitances include capacitances of the silicon substrate, anchors, RF pads and strips. The parasitic capacitances from the pads and strips to the substrate are calculated using a metal-dielectric-substrate model (Bakri-Kassem and Mansour 2004). The dielectric layers that generate parasitic capacitance under the strips include: Isolation oxide, Nitride 1, Nitride 2 and Oxide 2 (sacrificial layer between Nitride 2 and the Metal layer) with dielectric constants of 3.9, 8, 8 and 4, respectively (Bakri-Kassem and Mansour 2004). After release, the Oxide 2 layer is replaced by an air gap under the strips, thus the dielectric constant becomes 1.0. However, for the pads, the Oxide 2 layer is etched away by an anchor mask to create connection to the substrate. Thus the dielectric layers under the pads are Isolation oxide, Nitride 1 and Nitride 2 only. The equivalent dielectric constant (ϵ_{eq}) of the dielectric layers between the RF pads, strips and the substrate are calculated using Eq. (5).

$$\epsilon_{eq} = \left(\sum_{n=1}^N \frac{t_n}{\epsilon_n} \right)^{-1} \left(\sum_{n=1}^N t_n \right) \quad (5)$$

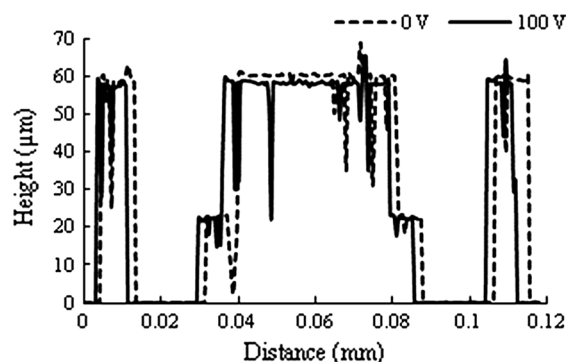
The equivalent dielectric constant for the pads and strips are calculated to be 4.6 and 2.25, respectively using Eq. (5). The total thickness of the dielectric layers is $2.7 \mu\text{m}$ (Cowen et al. 2002) under the pads and $3.8 \mu\text{m}$ under the strips. The total area of the pads and strips that is subject



(a)



(b)



(c)

Fig. 6 Fabricated tunable capacitor: **a** SEM image, **b** optical image of surface profile, **c** profile plot through the mid-point of the moving plate along line Y–Y

to the RF signal is $591,486 \mu\text{m}^2$ in the original design (Fig. 1). The simulated parasitic capacitance of the strips and the RF signal pad is 0.635 pF . The simulated parasitic capacitance of the substrate is 0.45 pF . The parasitic capacitance is the sum of the parasitic capacitance of the strip, the pads and the substrate. The simulated capacitance of the VCD and PPD units is 431.2 fF at 0 V (Sect. 3.2). The total simulated capacitance of the capacitor (i.e. the sum of the capacitance of the VCD, PPD units and the parasitic capacitance) is found to be 1.5162 pF .

4 Experiments

4.1 Displacement measurement

The prototypes of the capacitor were fabricated using the MetalMUMPs process to verify the design principle and extract measurement results. The magnified views of the VCD units, the PPD unit and the RF ports of the capacitor are labeled as shown in the SEM image of the tunable capacitor, in Fig. 6a. The profile measurement along line YY which

passes through the midpoint of the moving plate (Fig. 6 (b)) of the capacitor verified that the moving structures are raised above the substrate by the bending of the curve-up beams after the nickel structures are released. Additional layout, Support pad, is added to Fig. 1 to avoid the bending of the RF strip due to the stress gradient and to keep better uniformity of metal layer deposition during the fabrication process (Hailu 2014). This structure is labeled as shown in Fig. 6a. The measured gap between the moving plate and the fixed plate along line YY is 17.05 μm. This measured gap is 1.38 μm higher than the simulated gap which could happen as a result of non-uniformity of the nickel layer deposition during fabrication (Cowen et al. 2002; Hailu 2014).

As the surface color map in Fig. 6b shows, the moving fingers are also lifted above the fixed fingers. The deformation due to the residual stress gradient has curving effect on all the structures of the nickel as discussed in (Hailu et al. 2014). However, since the length of fixed and the moving fingers are 350 μm the bending of the tips of the fingers is negligible (Hailu 2014). The measured initial vertical overlap between the moving and the fixed fingers is 2.45 μm.

Voltages are applied across to the capacitor to verify the downward displacement of the moving structures. At 100 V the measured displacement is 2.91 μm as illustrated in Fig. 6c.

4.2 Quality factor

The scattering parameters (S-parameters) are measured to determine the quality factor and the tuning ratio of the tunable capacitor. The measured S-parameters are converted to transmission line (ABCD) parameters (Pozar 2005) to calculate the impedance using Eq. (6).

S - parameters → ABCD parameters in terms of S - parameters

$$[S] \rightarrow \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \rightarrow \begin{bmatrix} \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} & Z_0 \frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{2S_{21}} \\ \frac{1}{Z_0} \frac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{2S_{21}} & \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}} \end{bmatrix}$$

where $A = 1$, $B = 0$, $D = 1$ and $C = Z$ represents the impedance of the capacitor, S_{11} is the reflection coefficient at input port, S_{22} is the reflection coefficient at output port, S_{12} the transmission coefficient from input to output port and S_{21} is the transmission coefficient from output to input port. Using the ABCD parameters the entire tunable capacitor is modeled as a two-port impedance network. From the impedance, the real and imaginary parts are extracted to calculate the quality factor using Eq. (7).

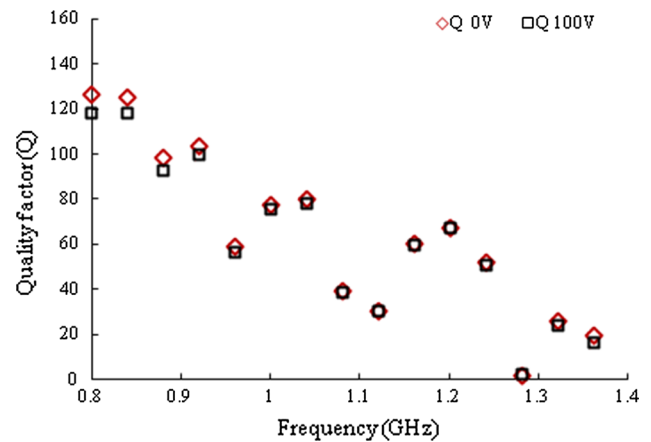


Fig. 7 Quality factor plot at 0 and 100 V

$$Quality\ factor\ (Q) = \frac{1}{2\pi f C R} \tag{7}$$

where f is the RF signal frequency, C is the capacitance (referred to as measured capacitance in the remainder of this paper) and R is the resistance of the capacitor.

The maximum voltage applied across the tunable capacitor to measure the S-parameters is limited to 100 V to protect the vector network analyzer (VNA) from the damage caused by high voltages. As the voltage is increased from 0 to 100 V with a step of 25 V, the capacitance increases whereas the quality factor decreases. The quality factors at 0 V and 100 V are found to be 126.7 and 118.5, respectively at 0.8 GHz. At 1.24 GHz the quality factors are 51.9 and 50.8 for 0 and 100 V, respectively. Figure 7 shows the quality factor plot vs. frequency.

4.3 Tuning ratio

The tuning ratio is calculated using the capacitances from the ABCD parameters which were obtained from the measured S-parameters in Sect. 4.2. The capacitance is calculated from the imaginary part of the impedance $Z = R + (j 2\pi f C)^{-1}$ of the ABCD parameters. The tuning ratio is ratio of the capacitance at the maximum actuation voltage to the capacitance at the minimum actuation

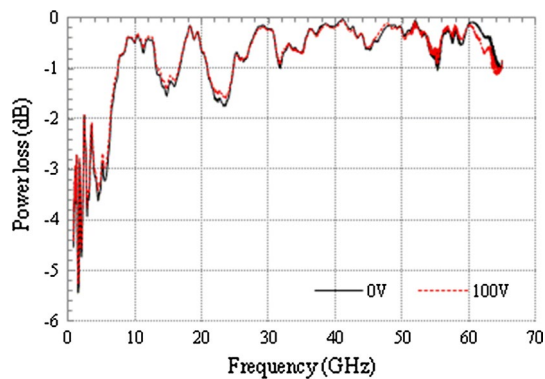


Fig. 8 Power loss curve at 0 and 100 V

voltage, C_{100V}/C_{0V} . The measured capacitances at 0 and 100 V are 1.5654 and 1.5799 pF, respectively. The tuning ratio of this tunable capacitor (C_{100V}/C_{0V}) is 101%. Comparison between the measured capacitance (1.5654 pF) with the simulated capacitance 1.5162 pF at 0 V shows an error of 3.14%.

4.4 Power losses

The RF power loss is calculated and plotted to show the power lost in the capacitor and the frequency ranges at which the capacitor can operate with reasonable power loss. The RF power loss of the capacitor is calculated using Eq. (8) (Pozar 2005) and graphed in dB versus the frequency.

$$\text{Power loss} = 1 - |S_{11}|^2 - |S_{21}|^2 \quad (8)$$

where S_{11} is the reflection coefficient at the input port and S_{21} is the power incident from the output port of the capacitor. In this design the power loss is lower for frequencies below 8 GHz. This clearly shows the presence of high quality factors for lower frequencies. The power loss increases for frequencies greater than 8 GHz due to the increase in reactive impedance of the capacitor. Figure 8 shows power loss curve at 0 and 100 V. As the driving voltage increases from 0 to 100 V the curve jumps upward indicating capacitance change and hence the impedance.

The high quality factor and the power loss up to 8 GHz show that the capacitor can be used for tunable filters that operate in L, S or C frequency bands (Pozar 2005). However, the useful capacitance of the capacitor is dominated by the parasitic capacitance and therefore it does not offer high tuning ratio. This design (Fig. 1) is optimized in the subsequent section for high tuning ratio together with high quality factor by increasing the capacitance change and reducing the parasitic capacitance from the RF pads and strips. In the optimized design the area surrounded by the curve-up beams is neither increased nor decreased.

5 Optimized design of the tunable capacitor

5.1 Optimized design

The tuning ratio of the capacitor is very low as determined in Sect. 4.2 due to high parasitic capacitance from the substrate, strips and pads. As explained in Sect. 4.3, the parasitic capacitance it is mostly from the substrate, pads and strips and it is less affected by the moving structures. The area occupied by the capacitor will not change in the optimization process as a result; the parasitic capacitance from the substrate remains the same. Since the RF signal is applied to the fixed fingers and the fixed plate through the RF pads, the substrate parasitic capacitance is not affected by the moving structures even if the “pull-in” displacement is reached. The two techniques used to obtain high tuning ratio and quality factors are increasing change of tunable capacitance (ΔC) and reducing parasitic capacitance. The total capacitance at any voltage is the sum of the initial capacitance C_0 at 0 V and the capacitance change (ΔC) brought by the increased driving voltage. The tuning ratio is thus given by $(C_0 + \Delta C)/C_0$. Higher capacitance change (ΔC) is obtained by appropriately selecting fingers length, width, the gap between fingers, and number of fingers (Hailu 2014). However, the area bounded by the curve-up beams remains unchanged.

The horizontal gap between the moving and the fixed fingers is 9 μm in the original design (Table 1), which is 1 μm larger than the allowed minimum gap (8 μm) between the structures of the Metal layer of the MetalMUMPs process (Cowen et al. 2002).

In order to increase the tuning ratio, four changes are made to the moving and fixed structures of Fig. 1: (1) the number of fingers is increased (2) the gap between the fingers is reduced to 8 μm (3) the length of the fingers is increased to 400 μm (4) the turns of the plate supporting springs are compacted. As a result of compacting the turns of the plate supporting springs the stiffness is increased from 27.44 to 34 N/m. Using Eq. (1) the “pull-in” displacement of the optimized design is found to be 9.5 μm and the corresponding “pull-in” voltage is 90 V.

The second method to optimize the tuning ratio is reducing the parasitic capacitance generated from RF pads and strips. Reducing parasitic capacitance from pads and strips also leads to high quality factor. Figure 9 shows the RF pads and strips in a more detailed manner with their corresponding labels. The GND (ground) pads are not responsive to RF signals (Bakri-Kassem and Mansour 2004), thus neglecting the strip connected to the GND pad has no effect on the capacitance or the quality factor.

As shown the RF input (RF in) port and the DC voltage pad (DC in) are separate in the original design but share common strip (Strip 2). The RF output (RF out) side (parts

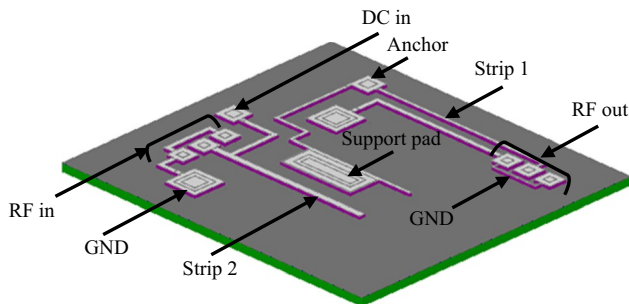


Fig. 9 RF pads and strips of original

Table 2 summary of Pads and strip sizes

Structure	Original design		Optimized design
	Pads (L × W)	Strips (L × W)	Strips (L × W)
RF out	120 × 120	2880 × 20	935.5 × 33
DC	140 × 140	1546.5 × 40	120 × 120 (pads)
RF in	120 × 120	1084 × 20	935.5 × 33

inside the pentagon) has the longest strip (Strip 1) and support pads which contribute to extra parasitic capacitance. These pads were purposely added in the original design (Fig. 1) (1) to minimize the non-uniformity and to ensure that the pattern of one chip design does not affect the Metal thickness of the other design on the same fabrication run (Cowen et al. 2002) and (2) to physically connect the strips to the substrate and thereby avoid any kind of movement or mechanical contact from the neighboring strips. The parts inside the pentagon (Fig. 9) are removed to reduce the parasitic capacitance and the resistance. The length of Strip 2 is slightly adjusted after leaving enough space for the RF and DC pads. A trench is cutout inside the substrate under the RF strips to reduce the parasitic capacitance contributed. Table 2 summarizes the dimensions of the RF pads, DC pads and strips.

The width of the strip is further adjusted to 33 μm to bring its characteristic impedance to 50 Ω standard microstrip transmission line (Pozar 2005). The parasitic capacitance without a trench is 0.218 pF for a strip size of 935.5 × 33 μm sq. With a trench of 25 μm depth in the substrate the parasitic capacitance from the strips becomes as low as 0.012 pF. The DC actuation voltage and the RF signal are applied via the RF pad.

In the optimized design the area of pads, strips, and anchors is reduced to 141, 391.5 μm sq., thus the simulated parasitic capacitance from the strips and pads to the substrate becomes 0.198 pF. In the optimized design the total parasitic capacitance is now 0.711 pF. Figure 10 shows

the completed 3D representation of the optimized tunable capacitor and the trench in the substrate.

Table 3 summarizes the optimized dimensions of the tunable capacitor design compared with the original design.

5.2 Tuning ratio and quality factor

The simulated capacitance of the VCD and the PPD units at the “pull-in” displacement (i.e. at 9.5 μm and 90 V) is 1.535 pF and 0.859 pF at 0 V. The total capacitance of the optimized design (i.e. including the parasitic capacitance) at 90 V and 0 V is 2.246 pF and 1.57 pF, respectively. The tuning ratio is therefore, 143% at the “pull-in” displacement.

The voltage-displacement curves for both the original and the optimized designs are plotted in Fig. 11 using analytical methods presented in (Hailu et al. 2016). As the curves show the optimized design brings down the “pull-in” voltage while increasing the travel range of the moving structures of the capacitor.

Figure 12 shows the simulated deformation of the optimized tunable capacitor without substrate at room temperature of 25 °C. The addition of the fingers caused a 0.07 μm increase in the deflection at the midpoint of the moving plate compared to the original design. The tips of the moving fingers bent down by 2.53 μm with reference to the midpoint of the moving plate (which is 2.11 μm for the original design). The deflection at the midpoint of the moving plate is 15.74 μm. The tips of the fixed fingers bend 2.43 μm towards the substrate. However, the maximum bending of the tips of the fixed fingers expected be reduced to 1.1 μm (thickness of the sacrificial layer Oxide2) by the substrate in the real fabricated prototypes. The bending at the tips of the fingers has very minimum effect on the performance of the prototypes as described in (Hailu et al. 2014).

The total resistance between the RF pads and the fixed fingers is found to be 0.2438 ohms. The quality factors of this optimized design at 0.8 and 40 GHz are 520 and 10.4, respectively at 0 V. At the “pull-in” displacement the quality factors at 0.8 and 40 GHz are 363.5 and 7.3, respectively.

Figure 13 shows the capacitance-displacement and capacitance–voltage curves of the optimized tunable capacitor. The capacitance change show linear relationship with the increasing displacement. The capacitance–voltage linearity is found to be 89.4%.

Table 4 shows the summary of comparison between the quality factor and tuning ratio of the design of the tunable capacitor presented in this paper with the MEMS capacitors in the literature at frequencies above or 1 GHz.

Fig. 10 Optimized tunable capacitor **a** complete structure, **b** trench in the substrate

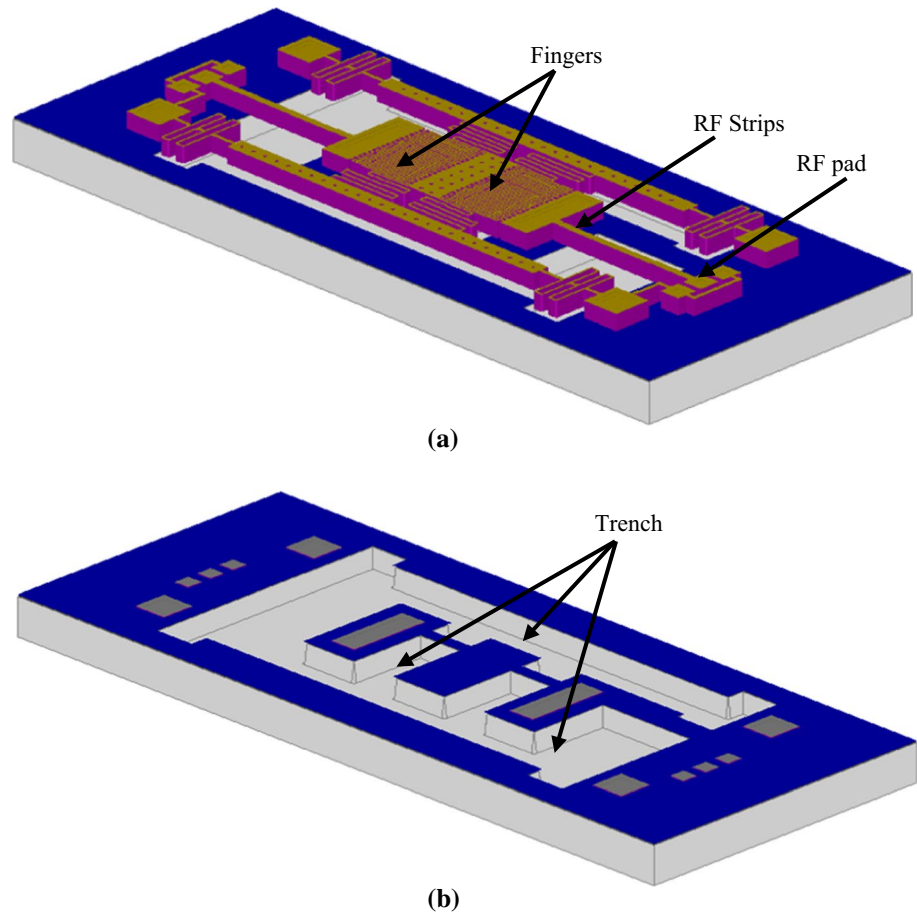


Table 3 List of optimized capacitor dimensions vs. original design

Parameters	Original design	Optimized design
Length of fixed/moving fingers	350 μm /350 μm	400 μm /400 μm
Width of fixed/moving fingers	9 μm /9 μm	8 μm /8 μm
Gap between fingers	9 μm	8 μm
Number of fixed fingers	22	32
Moving plate size	200 μm x 451 μm	200 μm x 556 μm
Deflection at midpoint of the moving plate	15.67 μm	15.74 μm at 25 $^{\circ}\text{C}$
Stiffness	27.44 N/m	34 N/m
“pull-in” displacement	8.73 μm	9.5 μm
“pull-in” voltage	107.2 V	90 V
Capacitance at 0 V	1.5654	1.57 pF
Capacitance	1.5799 at 100 V	2.246 pF at 90 V

6 Conclusion

A high quality factor tunable capacitor which integrated vertical comb-drive capacitors and parallel plate capacitor units is presented. The capacitor is fabricated using a

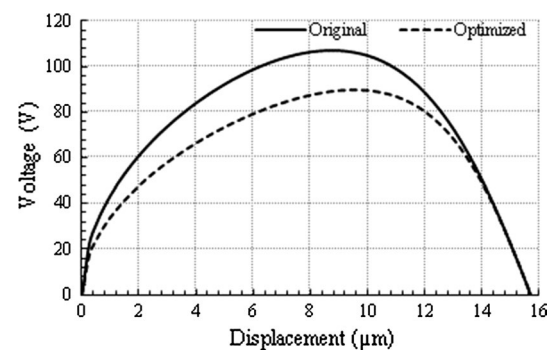


Fig. 11 Voltage-displacement curve of original and optimized design

thick nickel layer, MetalMUMPs, microfabrication process. Fabricated prototype measurement showed that quality factor 126.7 and tuning ratio of 101% has been achieved. The capacitor is optimized for high tuning ratio and high quality factor by increasing the number and length of fingers and reducing the parasitic capacitance. The maximum quality factor and tuning ratio of the optimized capacitor are 520 and 143.1%, respectively. The optimization of the capacitor structures also reduced the driving DC voltages.

Fig. 12 Simulated deformation of the optimized capacitor

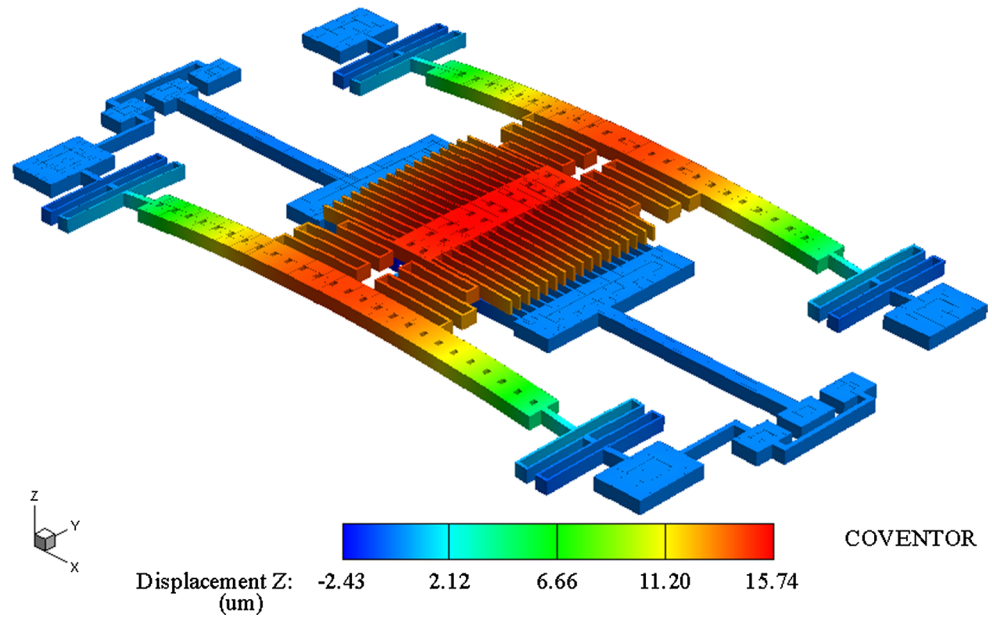


Fig. 13 Optimized capacitor curves **a** displacement-capacitance, **b** voltage-capacitance

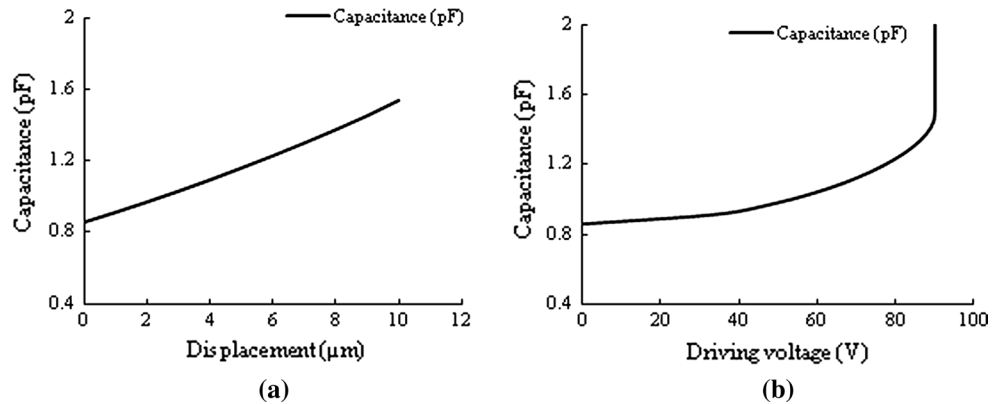


Table 4 Comparison with other MEMS capacitors

Reference	Tuning ratio	Quality factor
Young and Boser (1997)	16%	60, 1 GHz
Dec and Suyama (1998)	1.5–1.87	20, 1 GHz
Grichener et al. (2006)	1.5–2	225, X/Ku band
Grichener and Rebeiz (2010)	59	>100, C-X band
Ionis et al. (2002)	4	17, 1.5 GHz
Mahameed et al. (2010)	3:1	>100, 3 GHz
Rais-Zadeh and Ayazi (2007)	130%	>200, 1 GHz
Borwick et al. (2003)	8.4:1	>100, 200–400 MHz
Yoon and Nguyen (2000)	40%	218, 1 GHz
Lee et al. (2008)	41%	39.8, 1 GHz
Nguyen et al. (2004)	31:1	273, 1 GHz
Bakri-Kassem and Mansour (2004)	280%	13, 1 GHz
This work	143.1%	415.8, 1 GHz

The capacitor can be used in the design of tunable filters that operate in L, S or C frequency bands. Since the capacitor has high travel range and fabricated using a thick micro fabrication process it could provide high power handling capability.

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