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TECHNICAL PAPER

Operational efficiency of novel SISO shift register under thermal randomness in quantum-dot cellular automata design

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Abstract For nano scale logic circuit, device area and power consumption are the major concerns. In this paper, the design of an optimized SISO shift register is explored based on quantum-dot cellular automata (QCA) device. The design is achieved in a single layer. To design the shift register circuit, a new QCA D flip-flop has been proposed. These new D flip-flop has minimum cell count and lower device area over existing designs. The proposed shift register also outperforms the existing designs by reducing cell count and area. The power consumption by the proposed design is carried out that shows the low energy consumption nature of the circuit. Logic gate, QCA cell and device density have been considered to evaluate the circuit. Simulation timing diagram and truth table of the proposed circuits are compared which shows that all the designs are functioning efficiently. Stability under thermal randomness for all the designs are analyzed which shows the steadiness of the designs. The impacts of control input, i.e., clock on the designs are explored. Besides the defects in proposed QCA layouts are also identified and excelled for fault free implementation.

1 Introduction

The enhancements in integration, operating speed, and power consumption of integrated circuits have been achieved by nanoelectronics engineering through past several decades. The enhancement is achieved with reducing the attribute size of different semiconducting components (Lent and Tougaw 1997; Lent et al. 2006; Kianpour and Sabbaghi-Nadooshan 2014; Tehrani et al. 2013; Hashemi and Navi 2014). But decrease in transistor size caused problems like excessive heat dissipation. As an alternative solution, QCA technology was invented by Lent and Tougaw (1997). QCA is a promising nanotechnology that can encode binary data beyond current switches. It has high circuitry areas, low power consumption and faster switching speed (Das and De 2010, 2011, 2012; Das et al. 2015, Das et al. 2016). The information in QCA circuit is possessed in the form of charge on electrons (Pradhan and De 2013; Thapliyal and Ranganathan 2010; Thapliyal et al. 2013; Das and De 2015a, b). The columbic interaction between each QCA cell is responsible for information to carry from input to output within QCA circuit (Sardinha et al. 2013; Arjmand et al. 2013; Ghosh et al. 2014a, b, 2015). To store digital information, registers are essential component. This paper shows an optimized design and implementation of D flip-flop and 3-bit serial-in-serial-out (SISO) shift register using QCA.

This paper has the contributions as follows.

1. A new QCA layout of D flip-flop.
2. Optimized design of SISO shift register in QCA using proposed D flip-flop.
3. The detailed comparison of proposed D flip-flop and shift register circuit with existing layouts are explored. During comparison, cell count and device density are considered.
4. Defects in proposed QCA layouts are identified and excelled. To detect those defects, test vectors are also proposed.
5. The power consumption by the proposed designs is estimated.

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6. The stability of the layouts under thermal randomness is also deliberated.
7. The impact of control input i.e., clock on the designs are also explored.

The paper is oriented as follows. Section 2 shows QCA overviews. The design and implementation of proposed D flip-flop and 3-bit SISO shift register based on QCA is describe in Sect. 3. Section 4 outlines the simulation outputs including design complexity, comparison with existing layouts, power dissipation estimation and stability analysis of the proposed circuits under thermal randomness. At the end, the conclusion is drawn in Sect. 5.

2 QCA overview

A QCA cell consists of four quantum dot lies at the four corner of the cell as shown in Fig. 1a. Each of these cell occupies two mobile electrons (Lent et al. 2006; Kianpour and Sabbaghi-Nadooshan 2014; Hashemi and Navi 2014). Depending on the electronic charge of the electrons, the QCA cell possesses its polarization. Two polarized states are $P = +1$ and $P = -1$ respectively, and the binary information stored within them is 1 and 0 respectively. $P = 0$ means an un-polarized cell, i.e., the cell does not contains any information (Ghosh et al. 2014b; Das et al. 2012, 2013; De et al. 2013). Majority voter (MV) (Das et al. 2013; Silva et al. 2015; Sen et al. 2014; Pudi and Sridharan 2011; Debnath et al. 2016a, b) is the main building block of QCA circuit. It consists of five cells as shown in Fig. 1b. The logic expression for MV is obtained in Eq. (1)

$$MV(P, Q, R) = PQ + QR + RP \quad (1)$$

When one of the inputs of the MV is set to '0', the logic AND-gate is formed and if it is set to '1', logic OR gate is produced as shown in Fig. 1c. QCA wire (Arjmand et al. 2013; Ghosh et al. 2014a) can be constructed by placing QCA cell sequentially as given in Fig. 1d. Larger circuit is produced in combination of QCA wire with the MV. When QCA cells are placed at 45°, they act as a NOT gate which is shown in Fig. 1e (Ghosh et al. 2014b; Das et al. 2012; Das and De 2016a, b, c, d, e, f, g).

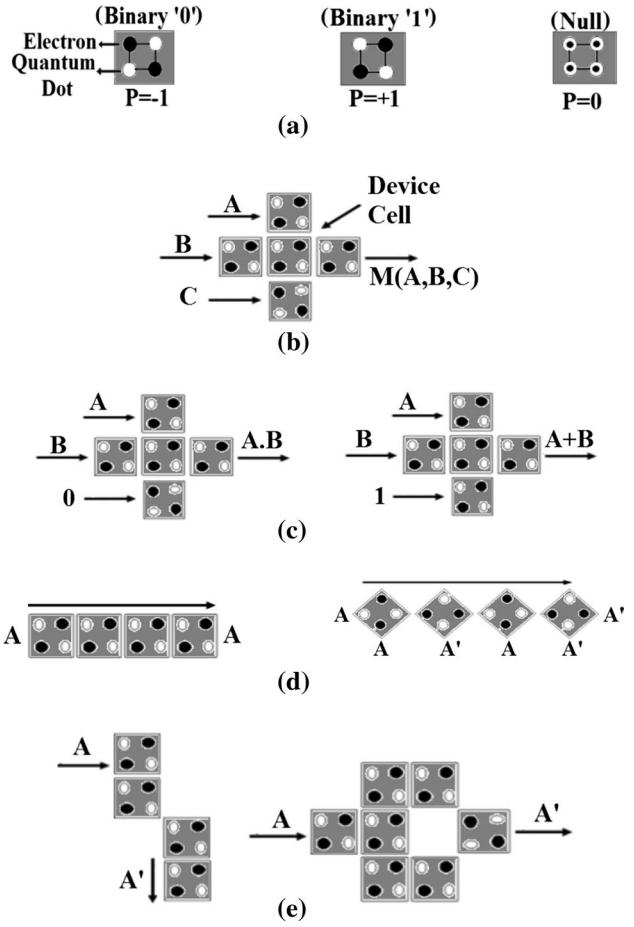


Fig. 1 QCA cell and logic gates **a** QCA cell structure, **b** majority voter **c** AND gate and OR gate **d** QCA 90° wire and 45° wire, **e** inverter

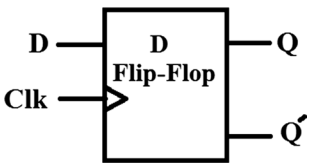


Fig. 2 Block representation of D flip-flop

3 Proposed work

3.1 QCA based D flip-flop

D flip-flop (Nelson et al. 1995) is a combinational circuit having one input and two outputs as shown in Fig. 2. Its characteristic expression is $Q(t + 1) = D$, where $Q(t + 1)$ represents the next state after every clock pulse. The

Table 1 Truth table of D flip-flop

Input		Output
D	Clk	Q
0	0	0
0	1	0
1	0	1
1	1	1

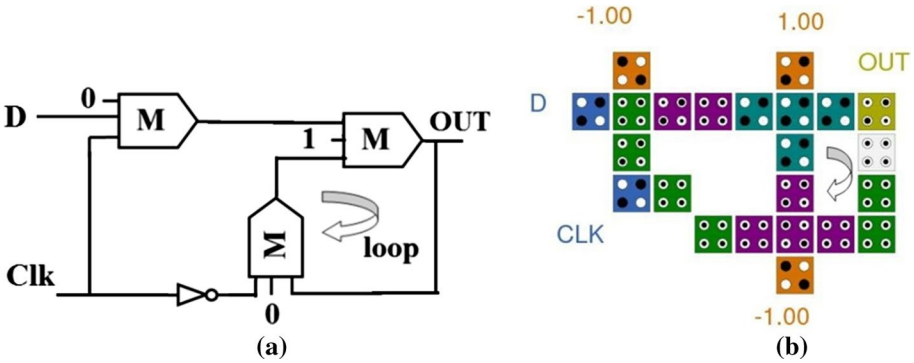


Fig. 3 D flip-flop **a** QCA schematic **b** QCA layout

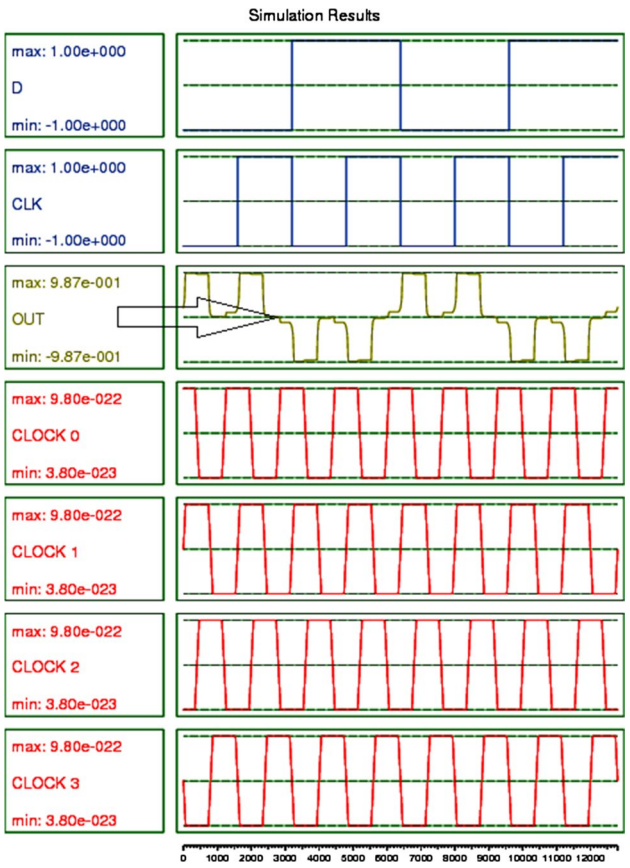


Fig. 4 Simulation result of proposed D flip-flop

truth table of D flip-flop is explored in Table 1. D flip-flop is basically R–S flip-flop having an inverter in place of input R. The inverter reduces the number of input of R–S flip-flop from two to one to form a D flip-flop. The proposed QCA schematic of D flip-flop and its QCA layout are shown Fig. 3a and b respectively. The structure of D flip-flop is achieved using a closed loop. Each QCA cell value within the loop stays in their current polarization until the clock value is altered. To design the circuit 3 MVs, 1 inverter, 23 QCA cell and 4 clocking zones are used. The latency of the circuit is 1. The simulation result is explored in Fig. 4. Outputs corresponding to inputs in Fig. 4 are shown by the arrow which describes that the required outputs are appeared after second clock pluses. The result is verified with the truth table as shown in Table 1. This verification confirms the accuracy of the circuit.

3.2 QCA based SISO shift register

A sequential circuit which can store and possess the digital data is called shift register (Nelson et al. 1995). Depending on the clock pulse, shift register advances the input signal from one bit to next MSB bit. Figure 5 shows a 3-bit SISO shift register, composed of three D flip-flops connected in a chain. The output of one flip-flop is used as an input to next flip-flop. All the flip-flops are driven through a common clock, and all are also set or reset concurrently. In Fig. 5, Q_1 and Q_2 are the intermediate states. Q_3 is the final output state. The proposed QCA schematic of shift register and its QCA layout are shown in Fig. 6a and b respectively. The QCA structure of 3-bit shift register is achieved by cascading three QCA D flip-flops. The layout consists of 9 MVs, 3 inverters, and 100 QCA cell. The latency of the circuit is 3. The simulation result is plotted in Fig. 6c. The arrows in Fig. 6c are used to show the outputs for each intermediate states and the final state corresponding to the inputs. The result is verified with theoretical values. This verification confirms the accuracy of the circuit.

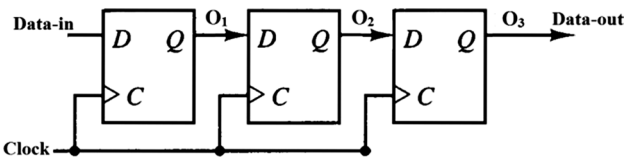


Fig. 5 Block diagram of 3-bit SISO shift register

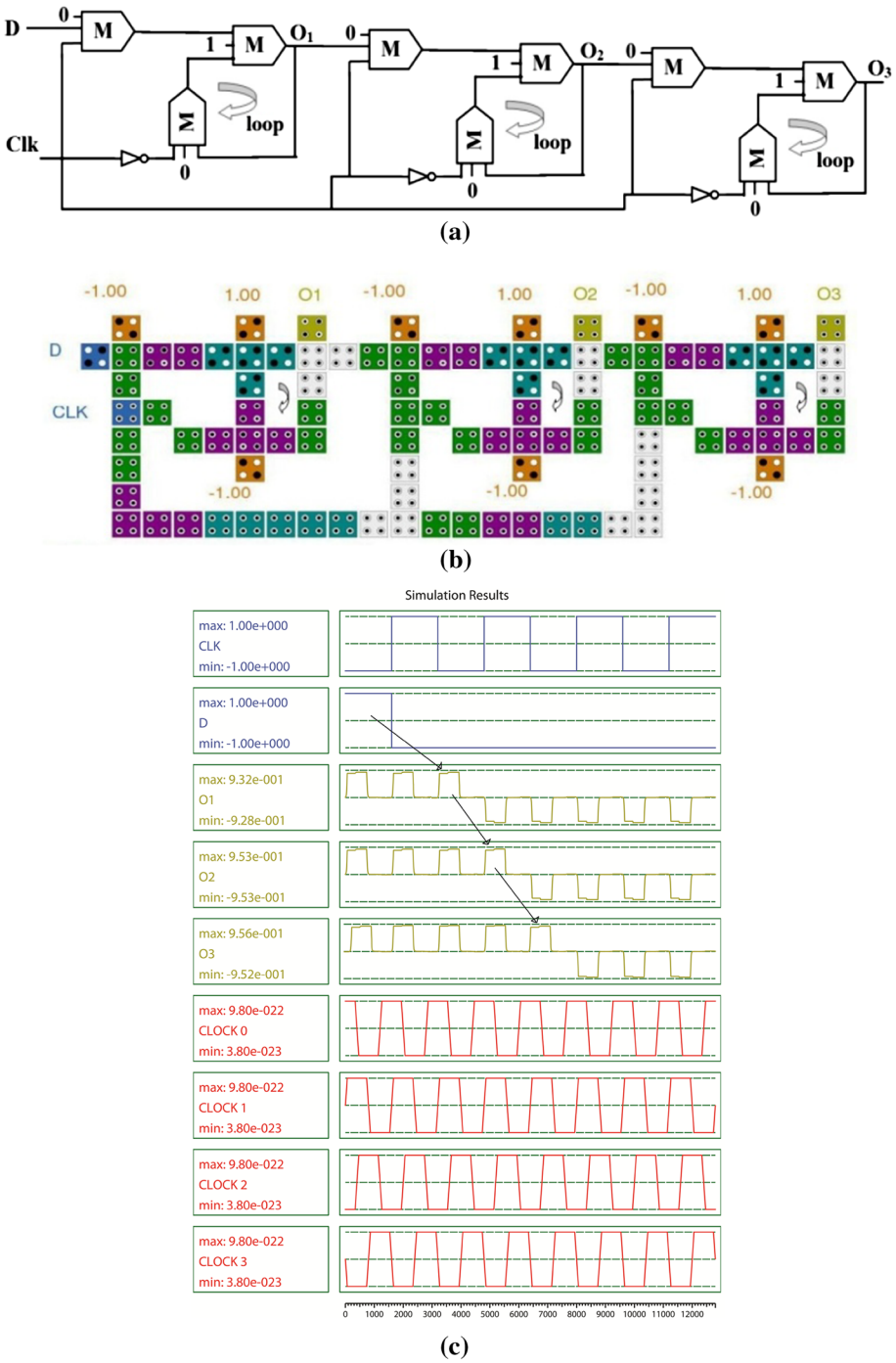


Fig. 6 Proposed 3-bit SISO shift register **a** QCA schematic, **b** QCA layout, and **c** simulation result

3.3 Impact of control input (Clk) on proposed designs

In this section the impact of control input (Clk) on the proposed designs are analyzed and explored. To perform this analysis, the layouts of proposed QCA D flip-flop and shift register as shown in Figs. 3a and 6a respectively are restructured. The new structures are based on individual input to different MVs which are shown in Fig. 7a and b respectively. Using this figures, the impact of control input (Clk) on proposed designs are observed and explored through Sects. 3.3.1 and 3.3.2 respectively.

3.3.1 Impact of control input (Clk) on proposed D flip-flop

The impact of control input (Clk) on the proposed D flip-flop, i.e., the changes in output due to Clk is described in

Table 2 Impact of Clk on the proposed D flip-flop

Clock status	q_1	q_2	Q
Stuck-at-0	0	Q	Q
Stuck-at-1	D	0	D
Transition from 0 to 1	D	0	D
Transition from 1 to 0	0	Q	Q

this section. The analysis is performed considering different clock status at the Clk. Suppose the input at Clk is stuck-at-0. Then the impacts on the output signal are as follows.

- The inputs of MV M_1 in Fig. 7a are as 0, D and 0 which results that the output of MV M_1, q_1, becomes 0.
- The inputs of MV M_2 are as Q, 1 and 0 which results that MV M_2 will have the output, q_2, becomes equal to Q.
- The inputs of MV M_3 are as q_1, 1 and q_2, i.e., 0, 1 and Q respectively, which results that the output of MV M_3, Q, becomes same as Q.

The result is shown in Table 2. Similarly, for different input status at the Clk, the impact on the output signal is carried out and explored through Table 2.

3.3.2 *Impact of control input (Clk) on proposed SISO shift register*

This section illustrates the impact of Clk on the proposed SISO shift register, i.e., the changes in output due to Clk. The analysis is performed considering different clock status at the Clk. Suppose the input at Clk is stuck-at-0. Then the impacts of control input (Clk) on SISO shift register, i.e., the changes in output due to control input are as follows.

- The inputs of MV M_1 in Fig. 7b are as 0, D and 0 which results that the output of MV M_1, q_1, becomes 0.
- The inputs of MV M_2 are as 1, 0 and O_1 which results that MV M_2 will have the output, q_2, becomes equal to O_1.
- The inputs of MV M_3 are as q_1, 1 and q_2 i.e., 0, 1 and O_1 respectively, which results that the output of MV M_3, O_1, becomes same as O_1.
- The inputs of MV M_4 are as 0, O_1 and 0 which results that the output of MV M_4, q_3, becomes 0.
- The inputs of MV M_5 are as 1, 0 and O_2 which results that MV M_5 will have the output, q_4, becomes equal to O_2.
- The inputs of MV M_6 are as q_3, 1 and q_4 i.e., 0, 1 and O_2 respectively, which results that the output of MV M_6, O_2, becomes equal to O_2.
- The inputs of MV M_7 are as 0, O_2 and 0 which results that the output of MV M_7, q_5, becomes 0.
- The inputs of MV M_8 are as 1, 0 and O_3 which results that MV M_8 will have the output, q_6, becomes equal to O_3.
- The inputs of MV M_9 are as q_5, 1 and q_6 i.e., 0, 1 and O_3 respectively, which results that the output of MV M_9, O_3, becomes same as O_3.

The result is shown in Table 3. Similarly, for different status at the Clk, the impact on the output signal is carried out and excelled through Table 3.

4 Result and discussions

The design as well as simulation of the proposed layouts has been performed on QCA Designer simulation tool (Walus et al. 2004). Parameters which are considered during simulation are shown in Fig. 8. The dimension of each QCA cell is 18 nm × 18 nm. The coherence vector technique and Euler method are employed during simulation.

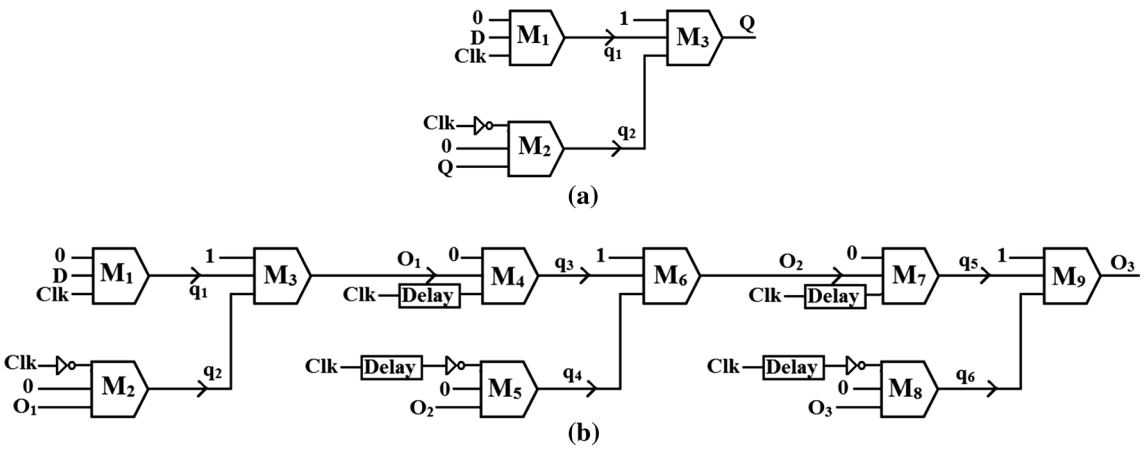


Fig. 7 Individual input based restructure schematic of **a** Proposed QCA D flip-flop and **b** Proposed 3-bit SISO shift register

Table 3 Impact of Clk on the proposed SISO shift register

Clock status	q_1	q_2	O_1	q_3	q_4	O_2	q_5	q_6	O_3
Stuck-at-0	0	O_1	O_1	0	O_2	O_2	0	O_3	O_3
Stuck-at-1	D	0	D	D	0	D	D	0	D
Transition from 0 to 1	D	0	D	D	0	D	D	0	D
Transition from 1 to 0	0	O_1	O_1	0	O_2	O_2	0	O_3	O_3

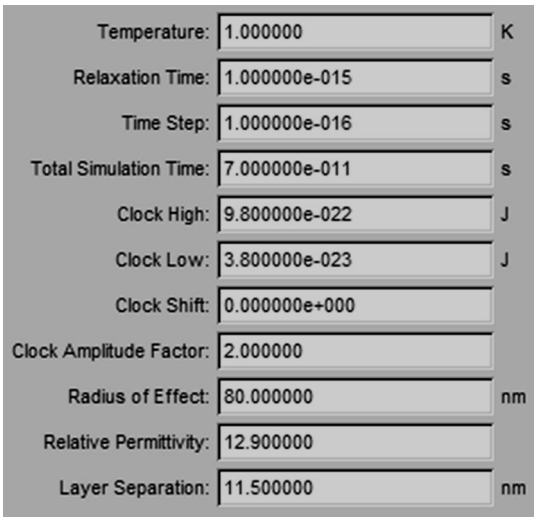


Fig. 8 List of parameters

4.1 Comparison with existing layouts

The comparison of proposed QCA D flip-flop and shift register circuit with previously reported designs in terms of circuit complexity are shown in Tables 4 and 5, respectively. Table 4 describes that the proposed QCA circuit of D flip-flop has less cell count and high device density than existing ones (Mustafa and Beigh 2014; Ahmad et al. 2014; Goswami et al. 2014; Lim et al. 2012; Xiao and Ying 2012; Hashemi and Navi 2012). Similarly from Table 5, it can be conclude that proposed shift register circuit has also less cell count and high device density than that of existing ones (Mustafa and Beigh 2014; Ahmad et al. 2014).

4.2 Defect analysis

In QCA circuit, defects may occur in three conditions as follows.

1. Single missing cell.
2. Single additional cell.
3. Misalignments of cell.

Among them, single missing cell and single additional cell based defects are most important (Sen et al. 2014). Thus in this paper, the defect analysis on proposed QCA circuits are performed based on single missing cell and single additional cell. The defect analysis is carried out as follows.

1. First, each cell of proposed QCA D flip-flop is marked according to their grid position as shown in Fig. 9. For

Table 4 Proposed QCA D flip-flop and existing layouts

QCA circuit of D flip-flop	Cell count	Total area (μm^2)	Cell area (μm^2)	Area usage (%)
Proposed	23	0.016	0.007	43.75
Existing circuit (Goswami et al. 2014)	30	0.03	0.009	30
Existing circuit (Ahmad et al. 2014)	33	0.027	0.010	37.03
Existing circuit (Mustafa and Beigh 2014)	35	0.027	0.011	40.74
Existing circuit (Hashemi and Navi 2012)	48	0.05	0.015	30
Existing circuit (Xiao and Ying 2012)	93	0.13	0.030	23.07
Existing circuit (Lim et al. 2012)	104	0.20	0.033	16.5

Table 5 Proposed QCA shift register and existing layouts

QCA circuit of shift register	Cell count	Total area (μm^2)	Cell area (μm^2)	Area usage (%)
Proposed	100	0.065	0.032	49.23
Existing circuit (Mustafa and Beigh 2014)	142	0.122	0.046	37.70
Existing circuit (Ahmad et al. 2014)	150	0.125	0.049	39.20

instance, the name 'B1' is assign just next to input cell 'D'. The term 'B1' indicates the Bth row and 1th column.
2. Next, simulation of D flip-flop circuit is performed using QCADesigner tool for each missing cell as well as for each additional cell.
3. The simulation results are observed and evaluated.

Based on simulation results, single missing/additional cells based all possible defects are identified and a list of test vectors are prepared to detect those defects. The results are excelled in Tables 6 and 7 respectively. Table 6 reflects that the output corresponding to missing cell 'B1' is '1'.

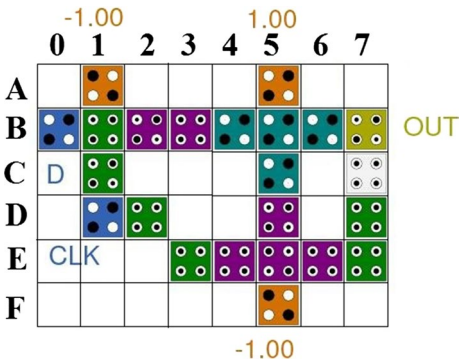


Fig. 9 Each cell of proposed QCA D Flip-Flop on their gird position

Table 6 Fault characterization of proposed QCA D flip-flop due to single missing cell

Position of missing cell (Fig. 9)	Test vector (AB)	Expected output (Q)	Faulty output (Q)
B1	01	0	1
B2	01	0	1
B3	01	0	1
B4	01	0	1
B5	11	1	0
B6	Fault free		
C1	01	0	1
C5	01	0	1
C7	01	0	1
D2	Fault free		
D5	01	0	1
D7	01	0	1
E3	11	1	0
E4	11	1	0
E5	11	1	0
E6	11	1	0
E7	11	1	0

Test vector <01> can be used to detect this kind of fault. The correct output of test vector <01> is '0'. Thus by comparing the correct output '0' and generated faulty output '1', the fault can be identified.

On the other side, Table 7 shows that the output corresponding to extra cell 'A0' is fault free whereas faulty output corresponding to extra cell 'A4' is '1', when 'A4' is in clock zone 1. Test vector <01> can be used to detect this kind of fault. The correct output of test vector <01> is '0'. Thus by comparing the correct output '0' and generated faulty output '1', the fault can be identified. The output corresponding to extra cell 'A4' is fault free if 'A4' stay in clock zone 2.

The same evaluation technique can be employed to detect all possible defects in the proposed shift register circuit.

Table 6 shows that in case of single missing cell based defect, test vector <01> has $(9/15) \times 100 = 60$ % fault coverage and <11> has $(6/15) \times 100 = 40$ % fault coverage. Thus, the test vector <01, 11> has $(60 + 40)\ \% = 100$ % fault coverage.

For single additional cell based defect, Table 7 shows that the test vector <01> has $(2/7) \times 100 = 28.571$ % fault coverage and <11> has $(5/7) \times 100 = 71.428$ % fault coverage. In this case, the test vector <01, 11> has $(28.571 + 71.428)\ \% = 100$ % fault coverage.

Therefore, the test vector <01, 11> provides 100 % fault coverage single missing/additional cell based defects.

4.3 Power dissipation by proposed circuits and existing layouts

In every clock cycle, Hamming distance between input variations is used to estimate the power dissipation of QCA inverter and QCA MV (Liu et al. 2012). For example, if inverter's input is switched either $0 \rightarrow 0$ or $1 \rightarrow 1$, the Hamming distance is taken as 0 and for either $0 \rightarrow 1$ or $1 \rightarrow 0$ switching; the Hamming distance is considered as 1. The switching in input $000 \rightarrow 000$ to MV, results in Hamming distance of 0 and for $000 \rightarrow 111$ switching, the Hamming distance is taken as 3 (Liu et al. 2012). Each QCA cell has identical power dissipation. In this paper, Hamming distance based approach proposed by Liu et al. (2012) is used in estimation the power dissipation by the layouts. The results are explored in Table 8. The estimation is carried out on temperature $T = 2.0\ K$ using different tunneling level. For example, each majority voter of D flip-flop circuit as shown in Fig. 3b has Hamming distance 2. To obtain the maximum power, Hamming distance 1 is considered for all inverters. Then at different tunneling level, the power dissipation calculation of the proposed D flip-flop layout is performed and plotted in Table 8. Similarly, the power dissipation by shift register circuit is estimated and shown in

Table 7 Fault characterization of proposed QCA D flip-flop due to single additional cell

Position of additional cell (Fig. 9)	Test vector (AB)	Expected output (Q)	Faulty output (Q)
A0, A2, A3	Fault free		
A4	01	0	1 (if cell A4 is in clock zone 1)
	Fault free (if cell A4 is in clock zone 2)		
A6, A7, C0, C2	Fault free		
C3	01	0	1 (if cell C3 is in clock zone 0)
	Fault free (if cell C3 is in clock zone 1)		
C4, C6, D0	Fault free		
D3	11	1	0
D4	11	1	0 (if cell D4 is in clock zone 0)
	Fault free (if cell D4 is in clock zone 1)		
D6, E0, E1	Fault free		
E2	11	1	0
F2, F3	Fault free		
F4	11	1	0 (if cell F4 is in clock zone 0)
	Fault free (if cell F4 is in clock zone 1)		
F6	11	1	0
F7	Fault free		

Table 8 Power dissipation at $T = 2.0\ K$ by proposed layouts

Tunneling energy level	D flip-flop (meV)	3-bit shift register (meV)
$\gamma = 0.25E_k$	104.3	312.6
$\gamma = 0.50E_k$	107.8	323.4
$\gamma = 0.75E_k$	113.0	339.0
$\gamma = 1.0E_k$	119.6	358.8

Table 8. The power dissipation at $T = 2.0$ K by proposed layouts are also shown in Fig. 10.

The comparison with existing designs in terms of dissipated energy is shown through Figs. 11and 12. Figure 11 represents the dissipated energy by proposed QCA D flip-flop and previously reported designs and Fig. 12 shows the dissipated energy by proposed QCA SISO shift register and existing ones. It is seen from Fig. 11 that the proposed QCA D flip-flop has slightly lower dissipated energy compare to the designs proposed by Mustafa and Beigh (2014), Ahmad et al. (2014), Goswami et al. (2014), Hashemi and Navi (2012) whereas compare to the designs reported by Lim et al. (2012) and Xiao and Ying (2012) the dissipated energy is very low. Similarly, proposed QCA SISO shift register has lower energy dissipation over previous circuits (Mustafa and Beigh 2014; Ahmad et al. 2014) as shown in Fig. 12. Thus, all the proposed designs have lower energy dissipation than the existing designs.

4.4 Stability of proposed QCA design

The stability of the proposed QCA D flip-flop and SISO shift register are demonstrated in this section. The evaluation is performed by simulating those circuits using coherence vector technique of QCA Designer tool (Walus et al. 2004). The simulation is performed in temperature (T) ranging from 1 to 15 K and by considering the relaxation time as 1.00e−015 s (Pudi and Sridharan 2011, 2012). The simulation results are examined to obtain maximum polarization (P_{max}), minimum polarization (P_{min}) and average polarization (P_{avg}) for each output cell of the designs. Here, K stands for Kelvin.

4.4.1 Stability of proposed QCA D flip-flop

P_{max}, P_{min} and P_{avg} for each output cell of proposed QCA D flip-flop are explored in Table 9. Table 9 shows that P_{max}, P_{min} and P_{avg} for output cell 'OUT' of QCA D flip-flop as shown in Fig. 3b, remain approximately same in different temperatures. The graphical representation corresponding to Table 10 is shown in Fig. 13. It is seen from Fig. 13 that within temperature 1–12 K, the value of P_{max}, P_{min} and P_{avg} have very little changes and QCA D flip-flop has an accurate output. But above 12 K temperature, the value of P_{max} and P_{min} drops dramatically which results faulty output. Thus the QCA circuit of D flip-flop is stable within

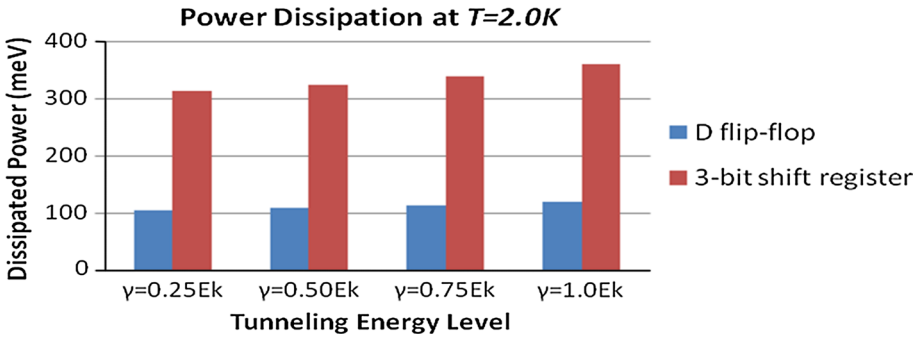


Fig. 10 Power dissipated by each proposed QCA layout

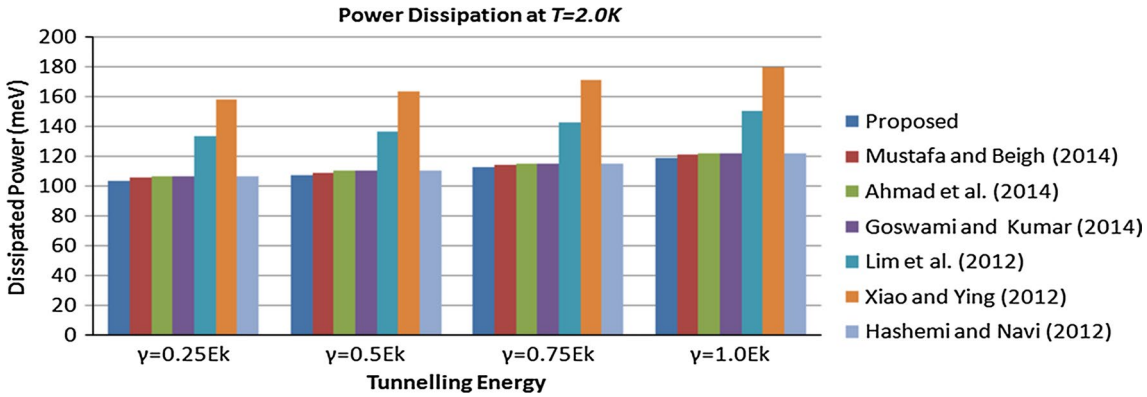


Fig. 11 Power dissipated by proposed QCA D flip-flop and existing designs

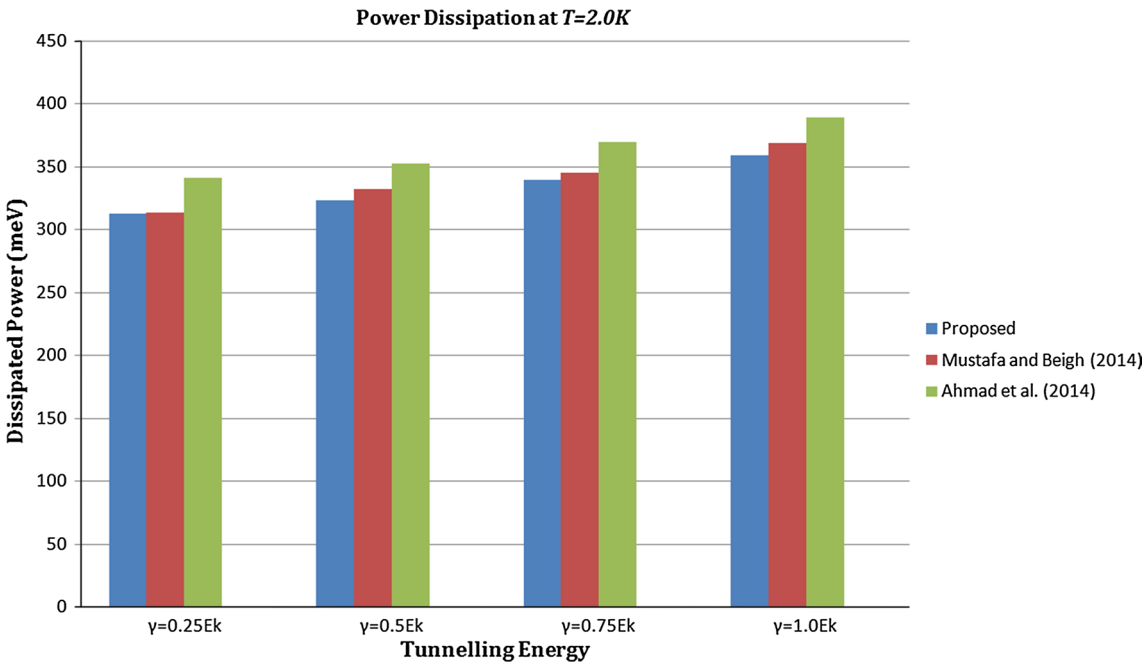


Fig. 12 Power dissipated by proposed QCA SISO shift register and existing designs

temperature 1–12 K. Similar approach can be used to measure the stability of proposed shift register circuit.

4.4.2 Stability of proposed QCA shift register

From simulation result, the polarization for each output cell under different temperatures are observed and explored through Table 10. Table 10 demonstrates that P_{max}, P_{min} and P_{avg} for each output cell decreases gradually by raising in temperatures. P_{max}, P_{min} and P_{avg} for output cell O_1, O_2, and O_3 are plotted in Figs. 14, 15 and 16 respectively. Figure 14 shows that the values of P_{max}, P_{min} and P_{avg} are lower if the temperature goes higher. But at any point of temperature level, P_{max}, P_{min} and P_{avg} have very little differences in their values. Though the polarization is dropped, up to 12 K temperature the output cell O_1 have correct outputs. But above 12 K temperature, the value of P_{max} and P_{min} are considerably lower which results in faulty output at output cell O_1. Similarly, from Figs. 15 and 16 it can also be seen that the values of P_{max}, P_{min} and P_{avg} getting lower and within temperature 1–12 K, the polarization is enough to produce correct outputs. Above these temperatures, the polarization is very low and the outputs are incorrect.

Finally the P_{avg} for all outputs of proposed shift register are plotted in Fig. 17 which shows that there are very small differences between average output polarization i.e., P_{avg} for the entire output cells O_1, O_2, and O_3. The circuit works efficiently under temperature range 1–12 K. Above 12 K, P_{avg} for any of the output cell is not well enough to produce correct output and the circuit becomes inefficient.

Table 9 Effect of temperature on output polarization of proposed QCA D flip-flop

T (K)	P_{max}	P_{min}	P_{avg}
1	9.87e−001	9.87e−001	9.87e−001
2	9.87e−001	9.87e−001	9.87e−001
3	9.87e−001	9.87e−001	9.87e−001
4	9.87e−001	9.87e−001	9.87e−001
5	9.87e−001	9.87e−001	9.87e−001
6	9.87e−001	9.87e−001	9.87e−001
7	9.86e−001	9.87e−001	9.86e−001
8	9.86e−001	9.86e−001	9.86e−001
9	9.85e−001	9.85e−001	9.85e−001
10	9.83e−001	9.83e−001	9.83e−001
11	9.79e−001	9.80e−001	9.79e−001
12	9.74e−001	9.76e−001	9.75e−001
13	9.66e−001	9.69e−001	9.67e−001
14	9.56e−001	9.60e−001	9.58e−001
15	9.42e−001	9.48e−001	9.45e−001

4.4.3 Stability of proposed QCA circuits and existing layouts

The comparison of proposed circuits with existing designs in terms of design stability is shown through Figs. 18 and 19. To perform evaluation, the average output polarization (P_{avg}) for the output cell has been considered.

Figure 18 represents the design stability of proposed QCA D flip-flop and previously reported designs and Fig. 19 shows the design stability of proposed QCA SISO shift register and existing ones. It can be seen from Fig. 18

Table 10 Effect of temperature on output polarization of proposed shift register

T (K)	Output (O_1)			Output (O_2)			Output (O_3)		
	P_{max}	P_{min}	P_{avg}	P_{max}	P_{min}	P_{avg}	P_{max}	P_{min}	P_{avg}
1	9.32e−001	9.27e−001	9.29e−001	9.53e−001	9.53e−001	9.53e−001	9.56e−001	9.51e−001	9.53e−001
2	9.32e−001	9.27e−001	9.29e−001	9.53e−001	9.53e−001	9.53e−001	9.56e−001	9.51e−001	9.53e−001
3	9.32e−001	9.25e−001	9.28e−001	9.54e−001	9.52e−001	9.53e−001	9.56e−001	9.51e−001	9.53e−001
4	9.32e−001	9.24e−001	9.28e−001	9.53e−001	9.52e−001	9.52e−001	9.55e−001	9.50e−001	9.52e−001
5	9.28e−001	9.20e−001	9.24e−001	9.52e−001	9.51e−001	9.51e−001	9.55e−001	9.49e−001	9.52e−001
6	9.21e−001	9.12e−001	9.16e−001	9.49e−001	9.47e−001	9.48e−001	9.52e−001	9.45e−001	9.48e−001
7	9.09e−001	8.99e−001	9.04e−001	9.44e−001	9.41e−001	9.42e−001	9.46e−001	9.39e−001	9.42e−001
8	8.93e−001	8.82e−001	8.87e−001	9.34e−001	9.31e−001	9.32e−001	9.38e−001	9.28e−001	9.33e−001
9	8.74e−001	8.61e−001	8.67e−001	9.21e−001	9.17e−001	9.19e−001	9.26e−001	9.14e−001	9.20e−001
10	8.52e−001	8.38e−001	8.45e−001	9.05e−001	8.99e−001	9.02e−001	9.11e−001	8.96e−001	9.03e−001
11	8.29e−001	8.13e−001	8.21e−001	8.86e−001	8.79e−001	8.82e−001	8.92e−001	8.88e−001	8.90e−001
12	8.15e−001	8.05e−001	8.10e−001	8.46e−001	8.39e−001	8.42e−001	8.72e−001	8.63e−001	8.67e−001
13	7.78e−001	7.71e−001	7.74e−001	8.41e−001	8.31e−001	8.36e−001	8.49e−001	8.27e−001	8.38e−001
14	7.53e−001	7.35e−001	7.44e−001	8.16e−001	8.04e−001	8.10e−001	8.26e−001	8.01e−001	8.13e−001
15	7.39e−001	7.08e−001	7.23e−001	7.66e−001	7.74e−001	7.70e−001	7.98e−001	7.93e−001	7.95e−001

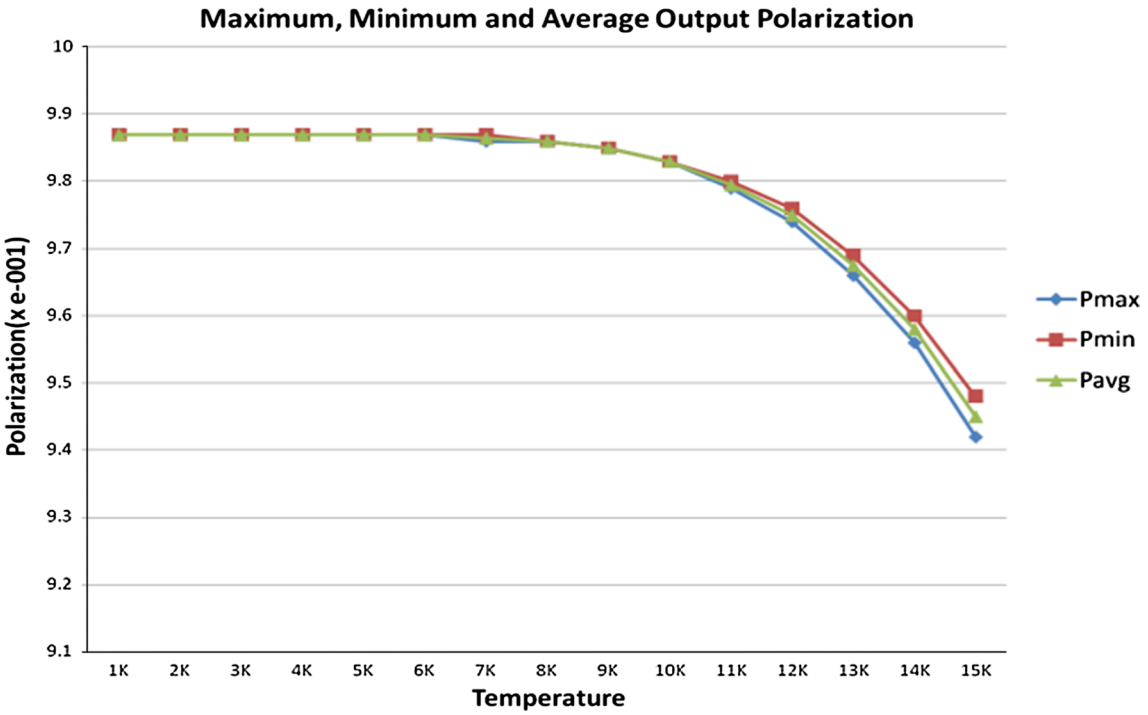
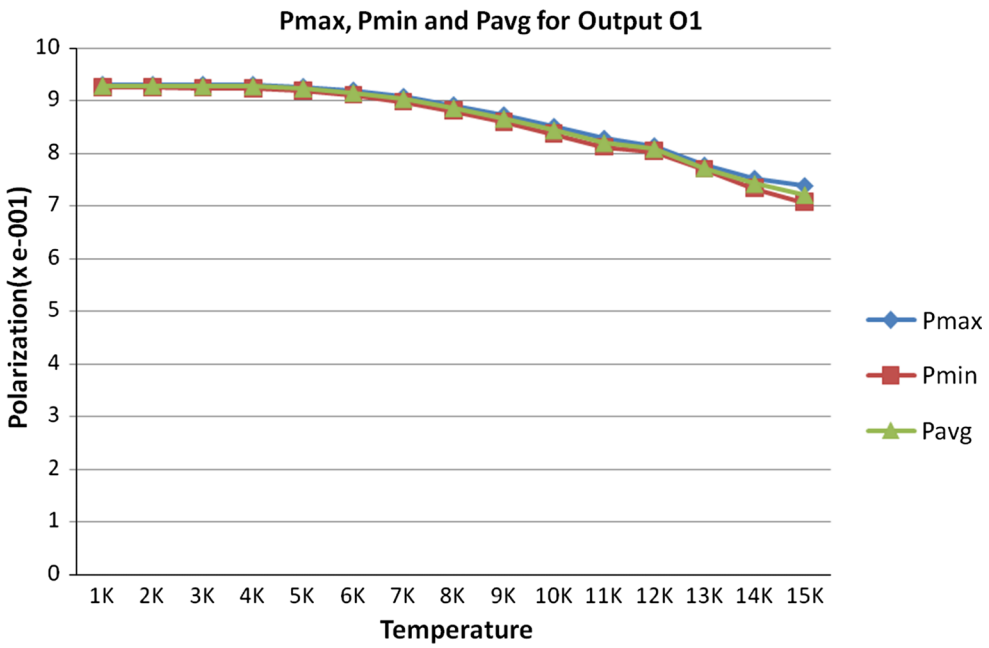


Fig. 13 Effect of temperature on output polarization of proposed QCA D flip-flop

Fig. 14 Changes in polarization for output cell O_1 of proposed QCA shift register



that the P_{avg} for proposed QCA D flip-flop is higher at every level of temperatures compare to the designs proposed by Mustafa and Beigh (2014), Ahmad et al. (2014), Goswami et al. (2014), Hashemi and Navi (2012), Lim et al. (2012) and Xiao and Ying (2012). After temperature of 7 K, the P_{avg} for output cell of existing D flip-flop is dropped drastically, but for proposed D flip-flop P_{avg} has little changes which is still enough to get correct outputs compare to others. Similarly, it can be seen from Fig. 19 that the P_{avg} for proposed QCA SISO shift register has higher value at every level of temperatures compare to the designs proposed by Mustafa and Beigh (2014) and Ahmad et al. (2014).

Thus, all the proposed designs are more stable under thermal randomness than the existing designs.

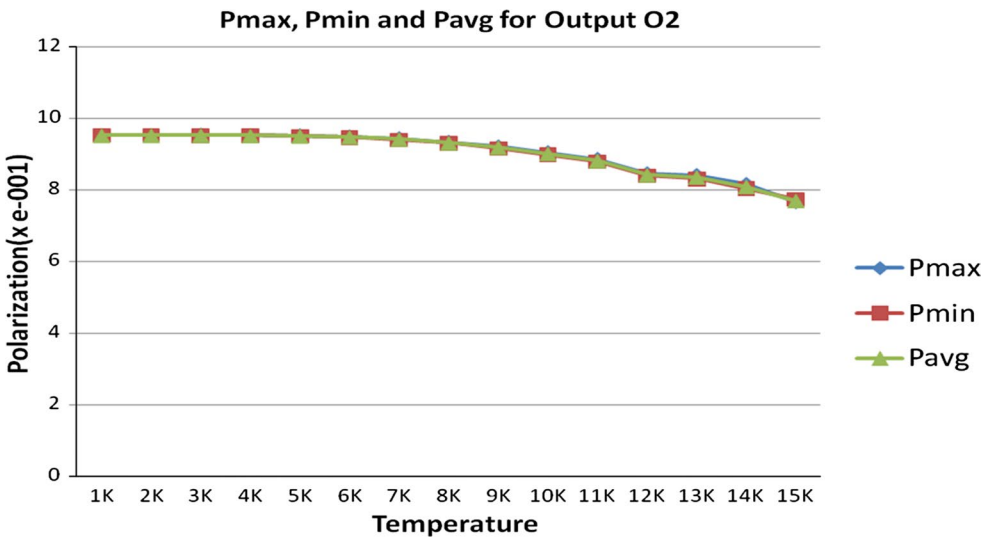


Fig. 15 Changes in polarization for output cell O_2 of proposed QCA shift register

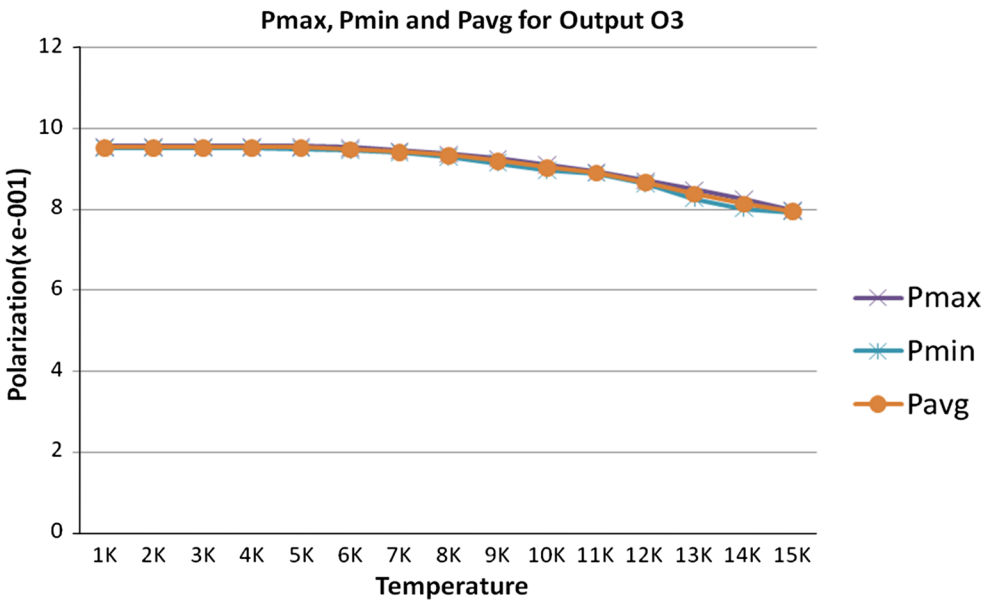


Fig. 16 Changes in polarization for output cell O_3 of proposed QCA shift register

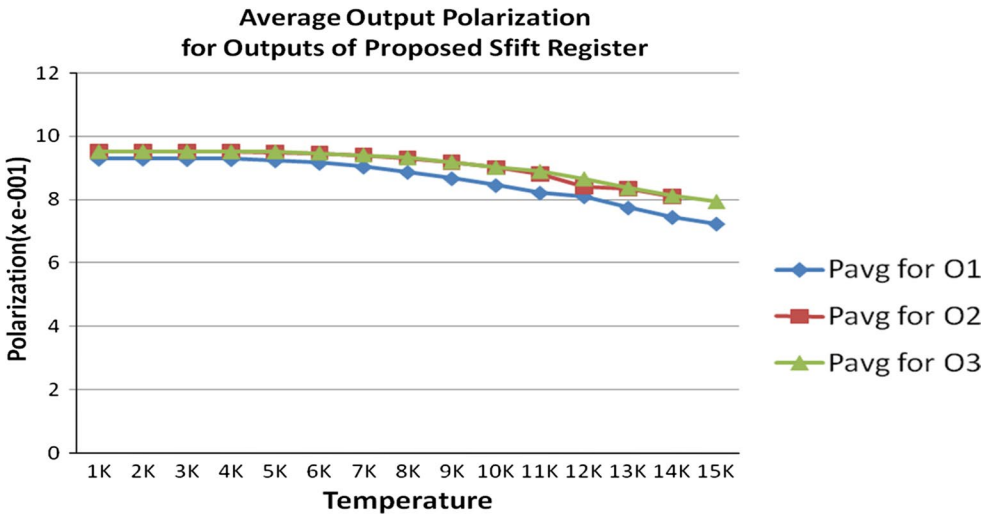


Fig. 17 Changes in average output polarization for output cell O_1, O_2, and O_3 of proposed QCA shift register

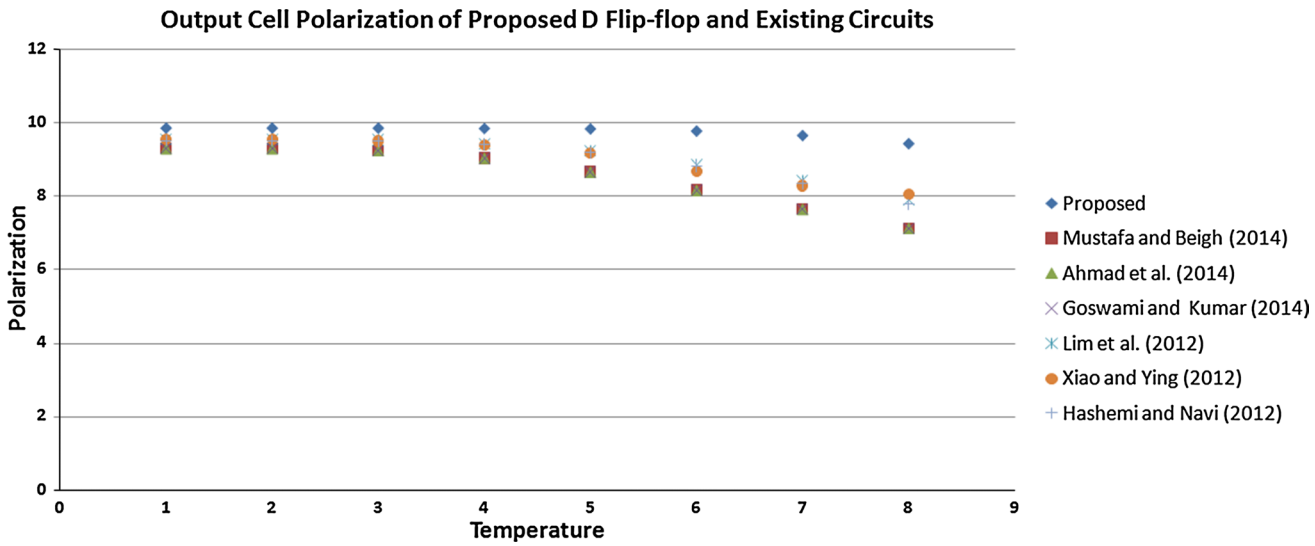


Fig. 18 P_{avg} of proposed QCA D flip-flop and existing layouts

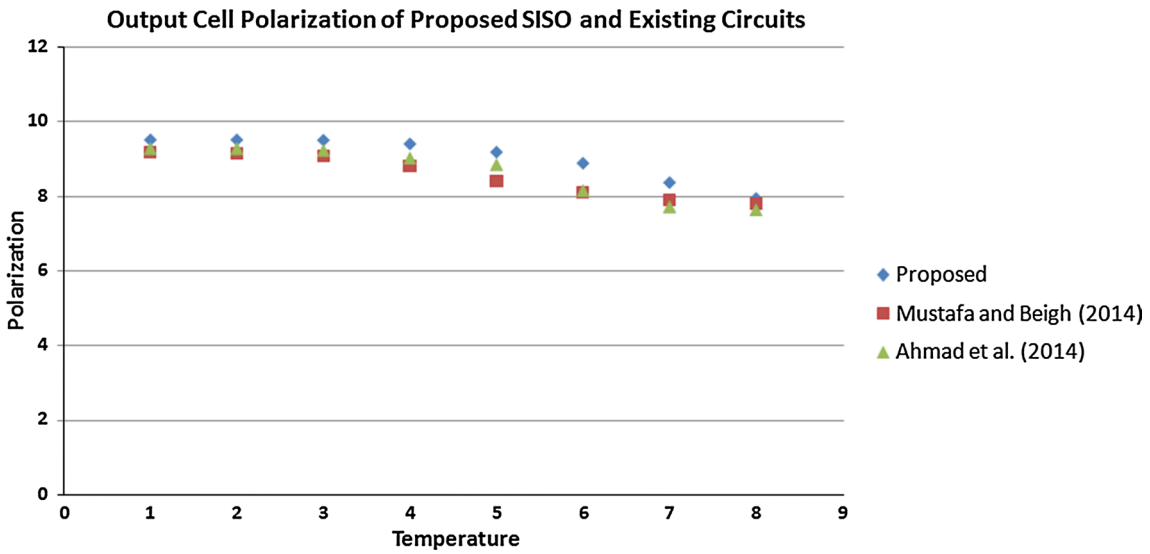


Fig. 19 P_{avg} of proposed QCA SISO shift register and existing layouts

5 Conclusion

This paper outlines an optimized QCA based design of shift register using a new QCA layout of D flip-flop. The designs are achieved in a single layer which provides the simplicity of the circuits. The proposed QCA layouts have less cell count and high device density than existing ones. The dissipated energy by the layouts describes that energy dissipation by all the designs are low. The simulation results establish the accuracy of the layouts when compared to the truth table. The exploration of temperature effect on polarization of each output cell of proposed QCA layouts shows the stability of the circuit. The impact of control input i.e., clock on the designs are explored which describes how the outputs are affected by the clock signal. Besides the defects in proposed QCA layouts are also observed and excelled to obtain error free implementation of the designs. All the designs can be utilized to achieve an advance building block for QCA based counters; linear feedback shift registers at nanoscale level.

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