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Low-power half-select free single-ended 10 transistor SRAM cell

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Abstract This paper proposes a novel subthreshold 10T SRAM cell. The proposed design removes the half-select issue which is a problem in SRAM array as observed in the case of conventional 6T and 8T cells. Since the proposed cell is free from half-select disturb, bit-interleaving scheme can be implemented. A bit-interleaved architecture helps to reduce errors in multiple bits of a single word. This makes the proposed design immune to soft error caused by α particles or high-energy cosmic rays. The proposed cell uses data-dependent stack PMOS switching scheme (DSPS) to reduce the write access time and improve the write-ability. A single-ended read decoupled scheme used to perform read operation enhances the read stability. Various design metrics of the proposed SRAM cell have been compared with previously proposed cells such as SBI9T, DF9T and UDVS10T. The proposed cell shows 1.07×, 2.89× and 13.78× improvement in write access time while writing '0' as compared to the SBI9T, DF9T and UDVS10T, respectively at a V_{DD} of 0.4 V. The proposed cell shows lesser spread in write delay as compared to DF9T cell, which signifies lower variability. There is 8.4, 10.3 and 6.5 % improvement in WSNM when compared to the three cells mentioned above, respectively. Also, 27.3 and 2.02 % improvements can be observed in RSNM when compared to the SBI9T and DF9T at a supply voltage of 0.4 V. RSNM of UDVS10T is same as that of the proposed design. As far as power consumption is concerned, the proposed design consumes 1.38× lesser read power as compared to UDVS10T and 1.67× and 5.02× lesser write power as compared to DF9T and UDVS10T respectively. The proposed design shows 1.8 % improvement in read current variability when compared to DF9T. Lastly, the proposed cell shows 2.21× and 5.25× higher I_{READ}/I_{LEAK} as compared to DF9T and UDVS10T.

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1 Introduction

More than 70 % of the SoC area is occupied by SRAM. As a large number of modern day processors use SRAM cells, the speed of their operation has a significant dependence on the speed of SRAM. Besides speed, power consumption, leakage current and area of SRAM play an important role for the processors. Power consumption is a very important aspect of VLSI circuits and an effective way to reduce it is to scale down the supply voltage. This is because of the quadratic relationship between the power consumption and supply voltage (Rabaey et al. 2003). Lowering the supply voltage to a value lesser than the normal threshold voltage ensures the operation of the circuit in subthreshold region. Figure 2 shows a plot of total energy versus V_{DD} for the circuit under test (CUT) of an FO4 inverter (Fig. 1). A minimum energy point is reached in the subthreshold region. Thus, it is desirable to operate the cell in the near-threshold/subthreshold region. But, several challenges are faced in subthreshold operation. These involve significantly degraded I_{ON}/I_{OFF} ratio and large process, voltage, temperature (PVT) variations. Subthreshold circuits suffer from threshold voltage (V_t) variation due to random dopant fluctuation (RDF) more acutely as I_{SUB} (drain-to-source subthreshold current) is exponentially dependent on V_t in subthreshold region (Pasandi and Fakhraie 2014).

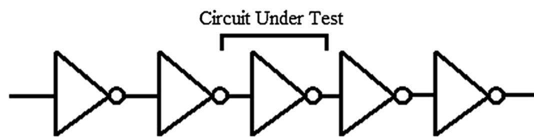


Fig. 1 FO4 inverter

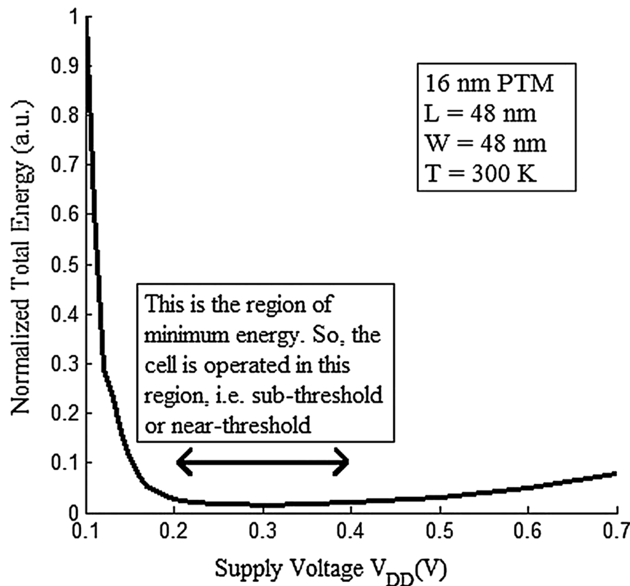


Fig. 2 Normalized total energy versus V_{DD} for the CUT in an FO4 inverter

The conventional 6T SRAM cell used in microprocessors (Sun et al. 2015) has a simple structure and possesses large storage capability but also suffers from half-select disturb and contradicting read/write requirements (Azam et al. 2010). Moreover, the stability of 6T SRAM gets degraded with down-scaling of supply voltage. Various other SRAM cells with read/write-assist schemes have been proposed. The 8T cell proposed by Chang et al. (2008) uses a decoupled scheme to perform read operation, in which, the read current does not flow through the storage node. This eliminates read-disturb but the 6T like write operation of this cell leads to dummy read operation during write in the half-selected cells on the selected word-line. Researchers have also used transmission gates instead of N-MOSFETs for the access transistors to mitigate the impact of PVT variations at the cost of read delay and write trip current (Islam and Hasan 2012b). Chang et al. proposed a D2AP 8T cell (Chang et al. 2012a) which possesses improved write-ability but faces read disturb. Joshi et al. (2011) proposed a column-decoupled (CDC) 8T cell in which a column select signal was used with an extra inverter to mitigate the half-select issue. But the cell suffers from read-disturb. In Chang et al. (2011), a 9T cell was proposed. The write margin was improved by using feedback-cutoff NMOS transistors and read-disturb was reduced by incorporating a dynamic read decoupled scheme. In Kulkarni and Roy (2012), a Schmitt-triggered (ST) based cell was proposed. This cell uses half Schmitt trigger in its pull down path. Due to this, the trip voltage of the cross-coupled inverters is raised, which reduces read failure. But the area overhead is a matter of concern. Various other cells have been put forth by researchers where peripheral assist circuits have been proposed to improve the read-stability and write-ability. But, peripheral circuits are generally vulnerable to global and local variations.

In this article, we propose a novel 10T SRAM cell which makes use of the data-dependent stack PMOS switching (DSPS) write assist scheme to improve the write-ability and write delay. The proposed design decouples the read current path from the storage node which significantly improves the read-stability. An important highlight of the 10T cell is that it is half-select disturb free. Section 2 gives an explanation of the soft-error and half-select issue in SRAM cells. In Sect. 3, the proposed circuit and transistor sizing have been discussed. The read/write operations and simulation results have been mentioned in Sect. 4. Section 5 concludes the paper.

2 Soft error and the half-select issue

SRAM cells suffer from soft-error problem (also called single-event upset). This error implies that the stored datum is incorrect. Positively charged alpha particles radiated from packaging materials that contain small amounts of radioactive contaminants transports through semiconductor resulting in impact ionization and modulating distribution of electrons of the storage nodes. Its impact is significantly felt in subthreshold region because of the critical charge in the storage node being less. According to Hazucha et al. (2003), for every 10 % decrement in supply voltage, the soft-error rate increases by 18 %. Soft error may also occur when energetic cosmic rays strike the storage node and changes the data state without affecting the circuit. Figure 3 shows three situations of soft error that may take place. In the first case, a single bit is affected due to particle strike. This can be corrected by Hamming single error correction/double error detection (SECDED) codes (Hamming 1950). In the next case, more than 1 bit is affected in a single word and finally, there is also a situation wherein, a single bit is affected for multiple words. In the second case (Fig. 3b) all the bits of a single word are located adjacent to each other. When a particle strikes, multiple bits of the same word are upset. This cannot be fixed by the use of SECDED codes. Complex mechanisms are used to reduce the abovementioned problem. One such method is to interleave the bits

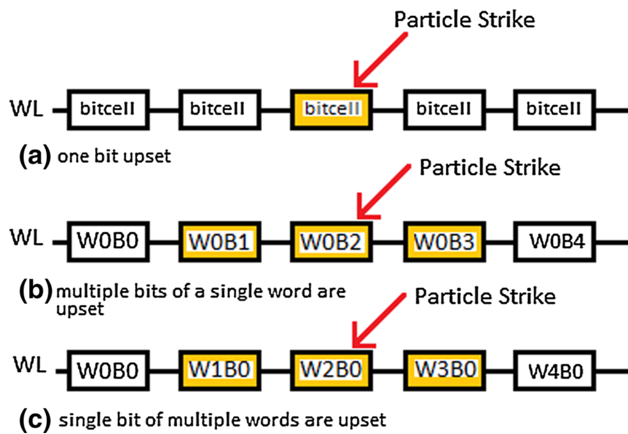


Fig. 3 Different scenarios in soft error

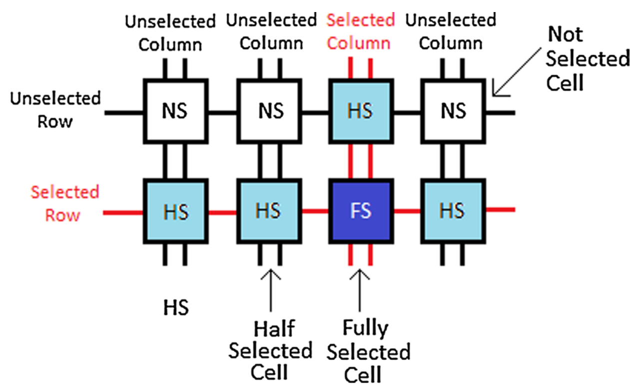
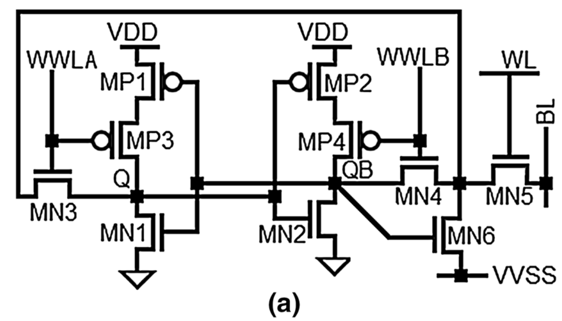


Fig. 4 Half-select problem in bit-interleaved architecture



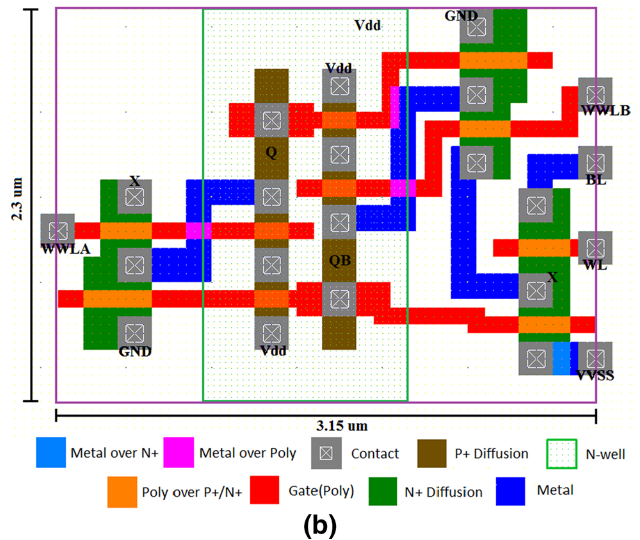


Fig. 5 **a** Schematic of proposed DSPS10T SRAM cell. **b** Layout of the proposed DSPS10T SRAM cell

of a word (Khayatzadeh and Lian 2014), which implies the logically adjacent bits of a single word will not be kept actually adjacent. Such a situation is depicted in Fig. 3c where a single bit of different words are placed adjacent to each other. This is a bit-interleaved arrangement and SECDED codes can now be used as a single bit of different words have been affected.

Thus, bit-interleaving seems to be an effective way to combat the problem of particle-strike induced upsets of multiple bits in a single word. But interleaving of bits raises another problem—the half-select disturb. This issue is depicted in Fig. 4. The cross-point of the selected column and the selected row is the fully selected cell. But there are also half-selected cells present like those cells which are present in the selected column and in the unselected row. In case of such cells, the contents of the storage node may flip leading to undesired write operation. Researchers have proposed several circuits to overcome the half-select disturb. Sinangil et al. (2009) proposed a column-interleaved 8T cell which decouples the large bitline capacitance from the half-selected cells. Chang et al. (2009) proposed a differential 10T subthreshold SRAM which makes use of bit-interleaving scheme by using vertical and horizontal word-lines. Do et al. (2011) used the idea of different cell voltages for basic modes which provided separate read and write operations. Thus, a bit-interleaving scheme was implemented.

3 Proposed design and circuit description

Figure 5a, b show the schematic and thin cell layout of the proposed 10T SRAM cell, respectively. The transistors MP1, MP2, MN1 and MN2 constitute the cross-coupled inverter latches. The transistors MN5 and MN6 are used for enhancing the read stability as the path of the read current is decoupled from the storage node. The proposed design, thus, has a single-ended read operation. An important feature of the proposed design is the DSPS write assist scheme. Since two different schemes are used to improve the read stability and write-ability, the issue of sizing conflict for read and write operations as faced in case of the conventional 6T SRAM cell is no more encountered. The

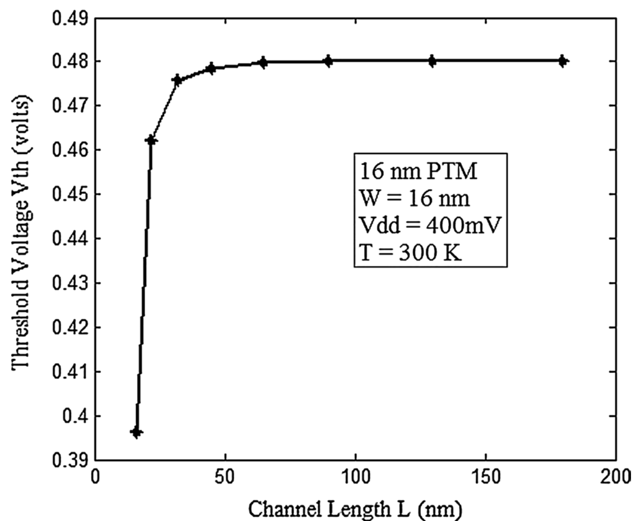


Fig. 6 Threshold voltage versus channel length of an N-MOSFET

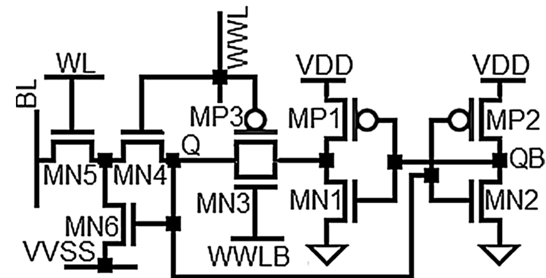


Fig. 7 Subthreshold bit-interleaving 9T SRAM cell (SBI9T) (Chang et al. 2012b)

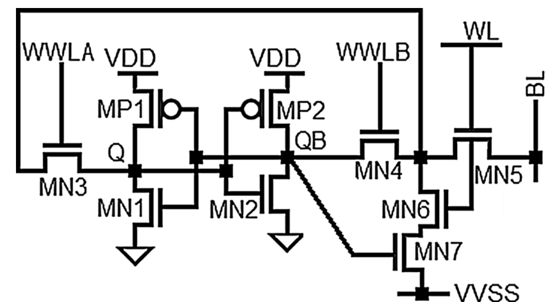


Fig. 8 Disturb free 9T SRAM cell (DF9T) (Tu et al. 2012)

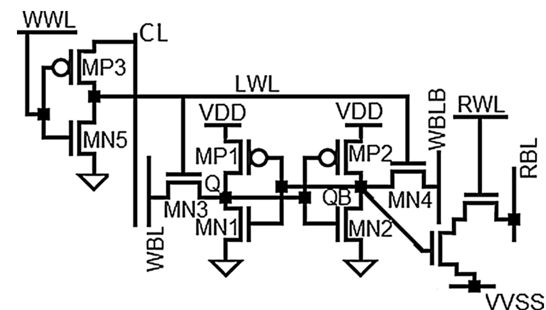


Fig. 9 UDVS10T SRAM cell (UDVS10T) (Chen et al. 2012)

transistors MN3 and MN4 are the access transistors and two PMOS transistors MP3 and MP4 are used as stack transistors. The PMOS stack transistors are used to implement the DSPS write assist scheme which is explained in detail later in this section. The word-line (WL) is row-based and the write word-line A (WWLA) and write word-line B (WWLB) are column based. The virtual VSS (VVSS) is row-based and is used to reduce the effect of leakage current from BL during the hold mode and for the half-selected cells during read/write by keeping it precharged. The proposed design utilizes a single bit-line (BL) which is column-based.

As the CMOS technology is scaling down, process variations are becoming prominent. This work is based on the 16-nm Predictive Technology Model (PTM), in which variation of threshold voltage is a matter of concern. Figure 6 shows the variation of threshold voltage of a single N-MOSFET with gate length. It can be observed that at a gate length of 48 nm (which is three times longer than the minimum length permitted in 16-nm technology node), the threshold voltage variation lessens and beyond 48 nm, the variation is no more prominent. So, at the 16-nm technology node, we have selected the gate length of all the transistors to be 48 nm. Transistors MP1 and MP2 have a width over length (W/L) ratio of 1. The NMOS transistors MN1 and MN2 have a W/L ratio of 2. The W/L ratio of the access transistors MN3 and MN4 is 1.5. The stack transistors (MP3 and MP4) and the transistors used for read buffer (MN5 and MN6) have a W/L ratio of 1 and 1.5 respectively. The transistor sizing for the other circuits (Figs. 7, 8 and 9) which have been used for comparison of design metrics have been chosen in such a way that the area is comparable to that of the proposed design.

As can be seen in Fig. 2, the voltage at which minimum energy is obtained for the case of CUT in FO4 inverter (Fig. 1) is 0.3 V. So, for minimum energy, the circuit has to be operated deep in the subthreshold region. Doing this leads to significant penalty in performance. It has been shown that a 20 % increase in energy from the minimum energy improves the performance by ten times. Moreover, the optimum energy delay curve flattens near the minimum energy point. So, by increasing the voltage to a little extent and by sacrificing small increment in energy, substantial improvement in performance can be observed (Markovic et al. 2010). Due to this, the point of operation now shifts from sub-threshold to near-threshold region. Thus, the voltage of operation in this paper has been taken as 0.4 V, whereas the minimum energy point as in case of an FO4 inverter was obtained at 0.3 V.

Table 1 Operation condition of the proposed DSPS10T SRAM cell

	Hold	Read	Write '0'	Write '1'
WL	GND	V_{DD}	V_{DD}	V_{DD}
VVSS	V_{DD}	GND	GND	GND
WWLA	GND	GND	V_{DD}	GND
WWLB	GND	GND	GND	V_{DD}
BL	V_{DD}	V_{DD}	GND	GND

3.1 Hold operation and read operation with read buffer

During the hold mode, WL, WWLA and WWLB are kept grounded. BL is precharged. VVSS is also kept precharged to reduce leakage of BL (see Table 1). The transistors MN5 and MN6 are used to perform the read operation. During read, the selected bitline, BL, is kept precharged. The selected WL is enabled. WWLA and WWLB are kept disabled. VVSS is forced to ground. If the node 'QB' stores'1', the transistor MN6 is switched on and BL discharges through the path formed by the transistors MN5 and MN6. Since the read current does not encounter storage nodes in its path, the read static noise margin (RSNM) of the proposed cell is improved and is as large as the hold mode SNM. A successful read operation occurs if the voltage of BL reduces to 50 % of the precharged value (Chang et al. 2009).

In the proposed cell, undesired read operation does not occur in the half-selected cells. To elaborate this point, consider a situation in which, '1' is stored at node QB of a cell in a different row but in the same column as that of the selected cell (i.e., a column half-selected cell). For such cells, read operation does not occur because WL is at ground and VVSS is precharged. Thus, the precharged BL does not find a path to discharge.

3.2 DSPS write assist

For the write operation, WL is raised to V_{DD}, BL and VVSS are forced to ground. The proposed cell utilizes the DSPS write-assist technique. According to the data to be written on the storage node, one of the write word lines, either WWLA or WWLB, is loaded with V_{DD} and the other one is grounded. Depending on the voltage of WWLA and WWLB, either of the stacked transistors MP3 or MP4 is switched off. This causes the corresponding cell storage node to cut-off from V_{DD}. If the PMOSFETs MP3/MP4 would not have been there, the node storing '1' would have had V_{DD} through MP1/MP2. Due to the presence of MP3/MP4, access transistors MN3/5 and MN4/5 need not to fight against pull-up transistors MP1/2 and win the fight during write operation. This helps in improving the write-ability of the proposed design. Suppose the node Q stores '1' and QB stores '0'. We wish to write '0' on the node Q. Depending on this choice of writing a '0' on Q, WWLA is raised to V_{DD} and WWLB is at ground. As a result, node Q is cutoff from V_{DD} as MP3 is switched off. Thus, the node Q storing '1' discharges through MN3/5 by BL and the node QB is pulled up by MP2/4. In the other case when QB is storing '1' and Q is storing '0' and we wish to write '1' to Q, WWLA is grounded and WWLB is raised to V_{DD}. Due to this, the stack transistor MP4 is switched off and thus, QB is cutoff from V_{DD}. Node QB discharges through MN4/5 by BL and Q is pulled up by MP1/3.

The proposed design is immune to unwanted write operation in the half-selected cells. Suppose a cell is present in the active column but present in an unselected row. In this column half-selected cell, suppose QB (Q) is storing '1' ('0') and WWLB (WWLA) is raised to V_{DD} (grounded). QB will not find a discharge path to BL (which is kept grounded) as WL is not charged for an unselected row and VVSS is also precharged. MN5 being off disconnects the node QB from the bitline. In case of a cell which is present in the active row but in an unselected column, WL is raised to V_{DD}. WWLA, WWLB, VVSS and BL are kept at ground. Thus, the '1' stored at either Q or QB will not find a discharge path to BL and write operation does not occur. Figure 10 shows four different scenarios. Figure 10a, b show the state of the cell during write '1' and write '0' operation in a fully selected cell. On the other hand, Fig. 10c, d show the state of the cell in case of the half-selected cells (cell in selected column and unselected row).

4 Simulation results and discussion

In this section, various design metrics are estimated using Monte Carlo simulations. The simulations for the proposed design as well as the previously proposed circuits have been done using the 16-nm PTM (http://ptm.asu.edu/). Further, in order to prove the effectiveness of the proposed design, corresponding simulations have also been performed using TSMC's 180 nm foundry file). It is assumed that the channel length (L), gate oxide thickness (t_{OX}) and the doping concentration in the channel region (NDEP) have independent Gaussian distributions with a 3 sigma variation of 10 % (Vaddi et al. 2010). With reference to ITRS 2009, 10 % fluctuation in V_{DD} is expected in further scaled technology node. This is why, the estimation of the design metrics have been done by altering the supply voltage from 0.2 to 0.4 V. As mentioned in (Carlson 2008), a sample size of 2000 leads to less than 4 % inaccuracy in standard deviation evaluation. To ensure even higher accuracy, a sample size of 5000 has been taken.

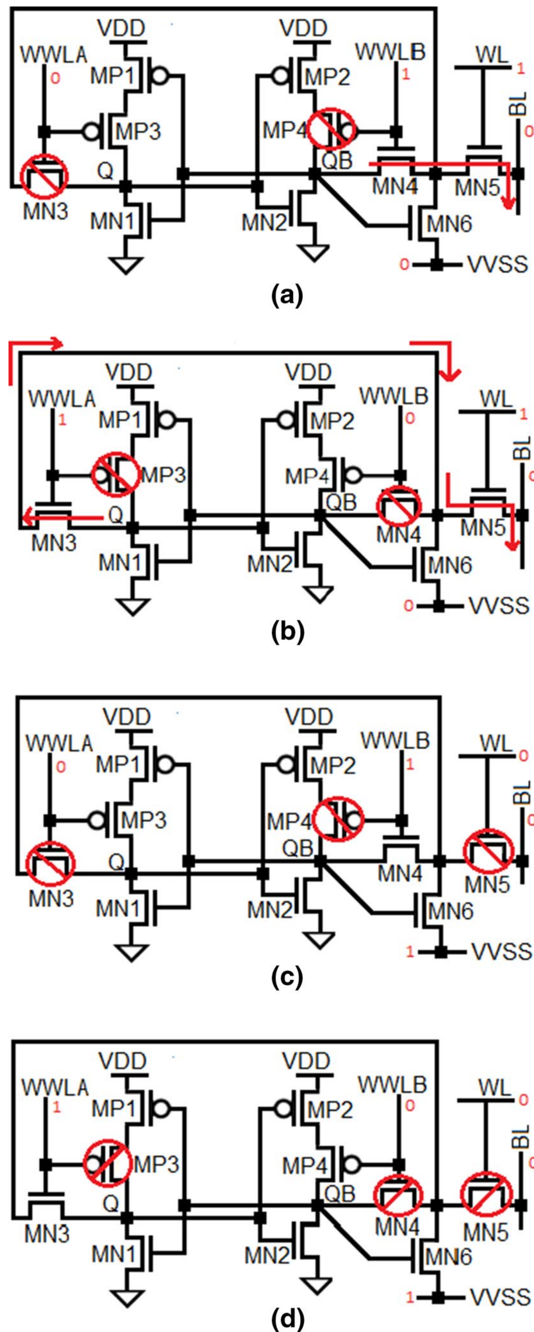


Fig. 10 **a** Selected cell under write ‘1’ operation. **b** Selected cell under write ‘0’ operation. **c** Column half-selected cell under write ‘1’. **d** Column half-selected cell under write ‘0’ operation

Table 2 T_{WA} during write ‘1’ on node Q

V_{DD} (V)	DSPS10T (s)	SBI9T (s)	DF9T (s)	UDVS10T (s)
0.20	1.35E−07	9.60E−07	2.99E−07	2.55E−06
0.25	4.85E−08	6.55E−07	1.17E−07	9.47E−07
0.30	1.77E−08	4.47E−07	4.74E−08	3.36E−07
0.35	6.91E−09	3.13E−07	2.07E−08	1.19E−07
0.40	3.16E−09	2.29E−07	9.74E−09	4.35E−08

Table 3 T_{WA} during write ‘0’ on node Q

V_{DD} (V)	DAPC10T (s)	SBI9T (s)	DF9T (s)	UDVS10T (s)
0.20	1.31E−07	2.00E−07	3.00E−07	2.54E−06
0.25	4.74E−08	6.92E−08	1.16E−07	9.45E−07
0.30	1.73E−08	2.43E−08	4.61E−08	3.35E−07
0.35	6.89E−09	8.82E−09	2.00E−08	1.19E−07
0.40	3.15E−09	3.38E−09	9.10E−09	4.34E−08

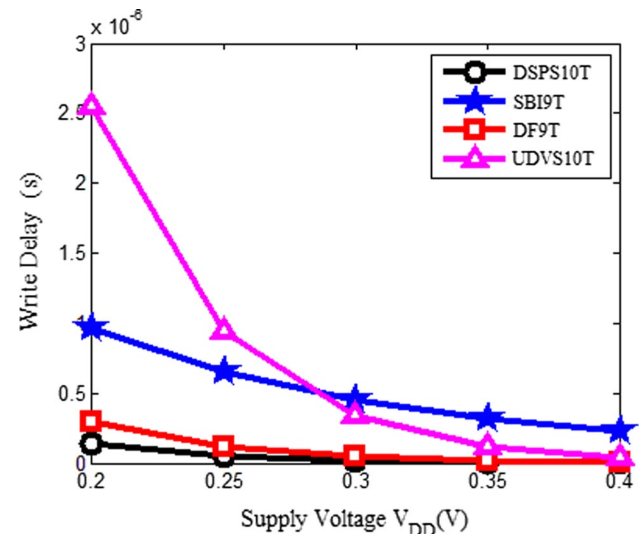


Fig. 11 Write access time versus supply voltage (write ‘1’)

4.1 Write access time

The estimation of write delay or write access time (T_{WA}) is done as the time required to write ‘0’ to storage node Q (previously storing ‘1’). This is essentially, the time when WL is asserted to the time when Q falls to 10 % of its initial high value (Islam and Hasan 2012a). This is the write ‘0’ condition. For writing a ‘1’ to node Q, or in other words, writing a ‘0’ to node QB, the write delay is estimated as the time from when WL is asserted to the time at which QB falls to 10 % of its precharged value. The MP1/MP3 then pulls up the voltage at node Q and thus, a ‘1’ is written. This is the write ‘1’ condition. Thus, for a successful write operation, a 90 % voltage swing has been enforced. As can be seen in Tables 2 and 3, at a V_{DD} of 0.4 V, the proposed cell shows improvements in write delay (write ‘1’ and write ‘0’) as compared to SBI9T, DF9T and UDVS10T, respectively.

During write operation in the proposed design, the stack PMOS transistor corresponding to the node storing ‘1’ is switched off, as per the DSPS write assist scheme. This causes the node to remain cutoff from V_{DD}. Hence, it is easier to pull down this node, and improvement in write delay is observed as compared to other circuits. Figures 11

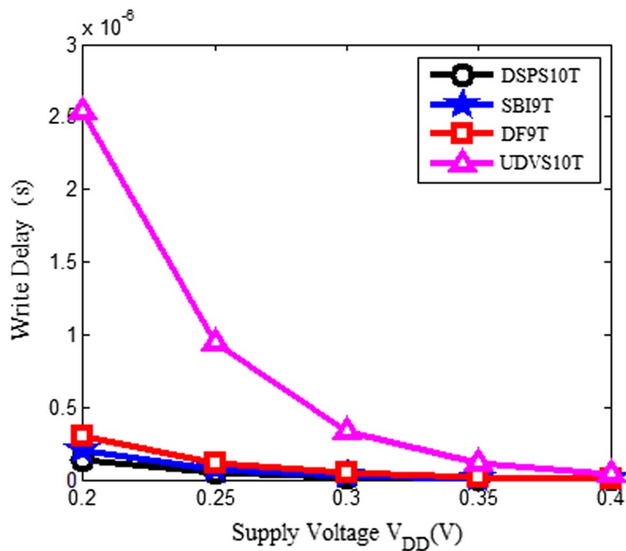


Fig. 12 Write access time versus supply voltage (write '0')

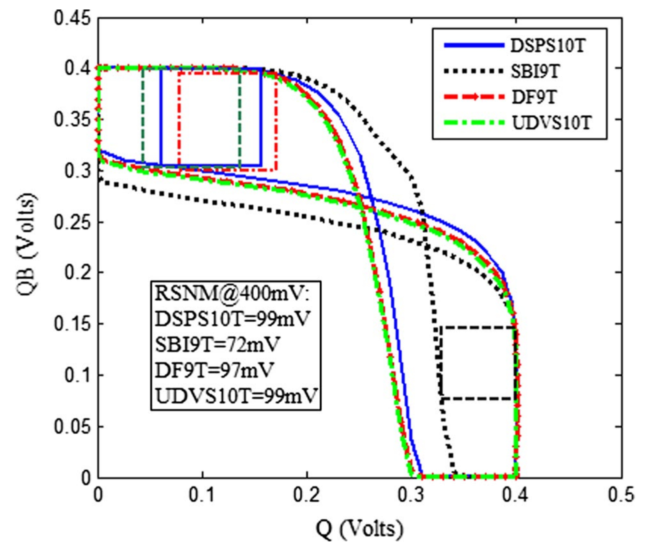


Fig. 14 Static voltage characteristic of SRAM cell during read operation

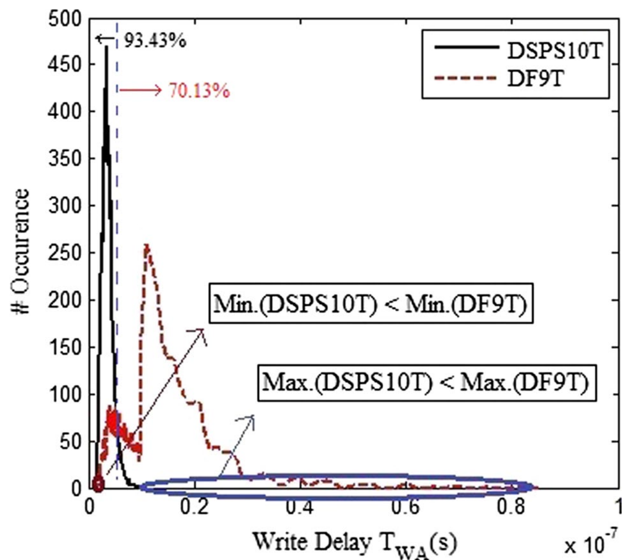


Fig. 13 Write delay distribution of DSPS10T and DF9T

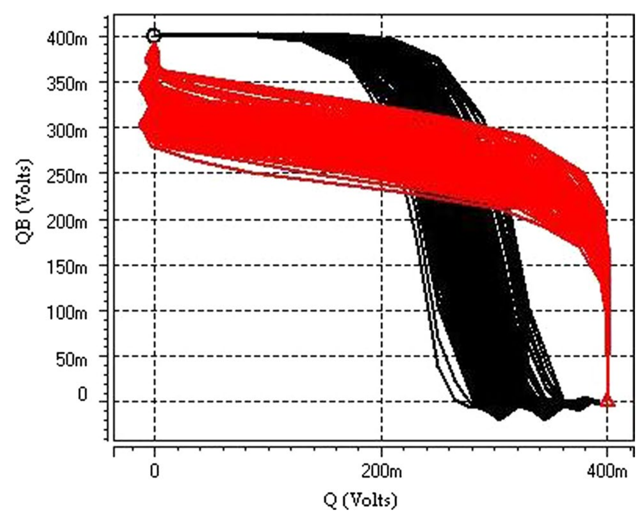


Fig. 15 Static voltage characteristics during read operation obtained from statistical method such as large number of Monte Carlo Simulations for proposed DSPS10T SRAM cell

and 12 show the plot of write delay versus V_{DD} for the DSPS10T, SBI9T, DF9T and UDVS10T for write '1' and write '0' cases respectively.

Write delay distribution is plotted in Fig. 13. The write delay of the proposed DSPS10T exhibits narrower spread as compared to DF9T. As is evident from Fig. 13, the long tail of write delay distribution plot in case of DF9T extends to the right beyond that of DSPS10T. This signifies that the spread of write delay is narrower as compared to DF9T. This verifies the robustness of the proposed cell in terms of write delay. Both the distribution plots intersect at 5.37 ns. Our simulation data bring out an important fact. 93.43 % of the statistical samples of DSPS10T are found to exhibit shorter write delay than 5.37 ns, whereas 70.13 % of the statistical samples of DF9T are found to show write delay longer than 5.37 ns. This implies that the proposed DSPS10T cells require shorter time to accomplish write operation as compared to DF9T cells. This is also evident from Figs. 11 and 12.

4.2 Read stability

The measure of read stability is the read static noise margin (RSNM). The estimation of RSNM is done graphically.

RSNM is evaluated as the side of the largest square that fits into the smaller lobe of the butterfly curve (Islam and Hasan 2012a). Figure 14 shows the butterfly curves for RSNM of DSPS10T, SBI9T, DF9T and UDVS10T. As can be observed, the proposed cell shows an RSNM of 99 mV. The reason for high RSNM is the employment of a technique in which the storage nodes are isolated from BL. SBI9T and UDVS10T also employ the concept of decoupled read scheme, and so, RSNM for these circuits are comparable to that of the proposed DSPS10T. As mentioned in Tu et al. (2012), an SRAM cell is considered to possess excellent read stability if its RSNM is about 25 % of V_{DD}. The proposed design very nearly meets this criterion. Thus, the proposed circuit has high read stability. Figure 15 shows static voltage characteristics during read operation obtained from statistical method such as large number of Monte Carlo simulations of DSPS10T cell.

4.3 Write-ability

Write static noise margin (WSNM) is a measure of the write-ability of a cell. The write-ability can be stated as the ability of a cell to pull down the voltage at node storing '1' to a value lesser than the switching threshold voltage of the other inverter, which is storing a '0' at its storage node. This will cause the cell storage nodes to flip states. WSNM is estimated by using the read and write VTCs. For the case in which,'1' is being written to node Q or '0' to QB, the write VTC is obtained by sweeping V_Q (see Fig. 16, x-axis) with WWLB and WWLA kept high and low, respectively, VVSS and BL kept low and the voltage at node QB is monitored. This write VTC is used in combination with the read VTC. The read VTC is obtained by sweeping V_{QB} (Fig. 16, y-axis) and monitoring V_Q (Fig. 16, x-axis). WSNM is evaluated as the side length of the smallest square that can be inscribed in the lower half of the read and write VTCs (Islam and Hasan 2012a). As can be seen in Fig. 16, the proposed design shows a WSNM of 26.75 mV, the highest as compared to the other SRAM cells. This is because of the DSPS scheme used for write assist in our proposed design. Depending on the data to be written on the storage node, one of the write word lines, either WWLA or WWLB, is loaded with V_{DD} and the other one is grounded by write driver (not shown). Thus, either of the stacked transistors MP3 or MP4 is switched off. If MP3 and MP4 were not present, the storage node would be at V_{DD} through MP1/MP2. The presence of PMOS transistors MP3/MP4 causes the corresponding cell storage node to cut off from V_{DD}. Hence, it becomes easier for MN3/MN5 or MN4/MN5 to pull down node storing 1 and flip the cell content. In other words, presence of MP3/4 improves write delay and hence write-ability. Figure 16 shows a plot of the read and write VTCs of the DSPS10T, SBI9T, DF9T and UDVS10T. It can be observed that the read and write VTCs

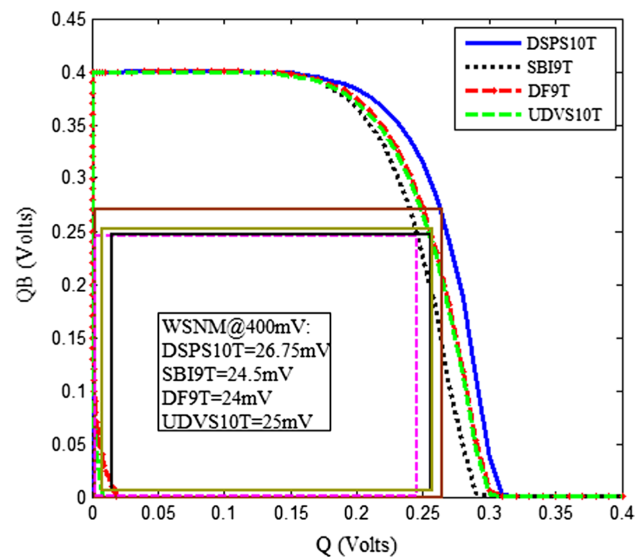


Fig. 16 Static voltage characteristic of SRAM cell during write operation

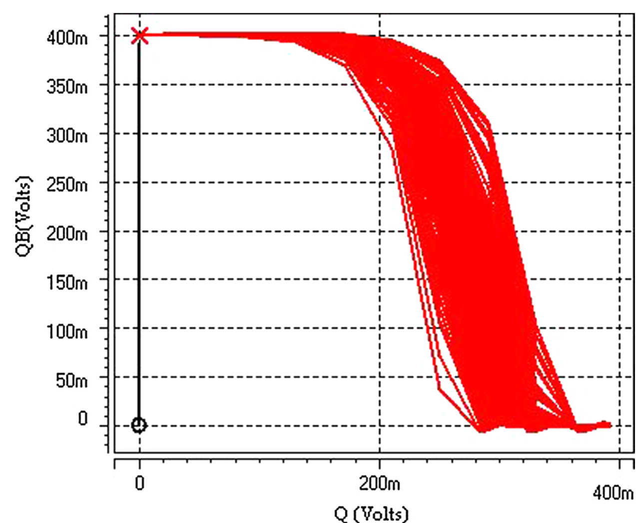


Fig. 17 Static voltage characteristics during write operation obtained from statistical method such as large number of Monte Carlo simulations for proposed DSPS10T SRAM cell

converge to a single point, which means the cross-coupled inverters can function as a mono-stable circuit (Islam et al. 2012). Thus, the write operation is successful. Figure 17 shows static voltage characteristics during write operation obtained from statistical method such as large number of Monte Carlo simulations of DSPS10T cell.

4.4 Read current variability

Read current variability of the proposed DSPS10T is estimated and compared with that of DF9T. Figure 18a, b

show the distribution plots of read current of DSPS10T and DF9T @400 mV. From the figures, it can be observed that the spread of the read current in case of DSPS10T is narrower as compared to DF9T. Read current variance of DSPS10T and DF9T are reported in Table 4. As can be observed from the table, the variance of DSPS10T is 1.8 % lower than that of DF9T. This signifies the robustness of the proposed cell compared to DF9T. Even though the percentage improvement is very low, it is appreciable because variability is a critical issue in nanoscale circuit design.

4.5 Read power

Read power is a measure of the power consumed by the SRAM cell under read conditions. The read power of the DSPS10T is compared with the read power of UDVS10T at 400 mV. It is observed that the proposed DSPS10T cell consumes 1.38 × lower read power as compared to UDVS10T. Table 5 shows the comparative results in terms of power consumption between DSPS10T and UDVS10T at various supply voltages. Figure 19 shows a plot of read power versus supply voltage for both DSPS10T and UDVS10T.

4.6 Write power

Write power is defined as the power consumption during write operation of the SRAM cell. The write power consumption of the DSPS10T is compared with those of DF9T and UDVS10T at various supply voltages. The proposed cell achieves 1.67×/5.02× improvement in write power compared with DF9T/UDVS10T at $V_{DD} = 400$ mV. Table 6 shows the values of write power versus supply voltage for DSPS10T, DF9T and UDVS10T. Schematic illustration of the same is shown in Fig. 20 for easier visual inspection.

4.7 Read current to leakage current ratio

As leakage current through the bit-lines increases, the sense margin of the SRAM cell decreases. This leads to lesser number of SRAM cells which can be placed in a column, thereby reducing the density. In order to attain higher density, it is desired that the SRAM cell possesses high I_{READ} to I_{LEAK} ratio.

The proposed DSPS10T possesses higher I_{READ}/I_{LEAK} as compared to DF9T and UDVS10T. The proposed cell shows higher read current and lower leakage current. This is why the ratio turns out to be highest among the SRAM cells considered for comparison. Since VVSS is kept precharged during the hold mode, this reduces the leakage from BL. This accounts for a reduced leakage current in the proposed design. Figure 21 shows the graphical representation of I_{READ}/I_{LEAK} plotted against supply voltage. Table 7 shows that at $V_{DD} = 0.4$ V, the improvement in I_{READ}/I_{LEAK} in case of the proposed design (4.2×10^5) is 2.21× and 5.25× as compared to DF9T (1.9×10^5) and UDVS10T (0.8×10^5), respectively.

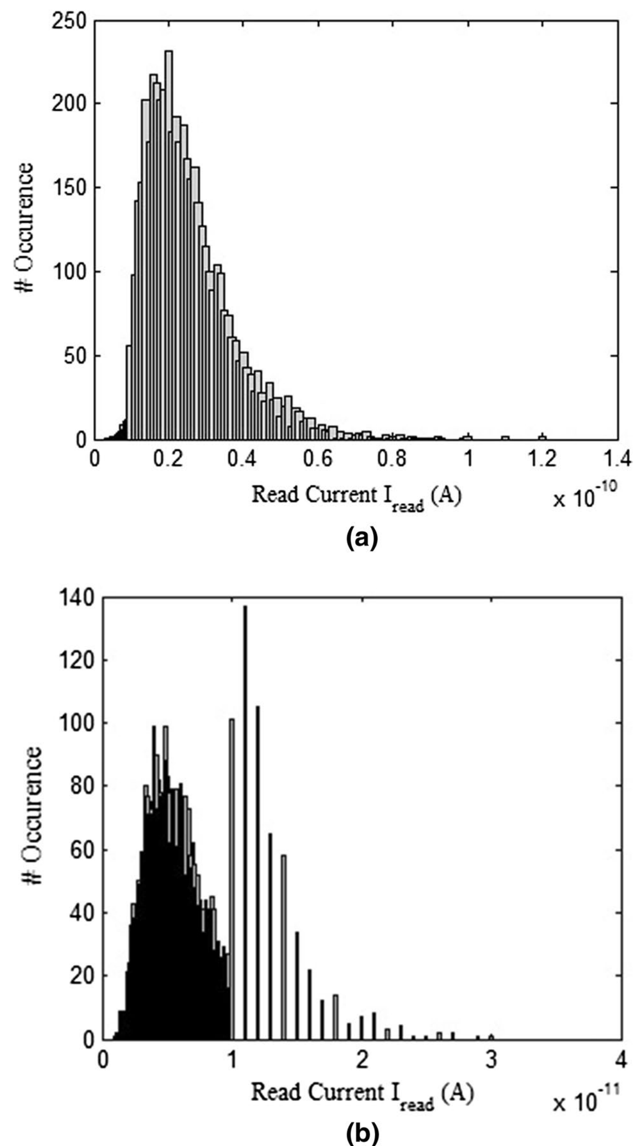


Fig. 18 Read current distribution plot for **a** DSPS10T, **b** DF9T

4.8 Effect of temperature on read power

In this subsection, temperature effect on read power is considered. Temperature is varied from −55 to 100 °C since VLSI circuits often operate at very low as well as elevated temperatures and the cell is operated in the subthreshold region by maintaining $V_{DD} = 0.4$ V ($<V_t$). Theoretically, the power should increase with increase in temperature.

Table 4 Comparison of read current variance of DSPS10T and DF9T @0.40 V

V_{DD} (V)	Variance of DSPS10T	Variance of DF9T	% Improvement
0.40	0.498	0.507	1.8

Table 5 Read power comparison between DSPS10Tand UDVS10T at various supply voltages

V_{DD} (V)	DSPS10T (pW)	UDVS10T (pW)
0.20	06.2	08.1
0.25	09.8	12.3
0.30	14.9	18.2
0.35	21.7	27.0
0.40	30.3	41.9

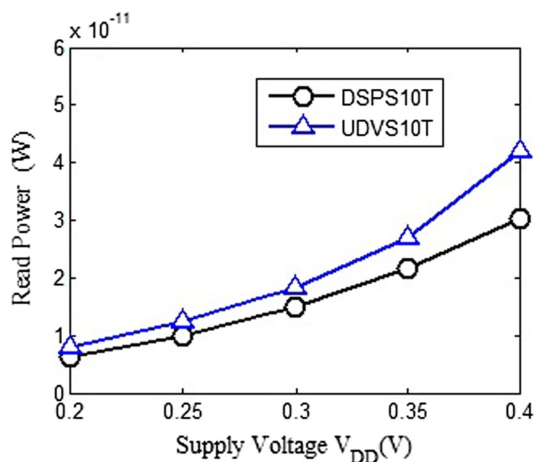


Fig. 19 Read power versus supply voltage for DSPS10T and UDVS10T

Table 6 Write power comparison among DSPS10T, DF9T and UDVS10T at various supply voltages

V_{DD}(V)	DSPS10T (pW)	DF9T (pW)	UDVS10T (pW)
0.20	6.7	9.8	15.7
0.25	11.1	17.5	28.7
0.30	14.8	20.1	49.5
0.35	20.0	44.4	83.9
0.40	28.3	47.3	142.0

Explanation for the same is as follows. Our proposed circuit is operated in subthreshold region. Therefore, subthreshold current (I_{sub}) plays an important role on its power consumption. I_{sub}, controlled by the carrier diffusion, exponentially increases with temperature. This is because V_t (threshold voltage) of a device decreases with increase in temperature, and I_{sub} is exponentially dependent on temperature through V_T (thermal voltage) ($V_T = kT/q = 26$ mV at 300 K).

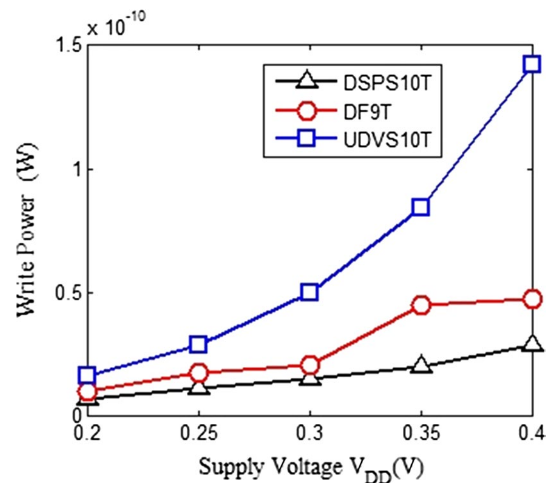


Fig. 20 Write power versus supply voltage for DSPS10T, DF9T and UDVS10T

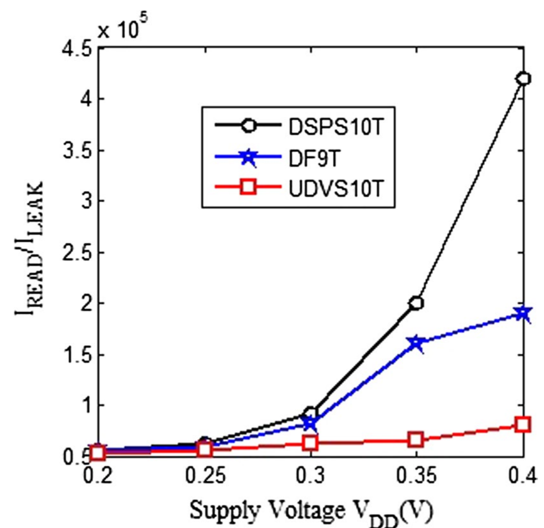


Fig. 21 I_{READ}/I_{LEAK} versus supply voltage for DSPS10T, DF9T and UDVS10T

Table 7 I_{READ}/I_{LEAK} comparison among DSPS10T, DF9T and UDVS10T at various supply voltages

V_{DD} (V)	DSPS10T ($\times 10^5$)	DF9T ($\times 10^5$)	UDVS10T ($\times 10^5$)
0.20	0.56	0.55	0.52
0.25	0.63	0.59	0.56
0.30	0.91	0.82	0.62
0.35	2.00	1.60	0.65
0.40	4.20	1.90	0.80

Table 8 Read power versus temperature for DSPS10T and UDVS10T at $V_{DD} = 0.4$ V

Temp (°C)	DSPS10T (pW)	UDVS10T (pW)
−55	6.8	9.1
0	19.1	25.6
25	30.3	41.9
55	54.3	67.6
100	79.9	92.1

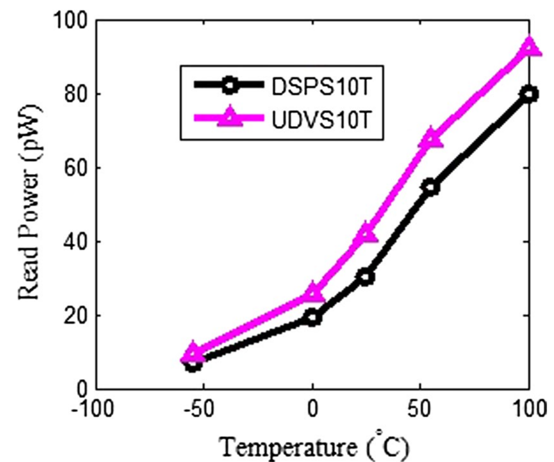


Fig. 22 Read power versus temperature for DSPS10T and UDVS10T at VDD = 0.4 V

We have tabulated read power versus temperature data in Table 8 and the same have been plotted in Fig. 22 for clear and visual inspection. As can be seen from Table 8 and Fig. 22, our simulation results go in line with the theory.

4.9 Validation

In order to validate the proposed design's effectiveness, the results which were obtained using the 16-nm Predictive Technology Model have been verified using the 180-nm Taiwan Semiconductor Manufacturing Company (TSMC) foundry file (Kulkarni et al. 2007; Narsimham 2013). Simulation results using the 180-nm TSMC file show that in the proposed DSPS10T cell, T_{WA} improves by 1.15×/0.124×/5.66× as compared to SBI9T/DF9T/UDVS10T. Read current variability improves by 2.7 % as compared to DF9T. Read power consumption improves by 2.31× as compared to UDVS10T and write power improves by 1.34×/3.83× as compared to DF9T/UDVS10T. Finally, read current variability estimation was done and it was observed that the proposed cell possesses 1.11× lesser variability compared to DF9T.

5 Conclusion

This work proposes a 10T SRAM Cell which is half-select disturb free. The design of this circuit is such that in the half-selected cells, undesired read/write operations do not occur. The proposed design employs a data-dependent stack PMOS switching write assist scheme. Due to this feature, the cell has improvements in write SNM and write delays. The proposed design also shows lesser variability in write delay and read current on comparison with other cells. The proposed design uses a single-ended read-decoupled scheme because of which, the read current does not flow through the storage nodes. This results in enhancement in read SNM. The proposed cell is also suitable for applications involving low power because as discussed, it dissipates lesser power during read and write conditions as compared to other cells. The effect of temperature on read power has also been demonstrated. Finally, the proposed design possesses higher I_{READ}/I_{LEAK}. Thus, the proposed SRAM cell is a good choice as far as fast write operation, overall stability of the circuit and meeting low power requirements are concerned.

References

Azam T, Cheng B, Roy S, Cumming DRS (2010) Robust asymmetric 6T-SRAM cell for low-power operation in nano-CMOS technologies. Electron Lett 46(4):273–274

Carlson AE (2008) Device and circuit techniques for reducing variation in nanoscale SRAM. Ph.D. dissertation, University of California Berkeley, Berkeley, CA

Chang L et al (2008) An 8 T-SRAM for variability tolerance and low voltage operation in high-performance caches. IEEE J Solid-State Circuit 43(4):956–963

Chang IJ, Kim J-J, Park SP, Roy K (2009) A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS. IEEE J Solid-State Circuits 44(2):650–658

Chang M-F, Chang S-W, Chou P-W, Wu W-C (2011) A 130 mV SRAM with expanded write and read margins for subthreshold applications. IEEE J Solid-State Circuits 46(2):520–529

Chang MF et al (2012a) A differential data-aware power-supplied (D2AP) 8 T SRAM cell with expanded write/read stabilities for low VDDmin applications. IEEE J Solid-State Circuit 45(6):1234–1245

Chang MH, Chiu Y-T, Hwang W (2012b) Design and iso-area Vmin analysis of 9T subthreshold SRAM with bit-interleaving scheme in 65-nm CMOS. IEEE Trans Circuits Syst II Exp Briefs 59(7):429–433

Chen J et al (2012) An ultra-dynamic voltage scalable (U-DVS) 10T SRAM with bit-interleaving capability. In: IEEE symposium on circuits and systems, May 2012, pp 1835–1838

Do A-T et al (2011) An 8T differential SRAM with improved noise margin for bit-interleaving in 65 nm CMOS. IEEE Trans Circuits Syst I 58(6):1252–1263

Hamming RW (1950) Error detecting and error correcting codes. Bell Syst Tech J 29:147–160

Hazucha P et al (2003) Neutron soft error rate measurements in 90-nm CMOS process and scaling trends in SRAM from 0.25-µm to 90-nm generation. In: IEDM technical digest, Dec 2003, pp 21.5.1–21.5.4

Islam A, Hasan M (2012a) Leakage characterization of 10T SRAM cell. IEEE Trans Electron Devices 59(3):631–638

Islam A, Hasan M (2012b) A technique to mitigate impact of process, voltage and temperature variations on design metrics of SRAM cell. Microelectron Reliab 52(2):405–411

Islam A, Hasan M, Arslan T (2012) Variation resilient subthreshold SRAM cell design technique. Int J Electron 99(9):1223–1237

Joshi RV et al (2011) A novel column-decoupled 8 T cell for low-power differential and domino-based SRAM design. IEEE Trans Very Large Scale Integr (VLSI) Syst 19(5):869–882

Khayatzadeh M, Lian Yong (2014) Average 8-T differential-sensing subthreshold SRAM with bit interleaving and 1 k bits per bitline. IEEE Trans Very Large Scale Integr (VLSI) Syst 22(5):971–982

Kulkarni JP, Roy K (2012) Ultralow-voltage process-variation-tolerant Schmitt-trigger-based SRAM design. IEEE Trans Very Large Scale Integr (VLSI) Syst 20(2):319–332

Kulkarni JP, Kim K, Roy K (2007) A 160 mV robust Schmitt trigger based subthreshold SRAM. IEEE J Solid-State Circuits 42(10):2303–2313

Markovic D et al (2010) Ultralow-Power design in near-threshold region. In: Proceedings of the IEEE, vol 98(2), pp 237–252. Online. http://ptm.asu.edu/. Accessed 21 Mar 2015

Narsimham S (2013) Hardware Trojan detection by multiple-parameter side-channel analysis. IEEE Trans Comput 62(11):2183–2195

Pasandi G, Fakhraie SM (2014) An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs. IEEE Trans Electron Devices 61(7):2357–2363

Rabaey JM, Chandrakasan AP, Nikolic B (2003) Digital integrated circuits: a design perspective, 2nd edn. Prentice-Hall, New Delhi

Sinangil M. E., Verma N. and Chandrakasan A. P. (2009) A 45 nm 0.5 V 8T column-interleaved SRAM with on-chip reference selection loop for sense-amplifier. In: Proceedigs of the IEEE Asian solid-state circuits conference, Nov 2009, pp 225–228

Sun Y, Jiao H, Kursun V (2015) A novel robust and low-leakage SRAM cell with nine carbon nanotube transistors. IEEE Trans Very Large Scale Integr (VLSI) Syst 23(9):1729–1739

Tu MH et al (2012) A single-ended disturb-free 9T subthreshold SRAM with cross-point data aware write word-line structure, negative bit-line, and adaptive read operation timing tracing. IEEE J Solid-State Circuits 47(6):1469–1482

Vaddi R, Dasgupta S, Agarwal RP (2010) Device and circuit co-design robustness studies in the subthreshold logic for ultralow-power applications for 32 nm CMOS. IEEE Trans Electron Devices 57(3):654–664