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TECHNICAL PAPER

LCNT-an approach to minimize leakage power in CMOS integrated circuits

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Abstract Leakage power dissipation is the dominant contributor of total power dissipation in nanoscale complementary metal oxide semiconductor (CMOS) integrated circuits. CMOS technology scaling demands for a reduced power supply, low threshold voltage, high transistor density and reduced oxide thickness, which has led to significant increase in leakage power especially during standby mode. Here in this paper, at first we review some of the existing techniques for leakage minimization and pointed out their merits and shortcomings. We then propose a novel transistor level approach called leakage control NMOS transistor (LCNT) for leakage minimization. The proposed technique inserts two leakage control transistors (all N-type) within a standard CMOS logic circuit. The gate terminal of the leakage control transistors are connected with the drain of the pull-up transistors. Performance of the proposed technique is investigated in terms of area, power, delay, and power-delay product applying on some basic gates and benchmark circuits. The performance metrics of the proposed LCNT are then compared with other existing techniques. Extensive SPICE simulations were carried out using 32 nm predictive technology model. Simulation results indicate that the proposed technique is quite efficient in minimizing the leakage power which is found out to be 48.4 %.

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1 Introduction

In recent years, increasing demand of portable digital systems has led to rapid and innovative development in the field of low power design. The development of these portable devices requiring high performance and low power dissipation such as in mobile phones, notebook computers and personal digital assistants (PDAs). In high performance digital VLSI systems like microprocessor, digital signal processor and other applications, power dissipation is a major concern. High power dissipation reduces battery life and it requires extra cooling and packaging cost. Power consumption in a logic gate can be expressed (by Sayed and Al Asaad 2006) as

$$P_{total} = P_{dynamic} + P_{short} + P_{static} \quad (1)$$

The above equation shows three sources of power consumption, (1) $P_{dynamic}$ is due to the charging and discharging of output node capacitance, (2) $P_{short\text{-}circuit}$ is due to the conducting path between the supply and ground, (3) P_{static} is due to the leakage current.

In designing a VLSI circuit area, power dissipation and propagation delay are the major design parameters. Today, complementary metal oxide semiconductor (CMOS) device size has been scale down drastically to achieve the performance metrics of VLSI chips (Ekekwe and Etienne-Cummings 2006). As the technology scaled down to deep nanometer level, the power supply, threshold (V_t) and device geometry gets reduces (Chin et al. 2005). The sub-threshold current continue to increase exponentially, when the V_t of the device is reduced. The leakage current is now a dominant part of total power dissipation as the technology scales down (Butzen et al. 2010).

According to international technology roadmap for semiconductor (ITRS), total power consumption is

significantly contributed by the leakage power (as per International Technology Roadmap for Semiconductor 2009). It is expected that leakage power can increase up to 32 times per device (Roy et al. 2000). So it is important to need robust technique to reduce leakage power dissipation.

There are three primary concepts for reducing the leakages at gate level designs. These are body-biasing, multi-threshold techniques and transistor stacking (Tsui et al. 2008). In this paper, we analyze first the leakage minimization techniques, which have been proposed earlier for CMOS VLSI circuits. Then, we propose a new circuit technique called leakage control NMOS transistor(LCNT), which is self controlled and does not require any control circuitry to monitor the state of the circuit.The remainder of the paper is organized as follows. Section 2 describes the background work. Section 3 discusses the proposed design. Section 4 gives the analysis of the results. Finally, Sect. 5 concludes this paper.

2 Background

Many design techniques have been proposed to minimize leakage power. Multi-threshold CMOS (MTCMOS) (Mutoh et al. 1995) has been found to be very effective technique to minimize leakage in standby mode. The main drawbacks of the technique are: firstly, the propagation delay increases due to the presence of high V_t sleep transistor in active mode. Secondly, proper sizing of sleep transistors in a large circuit is a very tedious task. Moreover, timing is a critical concern for sleep signal generation and finally the data retention is also a big problem, when the sleep transistors are turned OFF. The variable threshold CMOS (VTMOS) reduces the standby power by increasing the V_t with body bias. But the major drawback of this technique is that it requires an additional circuitry for body bias generation (Kuroda et al. 1996). In dual threshold CMOS (DTMOS) (Drake et al. 2003), high V_t transistors are used in non-critical path to reduce the leakage current and low V_t transistors are used to improve logic performance. But the overall delay of circuit increases due to high V_t transistors. In stack effect (Narendran et al. 2001), two or more series transistors are turned OFF to reduce the leakage current in standby mode, however area is a penalty in this approach. The sleepy stack (Park et al. 2004) approach combines the sleep and stack approaches. This technique reduces the leakage power and delay, but the area penalty is significant issue in this approach as every transistor is replaced by three equivalent transistors. The leakage feedback approach (Kao and Chandrakasan 2001) solves the problem of data retention by utilizing two additional helper transistors to maintain logic state during sleep mode, but the area and the delay are the other issues in this approach.

Sleepy keeper utilizes the idea of leakage feedback technique (Hun and Mooney 2006). But it does not require any inverter at the output node as because the helper transistors positions are interchanged in the leakage feedback path. Data retention is not a problem in this approach but the signal level at the output node is weak in standby mode.

LECTOR (Hanchate and Ranganathan 2004) technique utilizes two leakage control transistors (LCTs) which are inserted between pull-up network (PUN) and pull-down

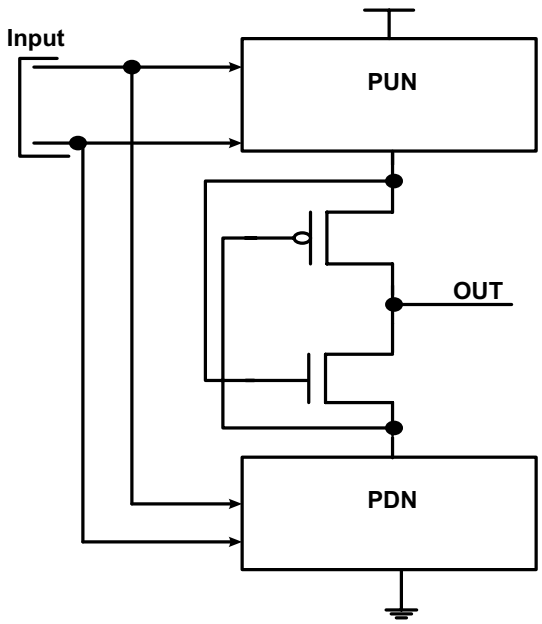

Fig. 1 LECTOR

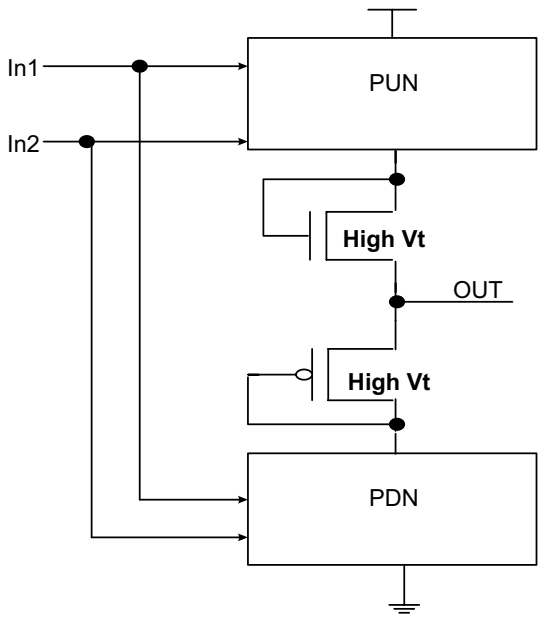

Fig. 2 GALEOR

network (PDN) in a CMOS gate as illustrated in Fig. 1. LCTs causes increase in the resistance of the path from V_{dd} to ground. In this arrangement, one of the LCT is always near its *cutoff* region, leading to significant decrease in leakage current. The wiring condition ensures that one of the LCTs will be near to its *cutoff* region irrespective of logic inputs applied to the logic gate. The basic idea behind this approach is the reduction of leakage power by effective stacking of transistor from supply voltage to ground. It is observed that when more than one transistor is OFF from supply voltage to ground, it is far less leaky than when only one transistor is in OFF state as in Narendra et al. (2001) and Sirichotiyakul et al. (2002). LECTOR does not require any control circuitry to monitor the states of the circuit. In this way it avoids the sacrifice of dynamic power which is consumed by additional circuitry. This technique is good for leakage reduction but this technique is not capable of reducing propagation delay.

GALEOR technique uses the same structure as LECTOR, except that the locations of extra gate leakage transistors (GLT) are now swapped as shown in Fig. 2. These GLTs are high V_t transistors offering higher resistance to leakage currents. A PMOS GLT is located between PDN and output whereas, an NMOS GLT is located between PUN and output (Katrue and Kudithipudi 2008). Leakage power saving is achieved by using high V_t.GLT transistors. GALEOR technique however, suffers a significant problem that the low signal level is very much higher than 0 V and high signal level is very much lower than V_{dd}. ONOFIC(Sharma and PattanaikM 2014) is a circuit level leakage reduction technique called on/off logic approach. ONOFIC logic block is inserted between PUN and PDN as shown in Fig. 3.

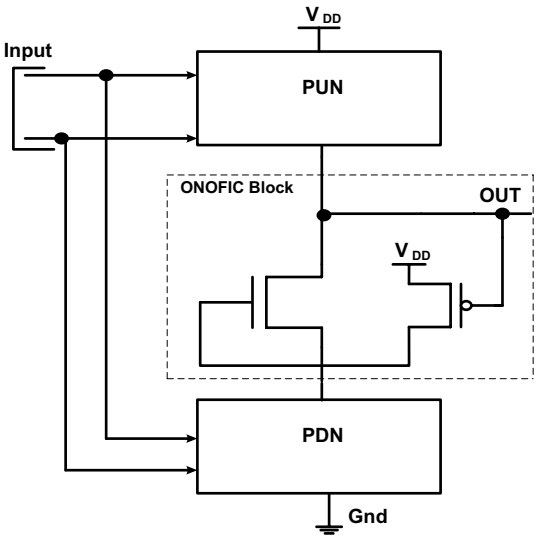

Fig. 3 ONOFIC

The logic block is called ONOFIC because for any output logic level this logic block must be in ON or OFF condition. If ONOFIC block is in 'ON' condition it shows that both the ONOFIC transistors are in linear region while in 'OFF' state both the transistors are in *cutoff* mode. This approach is simple and needs single threshold extra insert transistor. The propagation delay penalty in this technique is also less than LECTOR technique because single NMOS transistor between PUN and PDN is used to control the leakage current. On the other hand, leakage minimization in this technique is not as good as LECTOR technique because only a single NMOS transistor is creating the leakage resistance path between PUN and PDN.

There is another low leakage transistor level approach called INDEP (input dependent) (Sharma et al. 2015). The idea behind this approach is to reduce the leakage power by effective transistor stack in the path from voltage supply to ground. INDEP approach uses two extra inserted transistors between PUN and PDN. The V_t of this approach is same as PUN and PDN. This technique is good in reducing the leakage power. However, the leakage saving in this approach is based on appropriate selection of boolean logic input signals. So, the selection of input signals is needed to be done by algorithms which take extensive computational time.

3 Proposed design

The proposed technique is a circuit level approach for minimizing the leakage current in CMOS logic gate. This technique is called leakage control NMOS transistor (LCNT). Because, it uses two N-type leakage control transistors LCT1 and LCT2 which are inserted between PUN and PDN as shown in Fig. 4. The gate terminal of both LCT1 and LCT2 are connected to NP which is the output node. The switching of both the LCT's are controlled by the voltage at the node NP.This technique is further illustrated with the help of a CMOS NAND gate as shown in Fig. 5.

When input vector AB = 00, both the NMOS transistors MN1 and MN2 are turned OFFin PDN and both the PMOS transistors are turned ON in PUN. As a result, both the leakage control transistors (LCT1and LCT2) are turned ON. As the LCTs are in series and are turned ON so there is 2 V_t drop which will cause a reduced voltage in the path from output node to ground. Moreover, the two OFF NMOS transistors (MN1 and MN2) are offering more resistance, so we can expect a reduced leakage current. Again, when the input vectors are AB = 01 or 10, it will turn OFF one of the NMOS transistor in PDN and turn OFF one of the PMOS transistor in PUN. So, both the LCTs will behave exactly in the same manner as when the input vector AB = 00. In the case of input vector AB = 11, both the

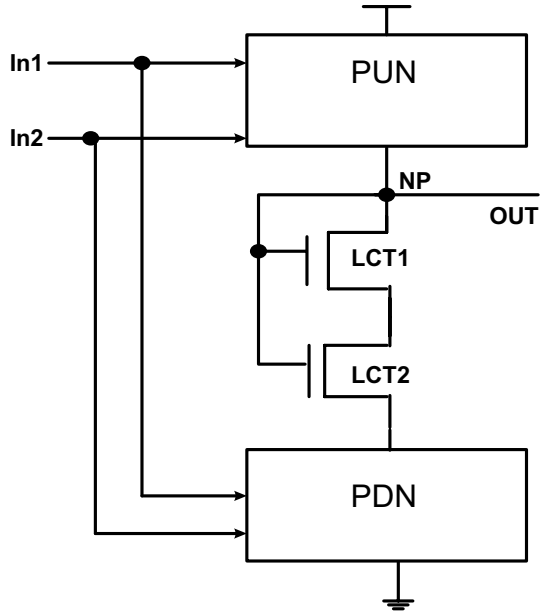

Fig. 4 Generalized structure for LCNT

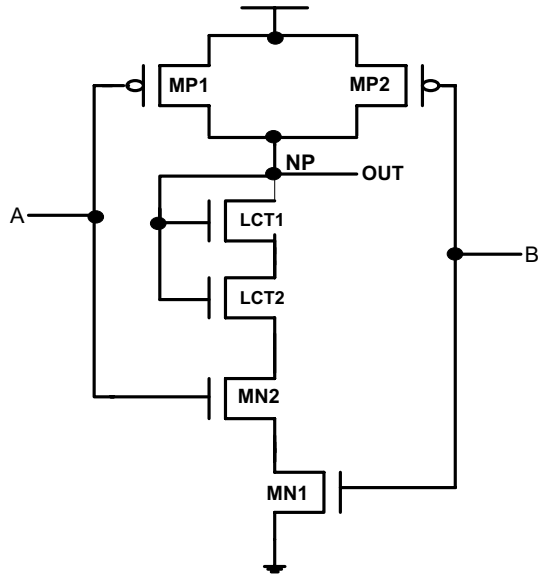

Fig. 5 Two input LCNT NAND gate

PMOS transistors are turned OFF in PUN and both NMOS transistors are turned ON in PDN. So both the leakage control transistor enters into their cut-OFF region, thereby offering highest resistance (due to stack effect) to any leakage current that would flow from PUN to PDN. Hence, it minimizes the leakage although both the NMOS transistors MN1 and MN2 are ON. Thus, it is clear that when the LCTs are ON they provide a good conducting path with minimum delay.

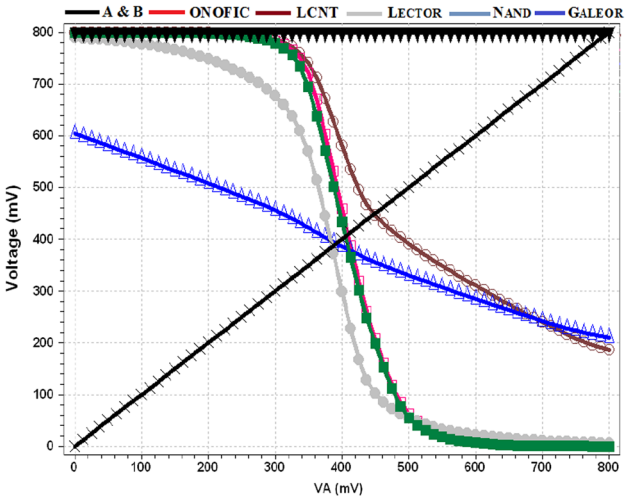

Fig. 6 Simulated DC characteristic of 2-input NAND gate

Whereas, when the LCTs are OFF, it provides the stacking effect. Consequently, it minimizes the leakage current. The proposed technique uses the same V_t devices for the entire circuit. This technique also solves the problem of using dual V_t transistors which can reduce the performance of the circuit. There are few other techniques in the literature which also uses the same V_t such as LECTOR and ONOFIC.

Simulated DC characteristics of conventional, LECTOR, GALEOR and LCNT using 2-input NAND gates are shown in Fig. 6. The DC transfer characteristic is obtained through simulation, keeping input B fixed to 1 V and A is varied from 0 to 1 V. In CMOS circuits, propagation delay of a gate (Park and Mooney 2006) is approximately given by

$$t_{pd}\alpha\frac{C_L V_{dd}}{I_{DS}} = \frac{C_L V_{dd}}{A(V_{dd}-V_t)^2} \tag{2}$$

where, C_L is the load capacitance, V_{dd} is the supply voltage, I_{DS} is the drain current in the saturation, V_t is the threshold voltage and A is a constant. From the expression of propagation delay we can expect that as we increase the load capacitance, delay time (t_{pd}) will increase. Again with a high drain current (I_{DS}) delay will be small. In the proposed design, we have a higher output node capacitance. So, we expect delay to rise, but this is nullified by the increase in drain current because of additional capacitive load as observed in DC characteristic. Leakage current in MOSFET devices is mainly guided by sub-threshold leakage current.

Sub-threshold current also vary exponentially with V_t (Kao and Chandrakasan 2000) and can be given as:

$$I_{leakage} = \frac{W}{W_0} I_0 e^{(V_{gs}-V_t)/nV_{th}} = \frac{W}{W_0} I_0 10^{(V_{gs}-V_t)/S} \tag{3}$$

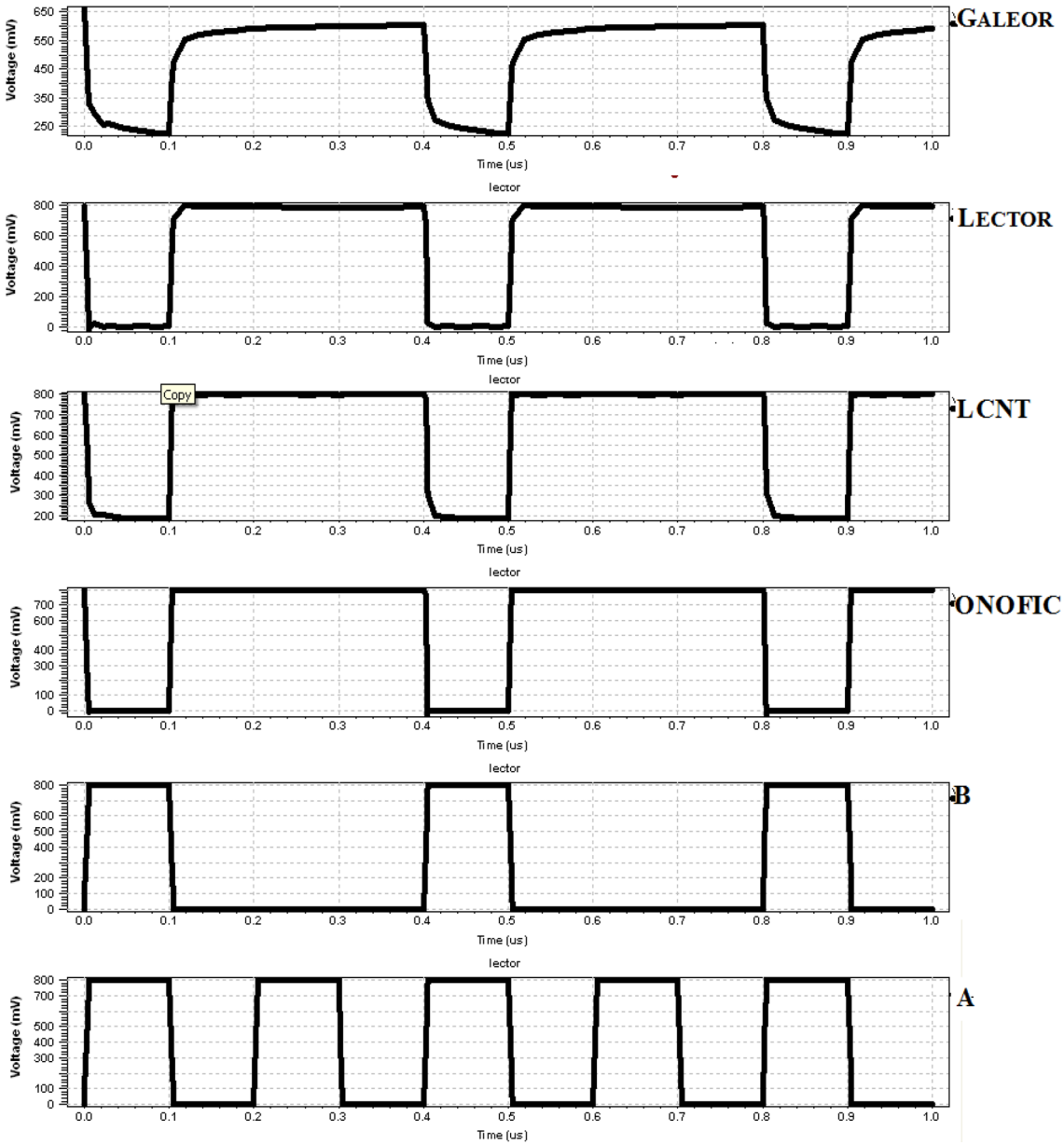

Fig. 7 Transient characteristic of 2-input NAND gate

Table 1 Comparison leakage power dissipation (W) for two input vectors

NAND	00	01	10	11	Total
Conventional	2.23E−10	1.78E−09	5.83E−09	1.67E−08	2.45E−08
LECTOR	1.60E−10	1.47E−09	2.01E−09	3.77E−09	7.41E−09
GALEOR	1.49E−10	9.12E−10	1.56E−09	1.92E−09	4.54E−09
ONOFIC	1.60E−10	1.47E−09	2.02E−09	1.69E−08	2.06E−08
LCNT	1.53E−10	1.36E−09	1.62E−09	3.85E−09	6.98E−09

where, V_{th} is thermal voltage, W is width, n is a constant and $S = nV_{th}$ ln0 is the sub-threshold slope of 100 mV/decade, which means for each 100 mV, decrease in V_t will cause an order of magnitude increase in leakage current.

Figure 6 shows the DC transfer characteristics of GALEOR, LECTOR, LCNT and the proposed designs as obtained through T-Spice simulation. LECTOR shows near to ideal DC transfer characteristics with a transition delay

time of about 200 µS. If we look at the transfer characteristics of GALEOR, we find that it is the worst amongst all.

In case of LCNT, the logic *high* is good and approaching to ideal transfer characteristics. However, the logic *low* is poor. But if we look at the transition time of all the plots, we find that LECTOR is as close as the conventional design and is about 200 µs, however, for LCNT it is 250 µs.

Figure 7 shows the transient curve obtained by TANNER EDA tool at various nodes of all designs simulated for 32 nm technology at 0.8 V supply voltage. It can be observe from the curve LCT NAND gate produces exact output voltage levels. In case of GALEOR technique, the output voltage level is not considered to be a good '0' and a good '1'. However, in case of proposed LCNT technique, the output waveform gives a good logic '1' but the logic '0' is not as good as ONOFIC.

4 Results

In this section, we compare and analyze the area, average power, delay and power-delay product (PDP) of the proposed design with conventional, LECTOR, GALEOR and ONOFIC. To analyze the performance matrices, we have used Tanner EDA tool using 32 nm PTM (predictive technology model) technology with a power supply of 0.8 V.

4.1 Leakage power

To estimate the leakage power accurately, at first the static leakage for each static input vector is calculated and thereafter, it is summed up to get the total leakage. This way, the total leakage power is calculated for all possible input vectors. Table 1 show the leakage power results for the case of a two input NAND gate, where the total leakage is computed as the sum of leakages for all possible input vectors. Similarly, for all the benchmark circuits and CMOS logic gates leakage power is calculated and the values are displayed in Table 2. Here in the calculation we have not considered any power dissipation due to switching activity. The percentage of leakage power saving is compared with the conventional circuit. Leakage power dissipation is

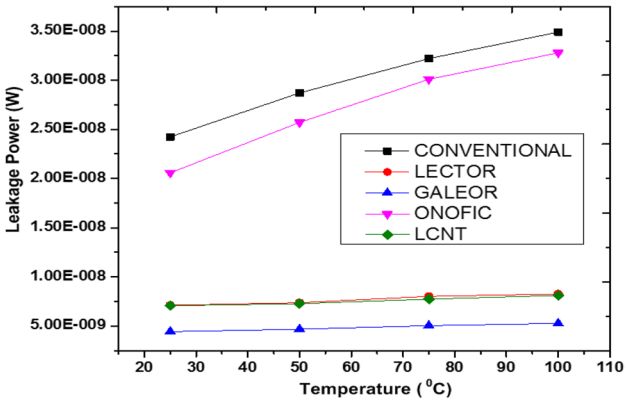

Fig. 8 Leakage power dissipation at different temperature for NAND gate

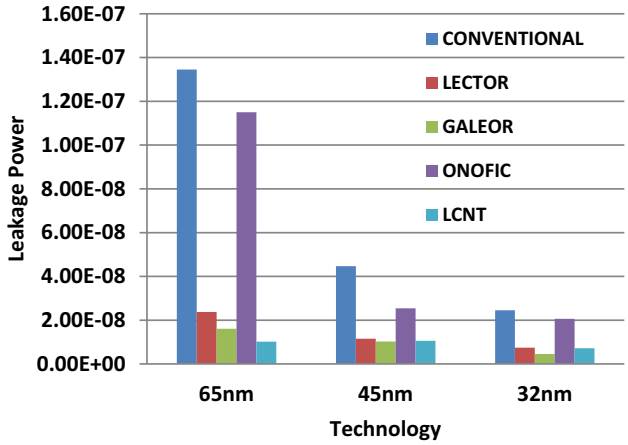

Fig. 9 Leakage power dissipation of CMOS NAND gate at different technologies

a function of temperature (Faraji et al. 2013). Comparative results of static power dissipation at different temperature are also shown in Fig. 8. We can observe from the figure that as we go on increasing the temperature, leakage power dissipation of the circuit increases gradually. We have also analysed the comparative results of all the techniques at different technology nodes such as 65, 45 and 32 nm

Table 2 Leakage power dissipation (W)

	NAND	NOR	B1	C17	Average saving (%)
Conventional	2.45E−08	2.22E−08	1.15E−03	5.23E−04	–
LECTOR	7.41E−09	7.51E−09	8.78E−04	6.87E−05	43.40
GALEOR	4.54E−09	6.35E−09	7.24E−04	6.15E−05	53.00
ONOFIC	2.06E−08	1.50E−08	1.02E−03	4.95E−04	9.44
LCNT	6.98E−09	7.93E−09	7.98E−04	6.45E−05	48.40

Table 3 Leakage power effect of variation of W/L ratio of LCT on LCNT technique

LCT sizes	00	01	11	10	Total
W = 48, L = 32	1.50E−10	1.31E−09	3.71E−09	1.61E−09	6.78E−09
W = 64, L = 32	1.53E−10	1.36E−09	3.85E−09	1.62E−09	6.98E−09
W = 80, L = 32	1.55E−10	1.39E−09	5.31E−09	1.78E−09	8.63E−09
W = 96, L = 32	1.56E−10	1.41E−09	5.53E−09	1.82E−09	8.92E−09

Table 4 Delay (s)

	NAND	NOR	B1	C17	Average penalty (%)
Conventional	1.51E−09	1.59E−09	2.06E−05	5.21E−06	–
LECTOR	1.96E−09	2.04E−09	2.37E−05	5.15E−06	10.50
GALEOR	3.17E−09	2.89E−09	2.54E−05	5.68E−06	19.80
ONOFIC	1.53E−09	1.54E−09	2.18E−05	5.27E−06	4.65
LCNT	1.91E−09	1.96E−09	2.30E−05	5.45E−06	9.28

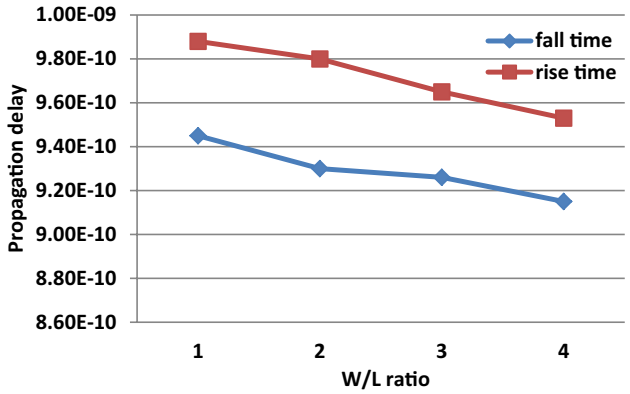

Fig. 10 Propagation delay effect of variation of W/L ratio of LCT on LCNT technique

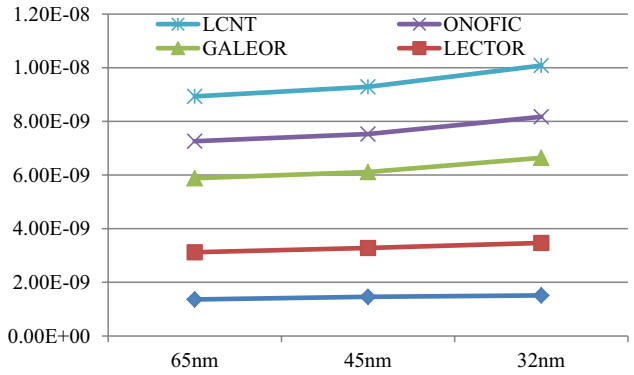

Fig. 11 Comparative delay of various techniques at different technologies

4.2 Delay

Table 5 Power-delay product (J)

	NAND	NOR	B1	C17	Average saving (%)
Conventional	3.70E−17	3.51E−17	2.37E−08	2.72E−09	–
LECTOR	(−)1.41507E−17	(−)1.46887E−17	(−)2.02E−08	(−)3.74E−10	22.10
GALEOR	(−)1.43E−17	(−)1.831E−17	(−)1.91E−08	(−)3.56E−10	26.30
ONOFIC	(−)3.1458E−17	(−)2.30115E−15	(−)2.22E−08	(−)2.61E−09	6.09
LCNT	(−)1.41E−17	(−)1.61902E−17	(−)1.89E−08	(−)3.32E−10	27.20

which are displayed in Fig. 9. It is to be noted that with technology scaling apart from $V_{t,}$ the power supply V_{dd} is also scaled which causes the overall power dissipation to reduce, although leakage power increases.

Table 3 shows as we go on increasing W/L ratio LCTs in LCNT circuit, the leakage power increases. The leakage power dissipation can be ranked in the increasing order as follows: GALEOR < LCNT < LECTOR < ONOFIC < Conventional.

Table 6 Area comparison $(\mu m)^2$

	NAND	NOR	B1	C17	Average penalty (%)
Conventional	29.5	29.7	5946	4929	–
LECTOR	32.5	31.6	6258	5710	9.13
GALEOR	32.5	31.1	6458	5880	11.84
ONOFIC	33	32.5	6578	6032	13.74
LCNT	32	31	6196	5637	8.09

Table 7 Active Power (W)

	NAND	NOR	B1	C17	Average saving (%)
Conventional	2.43E−06	4.66E−06	9.34E−04	2.45E−05	–
LECTOR	1.73E−06	2.32E−06	8.35E−04	2.31E−05	10.70
GALEOR	5.32E−07	1.71E−06	7.64E−04	1.78E−05	18.80
ONOFIC	1.93E−06	2.64E−06	8.53E−04	3.80E−05	7.25
LCNT	5.12E−07	1.42E−06	7.13E−04	1.23E−05	24.70

Table 4 shows the comparative analysis of propagation delay in case of conventional, LECTOR, GALEOR and LCNT based circuits. In all the techniques, extra leakage control transistors are inserted to reduce the leakage power but these extra transistors raises the propagation delay of the circuit. The increasing order of propagation delay for different approaches can be given as conventional < ONOFIC < LCNT < LECTOR < GALEOR. Among all the techniques, ONOFIC has the least propagation delay and GALEOR has the highest propagation delay. In LCNT, as two NMOS LCTs are inserted itgives a better speed of operation than LECTOR. From Fig. 10, we can observe that, as we go on increasing the W/L ratio of LCTs, the rise and fall time of LCNT decreases. Figure 11 shows that as technology node shrinks down, the delay of the circuit slightly increases in almost all the techniques which is because of additional leakage control transistors. Whereas in case of conventional circuit the delay remains almost the same.

4.3 Power-delay product (PDP)

Table 5 presents power-delay product (PDP) of all the designs. The (−) sign indicates that power delay product is decreasing with respect to conventional circuit. It can be observed that LCNT technique have minimum PDP.

4.4 Area Comparison

Layout area of each of the target circuit, using a particular design style is measured in microwind tool with 32 nm technology. Table 6 shows the area estimation in the target circuits using the proposed and other existing designs. As the proposed technique uses two additional leakage control transistors, so the area in the LCNT is more than conventional design.

4.5 Active power dissipation

Active power is measured by calculating the average power dissipation while asserting semi-random input vectors. The size of semi-random input vectors depend on the number of inputs present in the circuit. Both the static and dynamic power are included in active power calculation. We measure the active power of CMOS logic gates and benchmark circuits by asserting all the input vectors. Table 7 shows that the proposed design has the highest active power saving than all the other designs. This is because of low dynamic power consumption caused by reduced switching activity in the N-type LCTs and low static power consumption due to stack effect.

5 Conclusion

In nanoscale CMOS circuits, leakage power has become a more dominating component of total power consumption in battery operated portable systems. Here in this paper, LCNT-a new self controlled low leakage approach has been presented for nanoscale CMOS circuits. It has been observed that LCNT provides a better leakage reduction with minimal propagation delay, consequently giving a least value of PDP. We have analyzed and evaluated the performance level of the proposed approach and compared it with the existing leakage reduction techniques. It is found thatthe proposed technique minimizes the average leakage by about 48.40 %.

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