

# Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET

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**Abstract** In this work, the impact of parameter variation on hot-carrier effect immunity in transparent gate recessed channel (TGRC)—MOSFET based on the hydrodynamic energy transport model have been studied. The parameters of TGRC-MOSFET investigated include the oxide thickness, negative junction depth, and substrate doping. TCAD analysis shows the performance of TGRC-MOSFET in terms of transfer characteristics, transconductance, electric field, electron velocity, electron mobility and electron temperature. The simulation results indicate the improved hot-carrier immunity for TGRC-MOSFET in 30 nm device.

## 1 Introduction

The size of MOSFET's has been constantly scaled down to achieve advanced speed and packing density in VLSI technology. Apart from the intricacy of designing devices at these nanometer scales, high power dissipation and an increase in device temperature are prime concerns in semiconductor device design. The hot-carrier deprivation becomes the severe limitation to the reliability of nanometer devices and the packing density of VLSI (Ren and Hao 2002). Hot-carrier effect can be suppressed by reducing the supply voltage and gate oxide thickness (Fiegna et al. 1994),

but the supply voltage and gate oxide thickness are becoming inherent limits in nanometer regime. Under the influence of high lateral fields in short-channel MOSFETs, carriers in the channel and pinch-off regions of the transistor reach non-equilibrium energy distributions. The generation of these hot-carriers is the primary source of several reliability problems (Gupta et al. 2014). Hot-carriers can acquire sufficient energy to surmount the energy barrier at the Si–SiO<sub>2</sub> interface or tunnel into the oxide (Kumar et al. 2014b).

In MOSFETs, the substrate's hot carriers have been attracted towards the source and the drain electrode by the strong channel electric field before they get to interface when the device is scaled down to 100 nm regime. Therefore, sharp decrement in substrate hot-carrier is observed and then the influence of channel hot-carrier plays a dominant role in 100 nm device degradation (Ren and Hao 2002). These kind of mobile carriers in device create some physical damage which might change the device characteristics. Numerous device engineering schemes and novel device structures have been reported in the literature to overcome the problems arising from downscaling of device dimensions. Further scaling has faced serious limitations with respect to fabrication technology and device performances. Many solutions are proposed to overcome these limitations. Some of the solutions include such as SOI MOSFET (An et al. 2004), multi-gate MOSFET (Biswal et al. 2015), Recessed Channel (RC) MOSFET (Chaujar et al. 2008b), GAA MOSFET (Moreno et al. 2015), Silicon Nanowire MOSFET (Gupta et al. 2015a, b) etc. Conventional Recessed Channel MOSFET (CRC) MOSFET improves the short channel effects (SCEs) and HCEs appreciably because of the presence of groove which splits the source and drain regions.

In TGRC-MOSFET (Kumar et al. 2015, 2016a, b), a transparent conducting oxide is used instead of a metallic gate as it

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has a relatively high concentration of free electrons in its conduction band. The free electrons arise either from defects in material or from extrinsic dopants, the impurity levels of which lie near the conduction band edge. Transparent conducting oxides open a broad range of power saving optoelectrical circuits. Electrical conductivity and optical transparency of indium tin oxide (ITO) is quite high and the ease with which it can be deposited as a thin film makes it a desirable option. The circuit can be improved by using ITO since it decreases the device power consumption (Pammi et al. 2011).

The metal gate is replaced by a transparent conducting oxide (Edwards et al. 2004; Kawazoe and Ueda 1999) called ITO. ITO is a solid solution with doped impurity of indium oxide ( $\text{In}_2\text{O}_3$ ) and tin oxide ( $\text{SnO}_2$ ). Commercially available ITO has a resistivity in the order of  $1 \times 10^{-5} \Omega\text{-cm}$  (Minami 2005). It is transparent and colorless in thin layers. ITO is one of the most widely used transparent conducting oxides because of its two chief properties, its electrical conductivity and optical transparency as well as the ease with which it can be deposited as a thin film (Chaujar et al. 2008a, b).

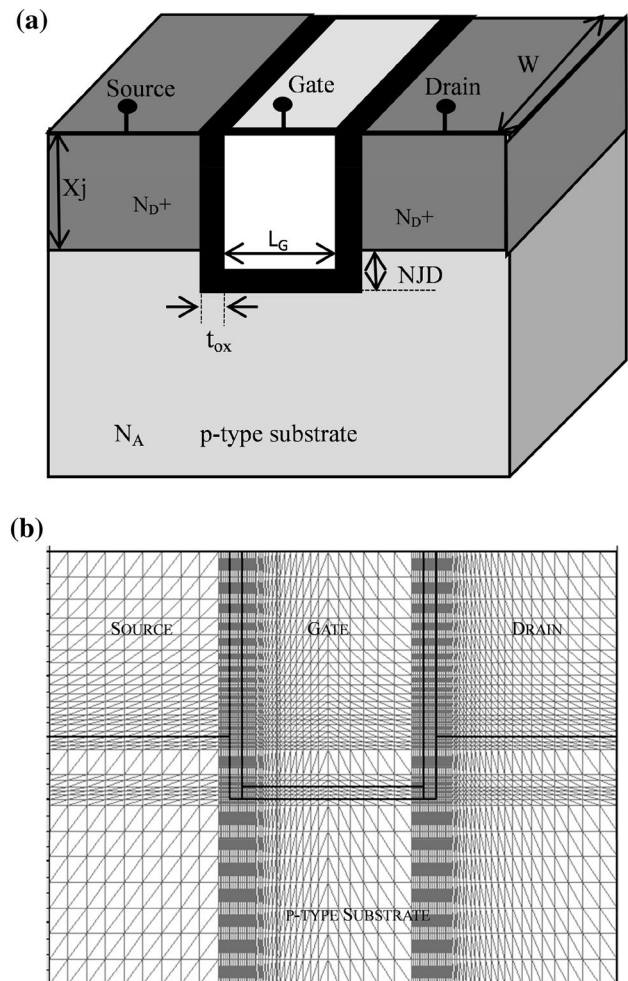
## 2 Device structure and its description

A schematic representation of the TGRC-MOSFET is shown in Fig. 1. ITO is a transparent conducting material and shows high transparency as well as good conducting material when the workfunction is 4.7 eV. Total gate length is 30 nm. Oxide thickness is varying from 1 nm to 3 nm and negative junction depth is varying from 5 nm to 15 nm. Here substrate doping is p-type with concentration of  $1 \times 10^{16}\text{cm}^{-3}$  and source/drain are n-type with uniform doping  $1 \times 10^{19}\text{cm}^{-3}$ . All the simulation have been done using ATLAS device simulator. Figure 1b shows the meshing in different regions of the device.

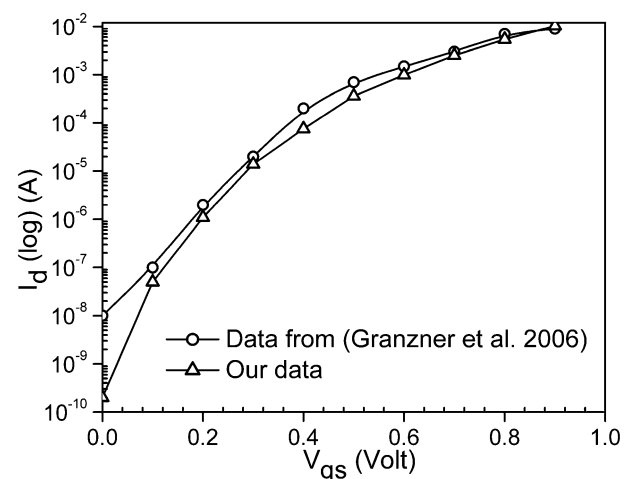
## 3 Simulation methodology and calibration

The simulations are based on the inversion layer Lombardi capacitance–voltage–temperature (CVT) mobility model with the Auger recombination model and Shockley-Read–Hall (SRH) for minority carrier recombination. Further, the hydrodynamic energy transport model comprising of the continuity equations, energy balance equations of the carriers, momentum transport equations and the Poisson equation have been used (ATLAS User’s Manual 2014).

Calibration of model parameters used in simulation has been performed according to the published results obtained (Granzner et al. 2006) using above mentioned models and the results are shown in Fig. 2. The data has been extended (Granzner et al. 2006) and then plotted.



**Fig. 1** a Schematic structure of transparent gate recessed channel MOSFET. b 2-D meshed structure of transparent gate recessed channel MOSFET



**Fig. 2** Calibration with the published result,  $I_{ds}$ – $V_{gs}$  characteristics of 40 nm gate length TGRC-MOSFET

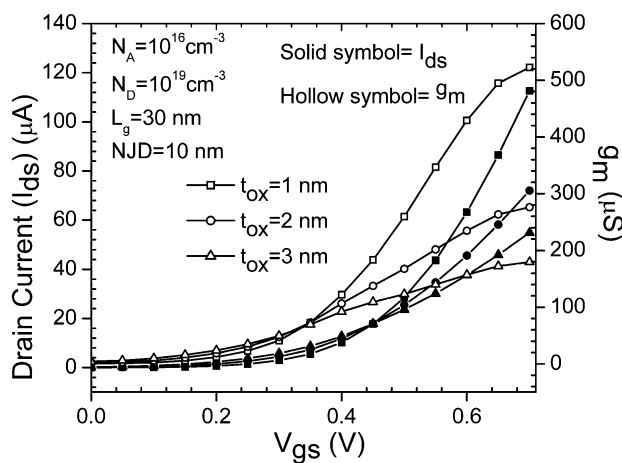
## 4 Result and discussion

### 4.1 Effect of oxide thickness

If gate length is scaled down to 25 nm with 1.6 nm oxide thickness then,  $I_{OFF}$  is 70 nA while if gate length is reduced below 20 nm (18 nm) with oxide thickness below 1.5 nm (1.3 nm), then  $I_{OFF}$  increases above 100 nA due to quantum effects and tunneling of electron and causes SCEs (mainly increase in  $I_{OFF}$ ) (Hu 2009; Iwai 2009) as mentioned in ITRS. Thus, there is need to optimize the value of oxide thickness. Therefore in this section, hot-carrier reliability of TGRC is studied in terms of oxide thickness.

In this section, the effects of oxide thickness variation have been observed. Figure 3 reflects the variation of the drain current ( $I_{ds}$ ) and Transconductance ( $g_m$ ) along the channel in TGRC-MOSFET at different oxide thickness. When oxide thickness is reduced from 3 to 1 nm,  $I_{ds}$  and  $g_m$  are enhanced because of more free charge carriers are generated in the channel due to the incorporation of ITO in gate region. These free charge carriers are contributing to enhancing the drain current. Thus, there are very less number of charge carriers which increases the hot-carriers in the channel and therefore hot carriers are reduced with the reduction of oxide thickness.

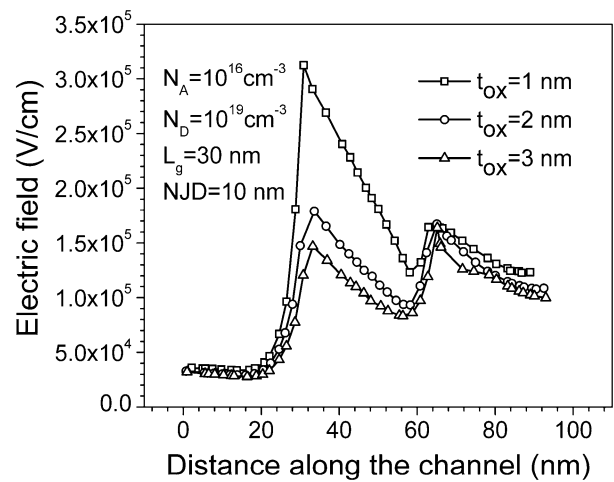
The hot-carrier effect is very sensitive to the electric field in the channel region (Ren and Hao 2002). Figure 4 shows variation of the electric field along the channel in TGRC-MOSFET at different oxide thickness. It is evident from Fig. 4 that electric field is very high on the source side as compared to drain side when the oxide



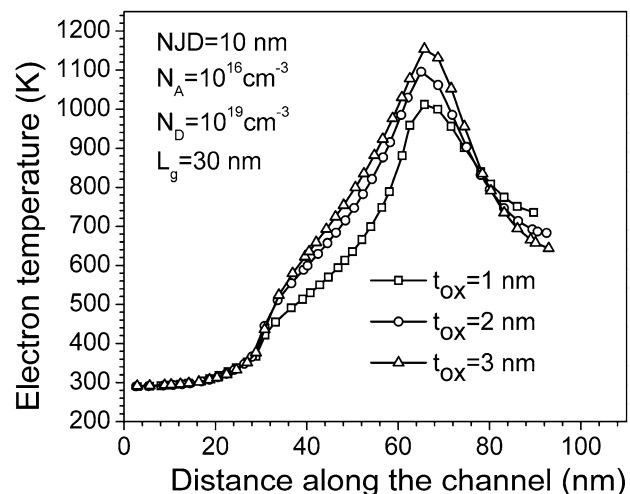
**Fig. 3** Variation of drain current ( $I_{ds}$ ) and transconductance ( $g_m$ ) w.r.t. gate to source voltage ( $V_{gs}$ ) in TGRC-MOSFET at different oxide thickness

thickness is 1 nm. If the oxide thickness is decreased from 3 to 2 nm, the electric field increases 29 % at the source side and increases 82 % when oxide thickness reduces from 2 to 1 nm, thus reflecting that if electric field is less at the drain side as compared to source side then the hot carrier generation will drop (Chaujar et al. 2008c).

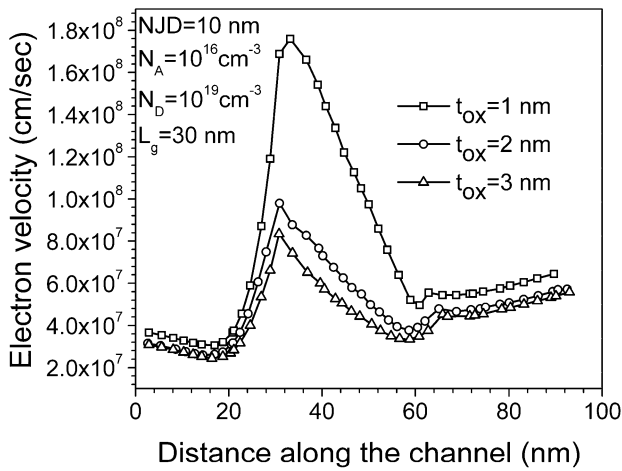
Variation of electron temperature along the channel for TGRC-MOSFET at different oxide thickness is shown in Fig. 5. For improved device performance, electron temperature should be low (Kumar et al. 2014b). When oxide thickness is reduced from 3 to 2 nm and then to 1 nm, the electron temperature reduces by 4.97 %. It is clearly evident that hot-carrier-effect is less pronounced when oxide



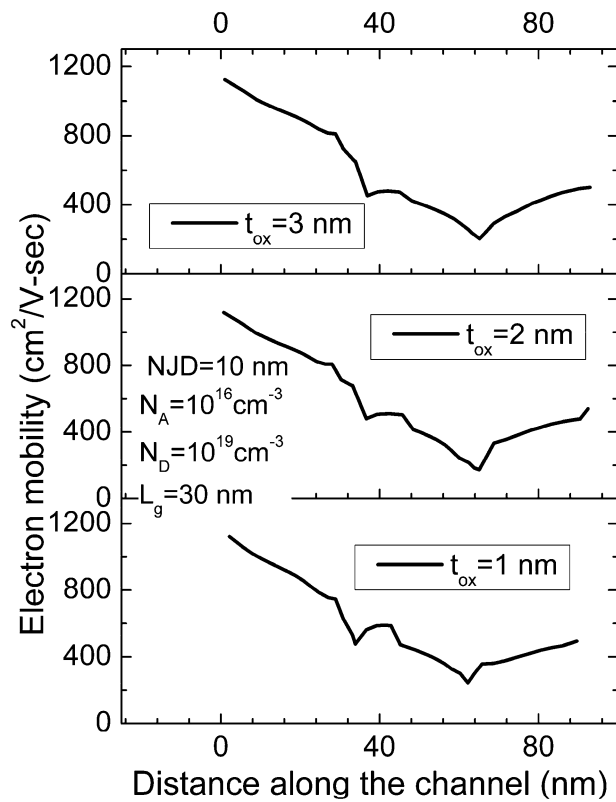
**Fig. 4** Variation of electric field along the channel in TGRC-MOSFET at various oxide thicknesses



**Fig. 5** Variation of electron temperature along the channel for TGRC-MOSFET at various oxide thicknesses



**Fig. 6** Variation of electron velocity along the channel in TGRC-MOSFET at various oxide thicknesses



**Fig. 7** Variation of electron mobility along the channel in TGRC-MOSFET at various oxide thicknesses

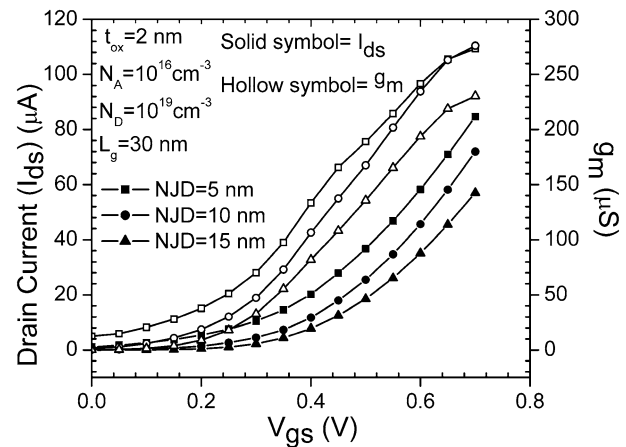
thickness is reduced. In the same manner, electron velocity increases at the source side nearly 19 % if oxide thickness decreases from 3 to 2 nm and increases 95 % when oxide thickness reduces from 2 to 1 nm as shown in Fig. 6.

Figure 7 shows the variation of electron mobility along the channel for TGRC-MOSFET at various oxide

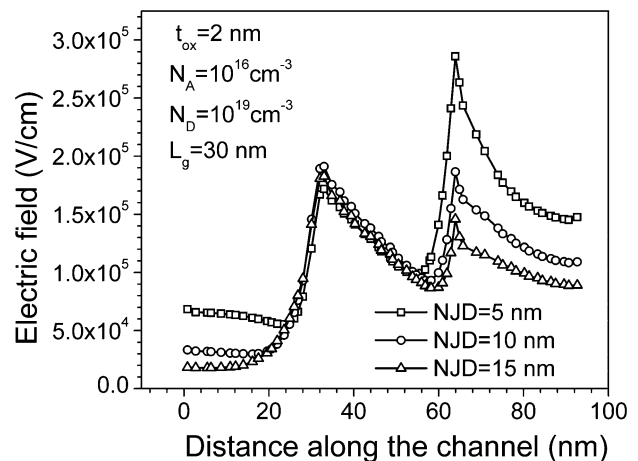
thicknesses. Electron mobility is high at source side in TGRC-MOSFET when oxide thickness is 1 nm and it is further decreases for 2 and 3 nm respectively. Electron mobility is lower at the drain side of 1 nm oxide thickness and increases when  $t_{ox}$  increases from 1 to 2 nm and further from 2 to 3 nm. Four scattering mechanisms largely stimulate the mobility of charge carriers in ITO thin films: lattice scattering, ionized impurity scattering, neutral impurity scattering, and grain boundary scattering (Thilakan and Kumar 1997).

#### 4.2 Effect of negative junction depth (NJD)

Further, different parameters of TGRC-MOSFET have been evaluated by the variation of negative junction depth (NJD). When NJD is reduced from 15 to 10 nm and from



**Fig. 8** Variation of drain current ( $I_{ds}$ ) and transconductance ( $g_m$ ) w.r.t. gate to source voltage ( $V_{gs}$ ) in TGRC-MOSFET at different NJDs



**Fig. 9** Electric field variation along the channel for TGRC-MOSFET at different NJDs

10 to 5 nm, drain current is enhanced by 26 and 17.5 % while transconductance is enhanced by 20 and 2.9 % respectively as decreasing the NJD causes more number of charge carriers to surpass from drain to source and hence, there is less impact of corner effect in TGRC-MOSFET. Thus hot-carriers are reduced causing an increase in drain current and transconductance as shown in Fig. 8.

Figure 9 shows electric field variation along the channel for TGRC-MOSFET at different NJDs. When NJD is reduced from 15 to 10 nm and further from 10 nm to 5 nm, it is observed that electric field is increased at source side by 6.8 and 18.8 % respectively while it decreases at the drain side. So we can say that with a rise in NJD, the reduction in the electric field at the drain end can be interpreted as a

reduction in hot carrier effects, higher device breakdown voltage and lower impact ionization (Kumar et al. 2014b).

Moreover, the variation of electron temperature has been observed at different NJDs. When NJD reduces from 15 to 10 nm and from 10 to 5 nm, then electron temperature is reduced by 27.3 and 24.1 % respectively at the drain side due to the incorporation of ITO (Kumar et al. 2015) as shown in Fig. 10. Figure 11 shows electron velocity variation along the channel for TGRC-MOSFET at different NJD. It is clearly evident from Fig. 11 that electron velocity increases on the source side as compared to drain side when NJD varies from 15 to 10 nm and further, 10 to 5 nm by 61.4 and 70.6 % respectively which reduced the hot carrier effects.

Electron mobility at the source is higher and lower at drain side when NJD is 15 nm and it reduces if the NJD reduces from 15 to 10 nm and further from 10 to 5 nm then the electron mobility enhanced by 0.7 and 2.6 % respectively as shown in Fig. 12. The main purpose of NJD is to eliminate short channel effects in the device. If NJD is tuned, then the probability of short channel effects will be less, but we need the reduction of short channel effects as well as higher mobility at source side for higher performance of the device. Here, optimized the device performance in terms of reduced SCEs and enhanced electron mobility. Higher electron mobility leads to a device for high switching applications such as logic gates.

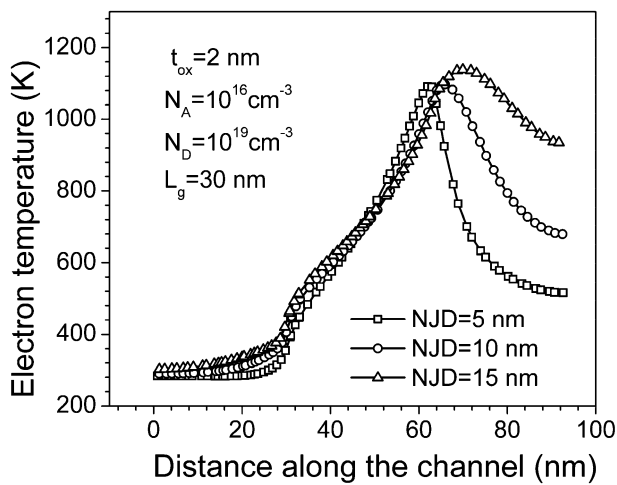


Fig. 10 Electron temperature variation along the channel for TGRC-MOSFET at different NJDs

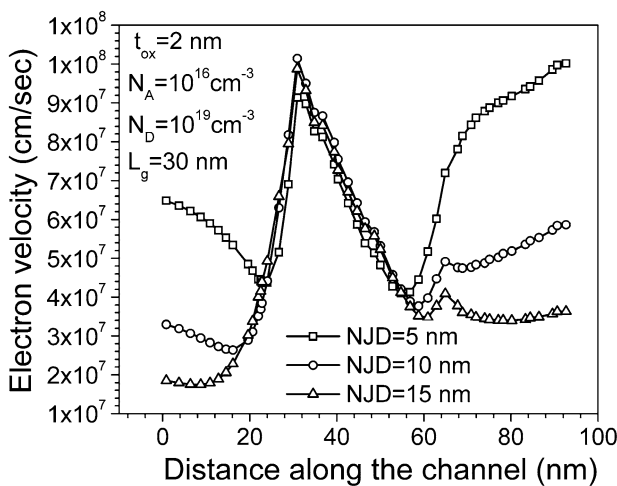


Fig. 11 Electron velocity variation along the channel for TGRC-MOSFET at different NJDs

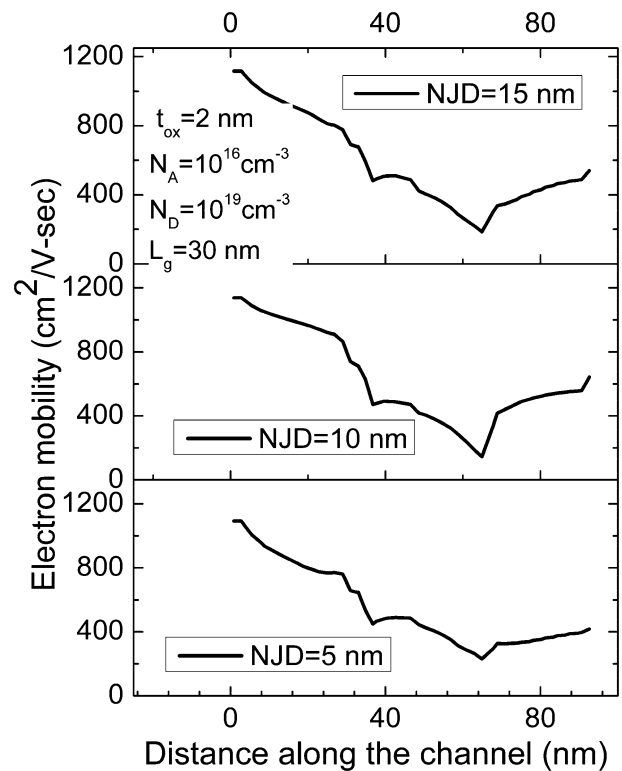


Fig. 12 Electron mobility variation along the channel for TGRC-MOSFET at different NJDs

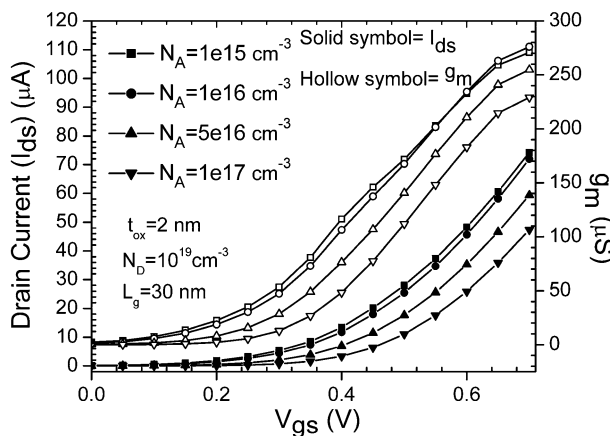
### 4.3 Effect of substrate doping

Yadav and Rana (2012) reported that if the substrate (channel) doping reduces, threshold voltage also reduces due to which driving current ( $I_{ON}$ ) and thus electron mobility enhances. Due to this reason, there is a need to study the effect of substrate doping on the performance of our proposed device. In this section, the efficacy of substrate doping on hot-carrier effects of TGRC-MOSFET has been studied.

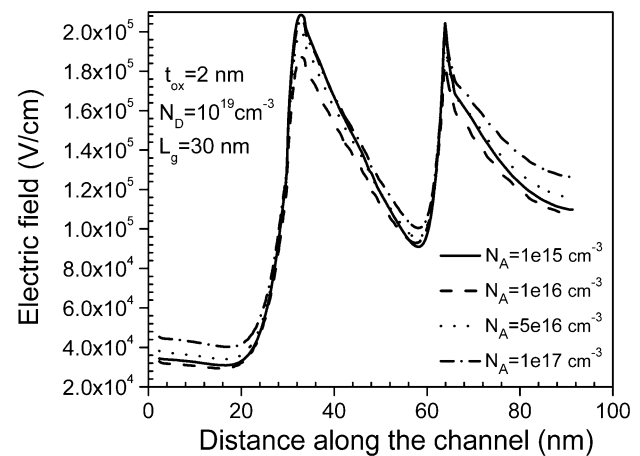
Figure 13 reflects the variation of drain current and transconductance in accordance with substrate doping. Both drain current and transconductance are enhanced with the reduction of substrate doping owing to reduction in threshold voltage of device due to more recombination of charge carriers and thus impact ionization of charge carriers are reduced causing the drain current and transconductance to enhance by 57.4 and 18 % respectively when substrate doping is reduced from  $1e17$  to  $1e15 \text{ cm}^{-3}$  in TGRC-MOSFET. Due to this, the gate controllability is improved and hot-carrier effects are reduced.

Further, the effect of substrate doping on the electric field has been observed. Figure 14 reflects the variation of the electric field along the channel, and it is observed that when substrate doping is reduced from  $1e17$  to  $1e15 \text{ cm}^{-3}$ , the electric field is enhanced by 2.3 % on the source side and reduced by 3.7 % at the drain side. Hence, the less electric field at the drain side reduces hot-carriers in the TGRC-MOSFET. Thus, reduction in hot-carrier effects leads to TGRC-MOSFET for high switching applications.

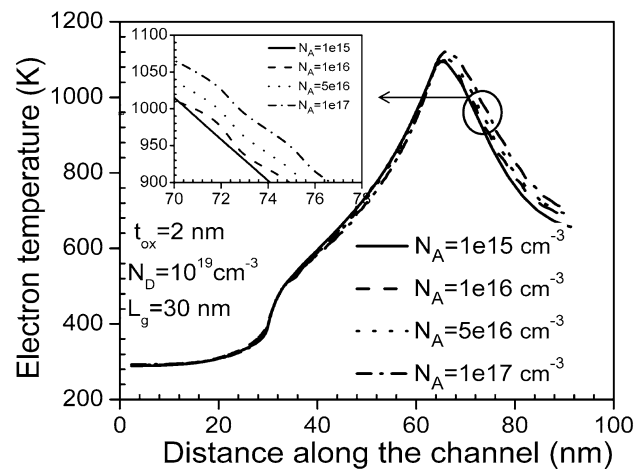
Figure 15 shows the variation of electron temperature along the channel length with a variation of substrate doping and it is clearly observed that the electron temperature is reduced by 6.67 % when substrate doping is reduced.



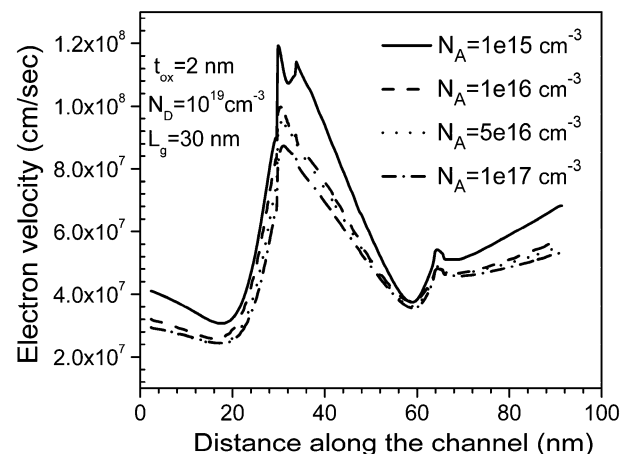
**Fig. 13** Variation of drain Current ( $I_{ds}$ ) and transconductance ( $g_m$ ) w.r.t. gate to source voltage ( $V_{gs}$ ) in TGRC-MOSFET at different substrate doping



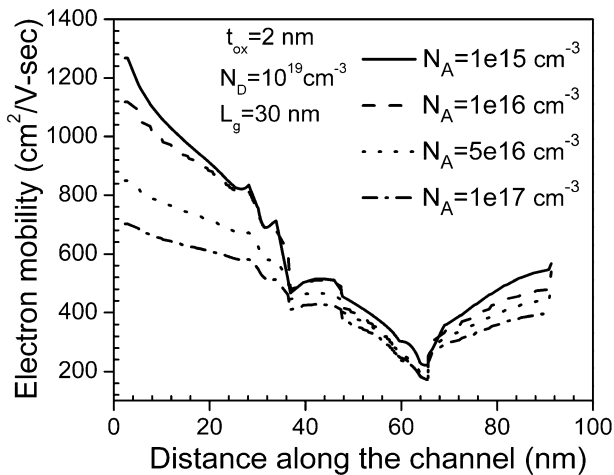
**Fig. 14** Variation of electric field along the channel in TGRC-MOSFET at various substrate doping



**Fig. 15** Variation of electron temperature along the channel in TGRC-MOSFET at different substrate doping



**Fig. 16** Electron velocity along the channel in TGRC-MOSFET at different substrate doping



**Fig. 17** Electron mobility along the channel in TGRC-MOSFET at different substrate doping

Thus, more hot-carrier immunity is observed when substrate doping reduces from  $1e17$  to  $1e15$   $\text{cm}^{-3}$ . Similar kind of work has been reported by Yadav and Rana (2012). Further, more hot-carrier degradation is observed in terms of electron velocity along the channel with the variation of substrate doping. Figure 16 shows that electron velocity is 28 % higher at source side as compared to drain side and it is increased when substrate doping is reduced from  $1e17$  to  $1e15$   $\text{cm}^{-3}$ . When substrate doping reduces then the velocity of charge carriers is more at the source end as compared to drain end.

Moreover, the efficacy of substrate doping variation on hot-carrier effects is observed in terms of electron mobility. Figure 17 depicts that electron mobility is higher (35.5 %) on the source side as compared to drain side and it is further enhanced when substrate doping is reduced from  $1e17$  to  $1e15$   $\text{cm}^{-3}$ . Electron mobility is inversely proportional to temperature. Thus, mobility is enhanced with the reduction of substrate doping; hence, the electron temperature is decreased in TGRC-MOSFET, which leads to TGRC-MOSFET for high-temperature applications.

## 5 Conclusion

Effect of structured parameters, such as NJD, oxide thickness and substrate doping are investigated to study the device's hot-carrier immunity. This study proves that the TGRC-MOSFET has a high hot-carrier immunity which is influenced by geometrical structure intensely. By reducing the oxide thickness and enhancing NJD, the capability of hot-carrier-immunity can be further increased. Thus, TGRC-MOSFET is a reliable device for high-performance applications in low power CMOS technology.

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