Microsyst Technol (2017) 23:4091–4098
DOI 10.1007/s00542-016-2872-9

TECHNICAL PAPER

Mathematical modeling insight of hetero gate dielectric-dual material gate-GAA-tunnel FET for VLSI/analog applications

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Received: 26 August 2015 / Accepted: 2 February 2016 / Published online: 22 February 2016
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Abstract This paper presents a mathematical modeling insight for the novel heterogate dielectric-dual material gate-GAA TFET (HD-DMG-GAA-TFET) and validating the results with TCAD simulation. By using the appropriate boundary conditions and continuity equations, the Poisson's equation is solved to obtain the potential profile. The developed model is used to study the analog performance parameters such as subthreshold swing (SS), threshold voltage (V_{th}), transconductance (g_m), drain conductance (g_d), device efficiency (g_m/I_{ds}), intrinsic gain (g_m/g_d), channel resistance (R_{ch}) and output resistance (R_o). Further, to optimize the effect of metal work function on analog performance, three different combinations of DMG configurations has been studied. The results demonstrated that for a difference of 0.4 eV, the analog performance of the device is optimized. Low off current and high value of on current resulting into a higher I_{ON}/I_{OFF} ratio has been obtained, which is appropriate for sub-nanometre devices and low standby power applications. The analytical results obtained from the proposed model shows good agreement with the simulated results obtained with the ATLAS device simulator.

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1 Introduction

Continuously scaling down the MOSFETs dimensions to sub-nanometer region lead to escalation in the power consumption (active and passive) in modern microelectronic circuits. Reducing the applied bias (according to the scaling factor) to solve this dilemma leads to reduction in gate overdrive. Along with higher power density, the fundamental limit of kT/q (due to thermal process) which corresponds to a subthreshold swing (SS) of 60 mV/dec also hindered further scaling of threshold voltage (V_{th}) and off current. To overcome these limitations, there is a renewed interest in exploring new devices that uses a new current mechanism, and that does not involve carriers traveling over a potential barrier. Among various new devices Tunnel FET has been studied extensively in the past few years. TFET uses BTBT mechanism at the tunneling junction (the source channel junction) and normal drift diffusion mechanism away from the tunneling junction (Cho et al. 2011).

TFET has the potential to lower the SS beyond the 60 mV/dec limit of conventional MOSFETs along with the extremely low OFF-current. Therefore, TFET seems to be a well adaptive candidate for ultimately scaled switches and low power devices with excellent immunity to short channel effects (SCEs) (Bhuwalka et al. 2006; Born et al. 2006; Nirschl et al. 2006; Mookerjea et al. 2009). The major roadblock with the planar TFETs is its lower ON-state current (I_{ON}), which results in lower operating speed. In order to resolve this issue, numerous kinds of TFETs with various structures and materials such as double-gate, delta layer, SiGe, and PNPN structures have been proposed (Toh et al. 2007; Boucart and Ionescu 2007a, b; Toh et al. 2008; Mallik and Chattopadhyay 2011; Jhaveri et al. 2010; Cho et al. 2011; Lee et al. 2010; Noguchi et al. 2015). To enhance the I_{ON}, Silicon nanowire TFET has already been fabricated

(Gandhi et al. 2011). Further, a high-k material has been locally inserted (near the source side) in the gate dielectric to form heterogate-dielectric (HD) TFETs (Choi and Lee 2010; Mallik and Chattopadhyay 2011). The presence of high-k dielectric results into a higher band bending due to increase in surface potential (at a constant gate bias) (Jhaveri et al. 2010; Lee et al. 2012; Madan et al. 2015a, b). This higher band bending leads to reduction in tunneling barrier width, which further increases the generation rate and hence the I_{ON}.

Another major problem with TFET is ambipolarity. The ambipolarity in the device is the conduction for both high positive and high negative V_{gs} while keeping the V_{DS} only in one direction (negative for p-type devices and positive for n-type devices) (Cho et al. 2011; Conde et al. 2014; Hraziia et al. 2012; Lee et al. 2010; Shaker et al. 2015). Ambipolarity can be reduced by using a HD structure, in which the gate dielectric is split into two regions; high-k dielectric near the source side and low-k dielectric near the drain side. The higher value of dielectric improves the electrical coupling between the gate and the tunneling junction and hence, increases the tunneling rate. The DMG further helps in the improvement of ON and OFF current characteristics. Lower work function metal near the source side increases the band overlap and hence reduces the tunneling barrier width. This reduced tunneling barrier increases the tunneling probability, and the generation rate which results in higher I_{ON} and the higher value of work function near the drain side increases the tunneling barrier width and hence helps in reducing the I_{OFF}. So an optimum value of metal work function value at source and drain side should be chosen to trade-off between ON and OFF characteristics. In this work, a heterogate dielectric, Dual material gate, gate-all around (GAA) structure has been applied to TFET to enhance analog performance of the device (Madan et al. 2014).

The paper is structured as follows: Sect. 2 describes the device structure, parameters and simulation models used in this work, Sect. 3 describes the model formulation for the device Sect. 4 describes the results verification and discussions in which the effect of DMG configuration on the analog performance of the device has been studied. Finally, the conclusions are drawn in Sect. 5.

2 Device structure, parameters and simulation models

The device structural parameters used in both simulations and analytical model are fixed: channel length is 50 nm, with L_1 (20 nm) and L_2 (30 nm), gate oxide thickness (t_{ox}) = 3 nm and radius (R) = 10 nm. Further, the source (p+), drain (n+) and channel doping (p) are 10^{20}, 5×10^{18} and 10^{16} cm^{-3} respectively. To reduce ambipolarity effect source and drain are doped asymmetrically. In this analysis the analog performance is studied for the three different cases of DMG scheme to optimize the device for better analog performance and the cases are as stated below.

Case 1. $\Phi_{M1} = 4.1$ eV and $\Phi_{M2} = 4.8$ eV
Case 2. $\Phi_{M1} = 4.3$ eV and $\Phi_{M2} = 4.8$ eV
Case 3. $\Phi_{M1} = 4.4$ eV and $\Phi_{M2} = 4.8$ eV

Region 1 consists of dielectric constant $\varepsilon_1 = 21$ HfO_2 (near the source) and region 2 consists of $\varepsilon_2 = 3.9$ SiO_2 (near the drain) for all the cases. The source and drain junctions are abruptly doped for an effective band to band tunneling and the interface of high-k and SiO_2 is abrupt. The simulation device structure i.e. HD-DMG-GAA-TFET consisting of heterogate dielectric and Dual material gate is shown in Fig. 1. All simulations have been performed using the ATLAS device simulator. The most important model for TFET simulations is the band-to-band tunneling (BTBT) model. Non-local models have a more physical basis and don't depend on the electric field at the individual mesh points in the simulated device structure, but rather on band diagrams calculated along cross-sections through the device. According to BBT.NONLOCAL, the tunneling happens through the 1D slice, at the tunnel junction, where each slice and the tunnel junction are perpendicular to each other. These slices are parallel to themselves. For nonlocal BTBT model, the quantum tunneling meshing has been used at the source-channel junction. In n-TFET, the electrons tunnel through the valence band of the source to conduction band of the channel by BTBT mechanism and then the carriers drift from channel to drain. Thus, to incorporate the transport away from the tunneling junction drift diffusion model is used (Boucart and Ionescu 2007a, b). The bandgap narrowing model is used in the simulations to incorporate the effect of heavily doped source and drain regions (as tunneling current is a sturdy function of bandgap). Instead of Boltzmann statistics, Fermi–Dirac statistics have been used for the same reason (heavily source and drain doping). The models activated during simulation

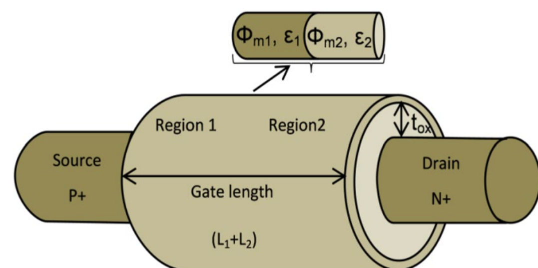

Fig. 1 Structure of n-type heterogate dielectric-dual material gate-Gate all around-tunnel FET (HD-DMG-GAA-TFET)

Table 1 Model parameters used in simulation

Physical model	Parameter	Value
Shockley–Read–Hall for carrier recombination (SRH)	TAUN0	1.0×10^{-7} s
	TAUP0	1.0×10^{-7} s
Bandgap narrowing (BGN)	BGN.E	6.92×10^{-3} V
	BGN.N	1.3×10^{17} cm^{-3}
Nonlocal band to band tunneling model (BBT. NONLOCAL)	BB.A	4.0×10^{14} V^{-2} s^{-1} cm^{-1}
	BB.B	1.9×10^{7} V cm^{-1}
	γ	2

Table 2 List of constant parameters

Parameters	Symbol	Value and unit
Electron affinity	χ_{si}	4.17 eV
Permittivity of silicon	ε_{Si}	11.8
Bandgap of silicon	E_g	1.08 eV
Temperature	T	300 K
Boltzmann constant	k_B	1.38066×10^{-23} J K^{-1}
Elementary charge	q	1.60219×10^{-19} C
Plank's constant	h	6.63×10^{-34} J s

are as follows: concentration and field dependent mobility model, Shockley–Read–Hall for carrier recombination, non-local band to band tunneling, band gap narrowing, Fermi–Dirac statistics and drift diffusion (Fukuda et al. 2013; Atlas User's Manual 2014). The parameters used in simulation along with their values are listed in Table 1.

3 Model formulation for HD-DMG-GAA-TFET

Assuming that the influence of the charge carrier and fixed carriers are uniform in the channel, it can be neglected. The parabolic potential profile along the radial direction is assumed and based on the following boundary conditions, the Poisson's equation is solved.

1. The surface potential is only z-dependent

$$\Phi_{si}(R,z) = \Phi_{si}(z) \tag{1}$$

2. The Electric field at the center of the channel is zero

$$\left.\frac{d\Phi_{si}(r,z)}{dr}\right|_{r=0} = 0 \tag{2}$$

3. Electric field at Si/SiO_2 interface is continuous

$$\left.\frac{d\Phi_{si}(r,z)}{dr}\right|_{r=R} = \frac{C_{fi}}{\varepsilon_{si}}[V_{GS} - \Phi_{si}(z) - V_{FBi}] \tag{3}$$

where; $V_{FBi} = \phi_{mi} - \phi_s$ is the flatband voltage. $i = 1$and 2 for region 1 and 2 respectively and Φ_s is the semiconductor work function.

$$\phi_s = \chi_{si} + E_g/2q + \phi_F \tag{4}$$

and $\phi_F = k_BT/q(\ln(N_{Ch}/n_i))$ is the fermi potential. Where the parameters, symbols and their values are as listed in Table 2.

C_{f1} and C_{f2} are the capacitances per unit area of the gate dielectric for region 1 and 2 respectively and are given by

$$C_{f1} = \frac{\varepsilon_1}{R\ln\left(1+\frac{t_1}{R}\right)} \text{ and } C_{f2} = \frac{\varepsilon_2}{R\ln\left(1+\frac{t_2}{R}\right)} \tag{5}$$

where $t_1 = t_2 = t_{ox}$, is the gate oxide thickness.

Solving Eqs. (1)–(5) we can obtain

$$\frac{\partial^2\Phi_{si}(z)}{\partial z^2} - k_i^2\Phi_{si}(z) = \eta_i \tag{6}$$

The general solution of (6) is

$$\Phi_{si}(z) = A_x\exp(k_iz) + A_y\exp(-k_iz) - \eta_i/k_i^2 \tag{7}$$

where $k_i^2 = \frac{2C_{fi}}{R\varepsilon_{Si}}$ and $\eta_i = \frac{qN_i}{\varepsilon_{Si}} - k_i^2[V_{gs} - V_{FBi}]$

Now using the following boundary conditions at the interface of each region, coefficients A_x and A_y can be determined.

At the source end

$$\Phi_{s1}(0) = -\frac{k_BT}{q}\ln\left(\frac{N_{source}}{n_i}\right) = V_{bi1} \tag{8a}$$

And at the drain end

$$\Phi_{s2}(L_g) = \frac{k_BT}{q}\ln\left(\frac{N_{Drain}}{n_i}\right) + V_{DS} = V_{bi2} + V_{DS} \tag{8b}$$

At the interface of region 1 and region 2,

$$\Phi_{s1}(L_1) = \Phi_{s2}(L_1) \tag{8c}$$

$$\left.\frac{d\Phi_{S1}}{dz}\right|_{z=L_1} = \left.\frac{d\Phi_{S2}}{dz}\right|_{z=L_1} \tag{8d}$$

The lateral electric field (2D) is given by

$$E_z(r,z) = -\frac{d\Phi_{si}(r,z)}{dz} \tag{9}$$

The lateral surface electric field is given by

$$E_{sz}(r,z) = A_xK_1e^{K_1z} - A_yK_2e^{K_2z} \tag{10}$$

Transverse electric field (2D)

$$E_r(r,z) = 2rP_2(z) \tag{11}$$

The tunneling generation rate determined by Eq. (13) is integrated over the volume ($\pi r^2 w_T$) to obtain the drain

current. Where w_T is the tunneling barrier width defined as the shortest distance between the valence band of the source and conduction band of the channel. It is determined from the surface potential profile, by taking the difference between the points where the surface potential falls by an amount equal to E_g/q below the surface potential and where the potential is Φ_s and is calculated as:

$$w_T = \frac{1}{K_1}\left[\ln\left[\frac{\Phi_s(z) + \frac{E_g}{q} + \frac{\eta_1}{K_1^2} + \sqrt{\left(\Phi_s(z) + \frac{E_g}{q} + \frac{\eta_1}{K_1^2}\right)^2 - 4C_1C_2}}{\Phi_s(z) + \frac{\eta_1}{K_1^2} + \sqrt{\left(\Phi_s(z) + \frac{\eta_1}{K_1^2}\right)^2 - 4C_1C_2}}\right]\right] \quad (12)$$

The tunneling generation rate can be evaluated as

$$G_{BBT} = AE^{\gamma}e^{-B/E} \quad (13)$$

where A, B and γ are the parameters dependent on the effective mass of electron and hole.

$$A = \frac{q^2\sqrt{2m_{tunnel}}}{h^2\sqrt{E_g}}, B = \frac{\pi^2 E_g^{3/2}\sqrt{m_{tunnel}/2}}{qh} \text{ and } \gamma = 2 \quad (14)$$

where m_{tunnel} is the effective mass $= 0.25m_0$ and m_0 is the rest mass of an electron. The values of A (BB.A) and B (BB.B) are listed in Table 1. The average electric field E_{avg} is calculated by integrating the total electric field E_{Tot} over the barrier width w_T as:

$$E_{Tot} = \sqrt{|E_z|^2 + |E_r|^2} \text{ and } E_{avg} = \frac{\int_{w_T} E_{Tot}dz}{w_T} \quad (15)$$

The expression for drain current (I_{ds}) is obtained as:

$$I_{ds} = q\pi R^2 w_T G(E_{avg}) \quad (16)$$

4 Result verification and discussion

Figure 2 shows the comparison of proposed device i.e. HD-DMG-GAA-TFET with the gate all around tunnel FET as reported by Ying et al. (2014). As evident from Fig. 2 that the V_{th} of GAA-TFET is high as compared to the proposed device. Moreover, the I_{ON} of proposed device is 219 times enhanced in comparison to the GAA TFET. Both the lower V_{th} and higher drain current makes the DMG scheme beneficial for VLSI/analog applications. Therefore in this work, critical analog parameters such as transconductance g_m, output conductance g_d, early voltage V_{EA}, device efficiency g_m/I_{ds}, intrinsic gain A_v, channel resistance R_{ch} and output resistance R_{out} has been studied to analyze the effect of DMG on the device performance.

The effect of gate bias and metal work function on electric field near source and drain side is shown in

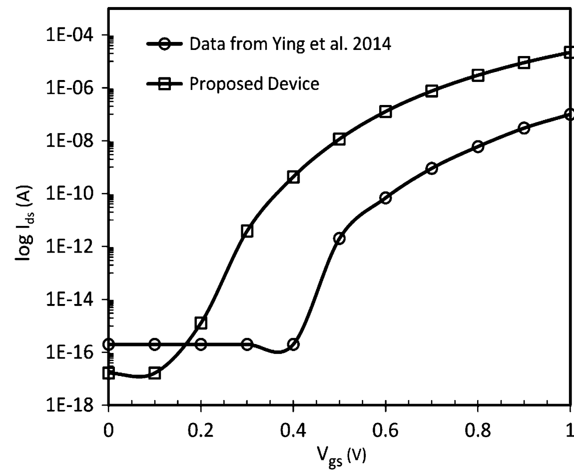

Fig. 2 Drain current–voltage comparison of proposed device HD-DMG-GAA-TFET with gate all around tunnel FET data from Ying et al. (2014)

Fig. 3a. As expected, the electric field is enhanced (near both source and drain side) with an increase in gate bias. Further, as the metal near drain side is constant; hence, the electric field near the drain is almost same for each case. With the increase in the difference in metal work function, the electric field near the source side enhances, which results in an additional lowering of barrier width and thus an increase in tunneling rate is obtained, which eventually leads to greater tunneling current and sought out the primary obstruction of TFET. Further, the SS is the amount of gate voltage required for one decade change in the drain current. In order to reduce the switching power of CMOS circuits, SS of the device should be as low as possible. Moreover, to accurately predict the circuit behavior, the V_{th} is an important parameter. The influence of metal work functions on the SS and V_{th} of the device is shown in Fig. 3b.

According to the previously reported work (Choi and Choi 2013), the I_{ON} can be enhanced by using a gate metal of lower work function near the source in comparison with metal used near drain side and to reduce the I_{OFF}, metal work function near drain should be high as compared to the metal used near the source. So in order to achieve an optimum device performance, metal near drain is kept constant ($\Phi_{M2} = 4.8$ eV) and the metal near source side is varied. As we increase the work function of metal near source side from 4.1 to 4.4 eV, the SS of the device is decreasing, but the V_{th} of the device is increasing. So the metal work function should be chosen such that the device is optimized in terms of both SS and V_{th}.

The transfer characteristics (I_{ds}–V_{gs}) are shown in Fig. 4a in both log scale and linear scale for each case. The graph shows the I_{OFF} of the order of 10^{-17} A and I_{ON} of the order

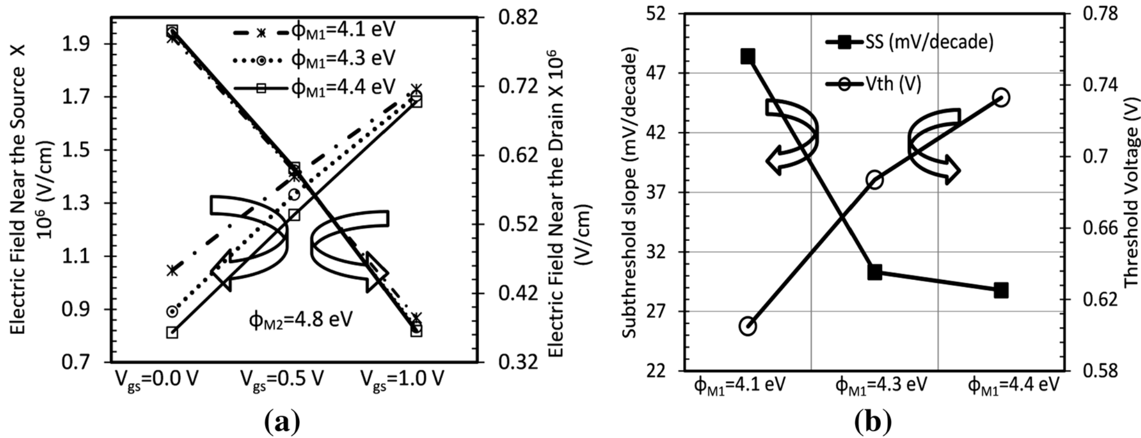

Fig. 3 **a** Electric field near source and drain side at constant $V_{ds} = 1.0$. **b** SS and V_{th} for different metal work function of HD-DMG-GAA-TFET

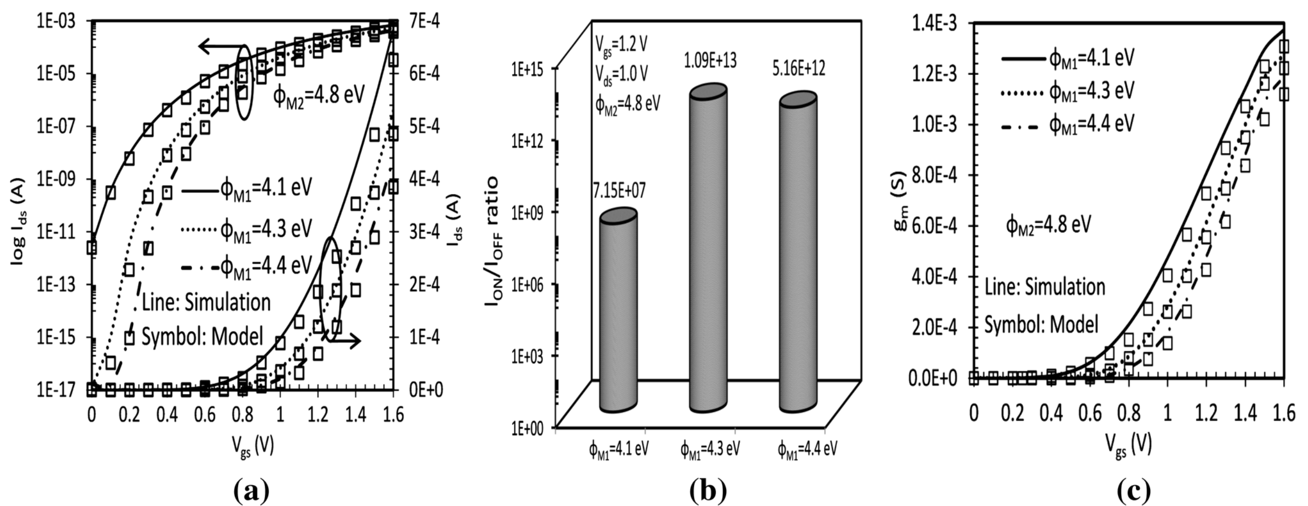

Fig. 4 **a** Transfer characteristics (I_{ds}–V_{gs}) in log and linear scale, **b** I_{ON}/I_{OFF} ratio, **c** transconductance as a function of V_{gs} for different metal work function for HD-DMG-GAA-TFET at constant $V_{ds} = 1.0$ V

of 10^{-4} A, which results in I_{OFF}/I_{ON} ratio of the order of 10^{13}. The lower value of I_{OFF} leads to a lower value of static power dissipation. Again, an increase in difference in metal work function leads to enhancement of I_{ON} by 1.5 times in case 1 as compared to case 3, but simultaneously I_{OFF} has also been increased significantly. So we need to optimize the values of metal work function to obtain an optimum value of I_{ON}/I_{OFF} ratio depending on the application. The increase in I_{ON} is the main advantage of heterogate dielectric and dual material gate. Also, it can be clearly seen from the graph that the model prediction and ATLAS device simulation are in good agreement. Figure 4b shows the variation of I_{ON}/I_{OFF} with different metal work function configurations of DMG. It is apparent from the bar graph that as work function of metal 1 increases from 4.1 to 4.3 eV the I_{ON}/I_{OFF} ratio enhances by an order of 10^5 times. Moreover for $\phi_{M1} = 4.4$ eV, the I_{ON}/I_{OFF} ratio reduces by 0.47 times w.r.t. case 2 and increases w.r.t. case 1. The reduction in I_{ON}/I_{OFF} ratio in case 3 w.r.t. case 2 is mainly attributed to enhanced I_{OFF} as shown in Fig. 4a. Transconductance g_m, which is basically the first order derivative of the drain current with respect to the gate voltage at constant drain voltage, is shown in Fig. 4c. Transconductance decides the current driving capability of the device for a given input voltage swing. It is clear from Fig. 4c that among the three cases, the higher value of transconductance is achieved for case 1. In each case, the transconductance of the device is very much higher in the case of on state as compared to off state. So for enhanced tunneling current and transconductance, the difference of metal work function should be possibly large.

The output characteristic (I_{ds}–V_{ds}) for each case is shown in Fig. 5a. The saturation mechanism of output characteristics in the case of TFET is mainly attributed to the saturation of tunneling barrier width for higher drain bias at a constant gate bias (Boucart and Ionescu 2007a, b, Madan et al. 2015a, b). It is evident from the figure that the device predicts a qualitative agreement in linear regime and also shows a good saturation in drain current for higher drain voltages. Among the three cases, the tunneling current is enhanced by 2.7 times in case 1 with respect to case 3; thus makes it suitable for analog applications. Figure 5b illustrates the effect of DMG configurations on drain/output conductance g_d. Further, in order to achieve high gain, transistors should have low output conductance for analog applications. The output conductance is increasing with an increase in drain bias and then attains maxima and further increase of drain bias reduces the drain conductance because of higher drain resistance at higher drain bias. As we reduce the metal work function difference, output conductance decreases, as is evident from Fig. 5b.

Figure 6a illustrates comparison of the device efficiency g_m/I_{ds} for each case. Device efficiency is the ability to convert dc power into ac gain performance at a particular drain bias. For each case, the highest value of g_m/I_{ds} is obtained for the weak inversion region and then a linear decrease is obtained with an increase in gate bias. Among the three cases, case 3 has higher device efficiency. For each case, the device efficiency has reached a value greater than 40 V^{-1} (the fundamental limit of conventional MOSFET) in the subthreshold region. Intrinsic gain is a valuable analog

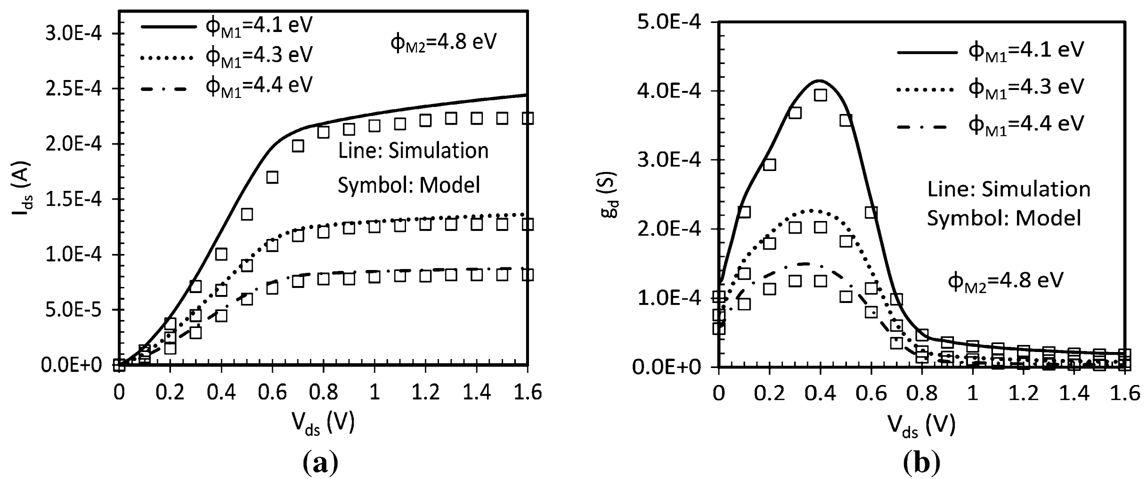

Fig. 5 **a** Output characteristics (I_{ds}–V_{ds}) and **b** output conductance for different metal work function of HD-DMG-GAA-TFET at constant $V_{gs} = 1.2$ V

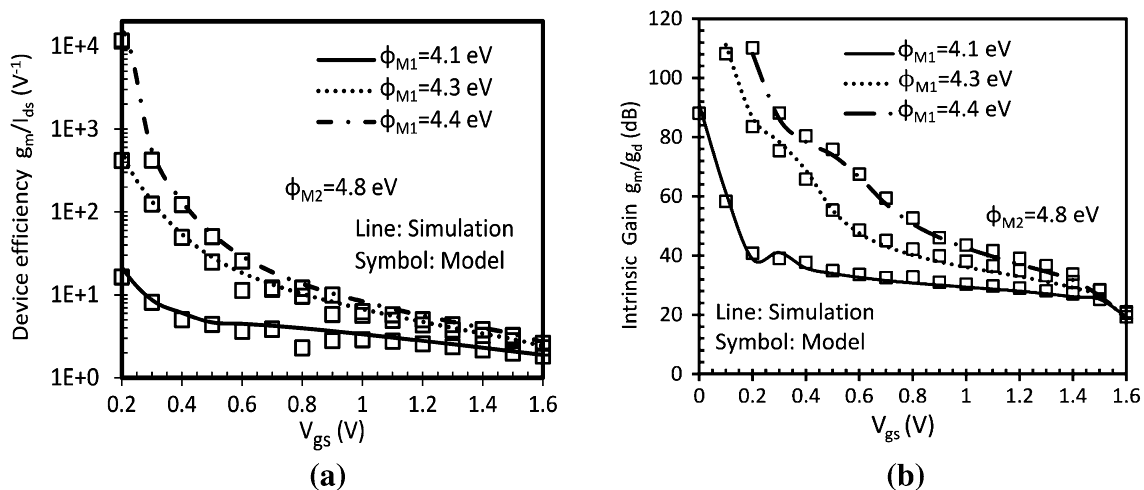

Fig. 6 **a** Device efficiency and **b** Intrinsic gain as a function of gate voltage V_{gs} for different metal work function for HD-DMG-GAA-TFET at $V_{ds} = 1.0$ V

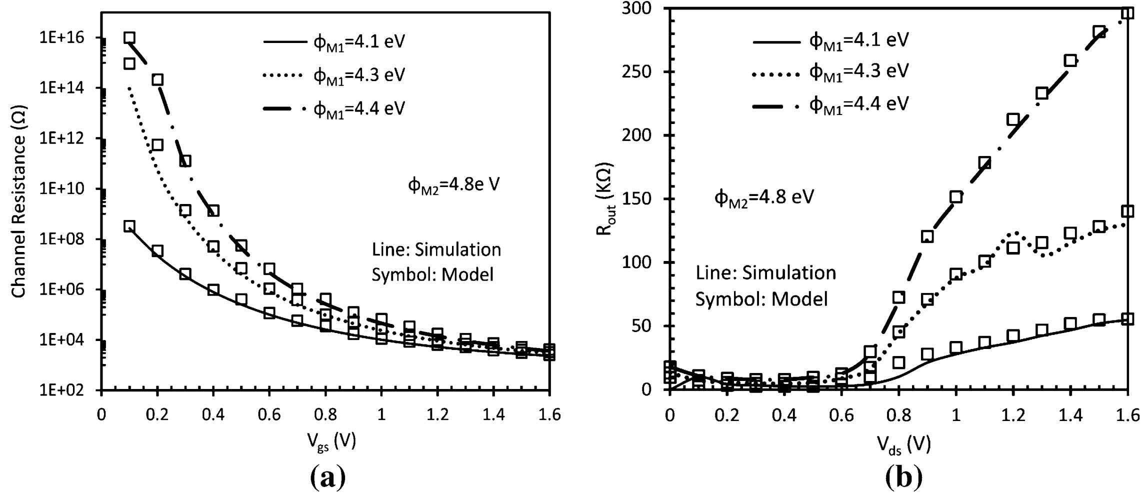

Fig. 7 **a** Channel resistance and **b** output resistance for different metal work function of HD-DMG-GAA-TFET

circuit design parameter used for designing amplifiers such as an operational transconductance amplifier (OTA). For better analog performance, an intrinsic gain of the device should be as high as possible. Comparison between of the intrinsic gain for different metal work function configuration with respect to gate bias is presented in Fig. 6b. The intrinsic voltage gain is obtained at the constant drain bias $V_{ds} = 1.0$ V, making use of the relation $A_v = g_m/g_d$. Highest intrinsic gain for a metal work function difference of 0.4 eV is attributed to the dominated decrease in output conductance in comparison with the increase in transconductance.

The influence of gate voltage and dual material gate configurations on channel resistance R_{ch} is demonstrated in Fig. 7a. For $V_{gs} = 0$ V, no band bending is there, ensuring into higher tunneling barrier width at the tunneling junction, resulting into very high R_{ch} of the order of 10^{15} Ω. As the gate bias increases, bands in the channel move downwards resulting in lowering of the tunneling barrier width as if a conductive channel is formed and thus drops the R_{ch} to a value of several KΩ's. Moreover, at lower gate bias, higher R_{ch} has been obtained for the case when metal work function difference is 0.4 eV, which shows a better OFF state characteristics for this configuration in comparison with the rest of the cases when the metal work function difference is 0.7 and 0.5 eV. Another important parameter for analog application is the output resistance or the drain resistance R_o. Drain resistance is numerically equal to the inverse of the output conductance. The variation of output resistance with the drain to source voltage is shown in Fig. 7b. It is clearly shown in the figure that in the linear region, the output resistance is very small, because of strong dependence of the drain current on drain voltage. But as the drain current saturates for the higher drain bias, R_o increases monotonically. It is evident from the figure that for the case when metal work function difference is 0.4 eV, R_o is found to be extremely high due to the better output saturation current as shown in Fig. 7b.

5 Conclusion

The present work is the detailed mathematical modeling insight for the analog performance of HD-DMG-GAA-TFET. The results obtained by simulations and analytical modeling are in good agreement. The tuning of metal work functions has been done to optimize the effect of Dual metal gate on the analog performance, which shows that both device efficiency and device gain are improved for a metal work function difference of 0.4 eV. Decrease in SS and increase in V_{th} is found on decreasing the difference between work functions of two metal used near source and drain junction. Moreover, I_{OFF}/I_{ON} ratio of the order of 10^{13} has been obtained for the same DMG configuration, making it suitable for low power applications. Enhancement of channel resistance and output resistance is obtained as we decrease the difference of the metal work functions. Moreover, it has been evaluated that SS is less than 60 mV/decade in each case, and device efficiency is more than 40 V^{-1} in the subthreshold region. This indicates that the developed model also validates with the fact that TFET overcomes the fundamental limit of MOSFET.

Acknowledgments Authors would like to thank Microelectronics Research Lab, Department of Engineering Physics Delhi Technological University to carry out this work. One of the authors (Jaya Madan) would like to thank University Grants Commission, Govt. of India, for providing the necessary financial assistance during the course of this research work.

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