CrossMark

TECHNICAL PAPER

Optimization for etching shallow ridge and trench profiles on silicon based on continuous etching process in ICPRIE system

Lei Wan[1] · Xuan Li[1] · Ning Zhu[1] · Rui-ying Zhang[2] · Ting Mei[3]

Abstract In order to directly characterize sidewall roughnesses of shallow microstructures with etching depth less than 10 µm using a conventional atomic force microscope tip, an easy bevel-cut sample technique was developed. With help of the proposed measurement technique, the sidewall verticalities and roughnesses between trench and ridge profiles were compared and optimized using an L9 orthogonal array experiment based on a simple continuous dry-etching process. Additionally, due to the influence of loading effect, the contribution proportions of four control factors on etching quality characteristics were evaluated. As some improved measurement results, optimized root mean square sidewall roughnesses of 3.61 and 4.7 nm were obtained for ridge and trench structures, respectively, with depth greater than 4 µm and the sidewall verticality of $90 \pm 1°$.

✉ Ting Mei
  ting.mei@ieee.org

1 Laboratory of Nanophotonic Functional Materials and Devices, Institute of Optoelectronic Material and Technology, South China Normal University, Guangzhou 510631, China

2 Key Labs of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Science, Suzhou 215123, China

3 Key Laboratory of Space Applied Physics and Chemistry, Ministry of Education and Shanxi Key Laboratory of Optical Information Technology, School of Science, Northwestern Polytechnical University, Xi'an 710072, China

1 Introduction

Recently fabrication of patterns with high-accuracy etching profiles and different aspect ratios on silicon wafers has drawn extensive attention in a number of applications, such as MEMS (Mouro et al. 2013; Miwa et al. 2013), biomedical (Miles et al. 2013), solar cells (He et al. 2012; Jeong et al. 2012), silicon-on-insulator (SOI) rib waveguides (Qiu et al. 2014; Gao et al. 2005), polymer optical waveguides (Yoon et al. 2004; Choi et al. 2003; Choi 2004), polymer-based waveguide devices (Jang et al. 2012), etc. The Bosch process, which consists of alternating etching and passivation steps, has an irreplaceable role in dry etching of high aspect ratio (HAR) vertical structures on silicon. However, the continuous etching process may be an alternative approach, especially more suitable for dry etching of low aspect ratio (LAR) vertical structures with smooth sidewalls. It is known that the ridge and the trench are basic structures for these application fields, whereas ideal shallow silicon microstructures with ridge and trench profiles are always expected in photonic applications. Excellent sidewall quality is essential to guarantee device performance, particularly, the optical scattering loss, and thus process optimization and characterization for sidewall quality are of great importance.

Works for optimizing the sidewall quality of shallow silicon microstructures have been reported by several research groups. A continuous silicon etching process with parameter ramping in inductively coupled plasma reactive ion etching (ICPRIE) system was used by Solehmainen et al. (2005) to obtain smoother SOI rib waveguide sidewall profiles than that done by the conventional Bosch process adopted by Wang et al. (2005). A root mean square (RMS) sidewall roughness of 10.2 nm in 2×2 µm^2 scanning area was reported by Gao et al. (2006) using a continuous

 Springer

etching process with constant parameters. In order to improve sidewall smoothness, Gao et al. (2014) further proposed a modified three-step Bosch process, which nearly eliminated the mouse-bite sidewall morphology and reduced the RMS sidewall roughness down to 8.02 nm in $4 \times 8\ \mu m^2$ area.

In this paper, we investigated the optimization of a simple single-step continuous etching process for efficient fabrication of shallow silicon microstructures, i.e. with etching depth less than ~10 μm, on target for improved RMS sidewall roughness and excellent sidewall verticality. With help of an easy measurement technique developed for characterizing the sidewall roughness of shallow microstructures, i.e. with depth <10 μm, the investigation of an orthogonal array experiment based on continuous etching process was conducted to optimize etching profiles. Owing to the difference of exposed silicon areas under mask patterns for making the ridge and trench structures, corresponding differences exist in their etching rates and the sidewall qualities. With analysis of variance (ANOVA) and comparison of their results, the effects of control factors on their etching profiles were understood. As a proof for optimal experiment, shallow silicon microstructures with excellent vertical and smooth sidewalls were successfully fabricated.

2 Experiment

The continuous silicon etching process based on ICPRIE system was chosen to optimize etching profiles, which is a process that the etching gas SF_6/O_2 and the passivation gas C_4F_8 are spontaneously provided to participate in anisotropic etching in the low vacuum chamber. Therefore, the sidewall profile is mainly determined by chemical equilibrium reaction between the etching and passivation process. When the rate of isotropic etching by SF_6 is slightly greater than that of passivation by C_4F_8, an undercut profile in the bottom of a structure will tend to appear. Particularly, as the rate of isotropic etching by SF_6 is predominant, this undercut profile will be evolved into overcut at the top of structure. Here in order to quantitatively characterize roughness of sidewall profile, a simple measurement technique was firstly proposed as following.

The roughness of a vertical sidewall with large depth, e.g. greater than 10 μm, can be easily measured by directly scanning the sidewall using a conventional scanning tip in atomic force microscope (AFM) on a sidecut sample. However, this can hardly be done for a shallow sidewall because it is difficult to position a conventional AFM tip on the tiny area. Therefore, a special bevel-cut technique was developed to allow the measurement done by a conventional AFM tip (Vecco D3100). The 250 μm-width line features, i.e. ridge and groove, were fabricated on $2 \times 2\ cm^2$ silicon substrates, and the substrates were beveled along plane A as illustrated in Fig. 1a, b using a dicing saw (Disco DAD340). After the location of tip landing was confirmed by observation under optical microscope as displayed in Fig. 1c, d, the AFM tip could be slowly moved into sidewall region. The preferred region was in the vicinity of the intersection between the sidewall and plane A. Here considering the intersection angle $\psi \sim 1.43°$ and 5 μm dynamic range of the AFM tip, a scanning range of approximately 200 μm

Fig. 1 The schematics of sample preparation with bevel cut for **a** the ridge structure and **b** the trench structure; the optical microscopic images at **c** top view and **d** cross-sectional view for the ridge structure
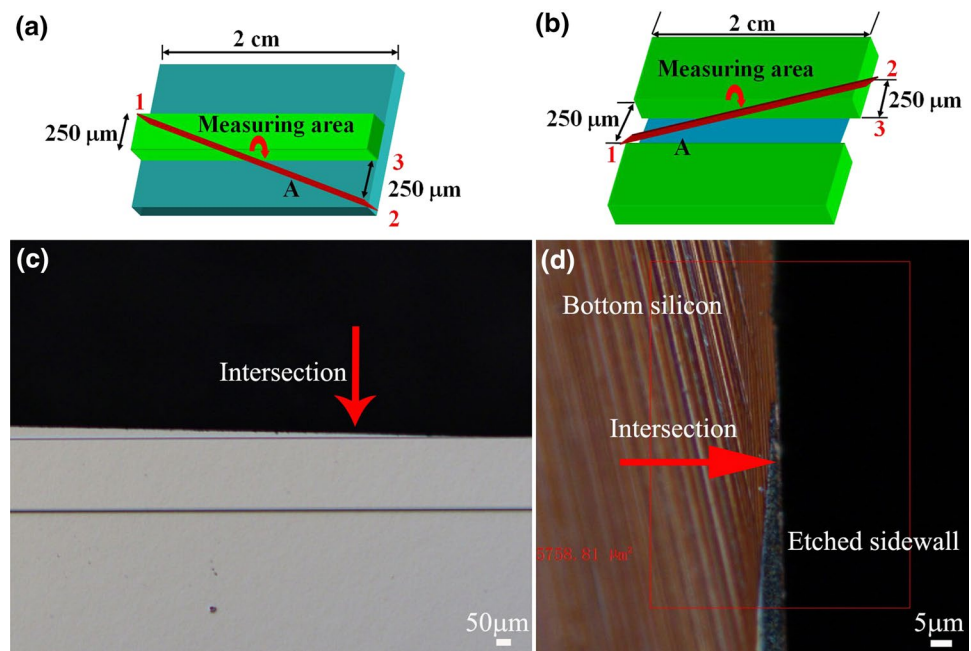
could be provided to avoid remnants from obstructing the scanning tip.

Shallow silicon profile etching is influenced by many factors including the inductively-coupled plasma (ICP) source power, the DC bias power, the etching gas (SF_6) flow rate, the passivation gas (C_4F_8) flow rate, the pressure, the bottom electrode platen temperature, and the oxygen (O_2) flow rate, etc. Based on precursory work, the ICP source power, the temperature of the bottom electrode platen, and the SF_6 flow rate were set as 600 W, 0 °C, and 130 sccm [sccm denotes cubic centimeter per minute at STP (standard temperature and pressure)], respectively, and the other parameters were taken as control factors to optimize the continuous etching process for smooth and vertical sidewall profiles. Therefore, considering the excessive variable and experiment cost, an efficient orthogonal array experiment included 9 recipes with 4-factor and 3-level was designed, which was denoted as L_9 (3^4). The arrangements of factor levels are shown in Tables 1 and 2.

The quality characteristics of etching profiles were evaluated by the average etching rate V (μm/min), the sidewall verticality θ (°) and the average sidewall roughness R (nm). V was derived by measuring an etching profile of a 5 μm-width pattern on the SEM image. The distance of adjacent patterns was 1 mm. θ was defined as the angle between the sidewall and the etched bottom, which

was also acquired from the SEM image. R was obtained by scanning a 2×2 μm^2 area near the bottom of the etched sidewalls using the above mentioned measurement technique. A third-order fit function was adopted to calibrate the base plane for calculation of the roughness.

For etching of ridge microstructures, the positive AZ5214 resist was chosen as the mask material. Firstly, the 2-in. silicon wafers were spin-coated with a 1.4 μm-thick resist layer, soft baked for 90 s on a hot plate at 95 °C, exposed for 6.8 s on a standard mask aligner (Karl Suss MA6), and then developed for 45 s in an immersion process using developer (3038). After that, the patterns for ridge microstructures were successfully transferred onto the resist.

For etching of trench microstructures, the negative AZ5214 resist was taken as the etching mask. Prior to the pattern formation, the identical resist pretreatment processes were adopted to fabricate resist films on wafers. Then a pre-exposure process was taken for 3.5 s on the mask aligner with an energy intensity of 9.3 mJ/cm^2, followed by a baking process for 90 s on a hot plate at 110 °C. The inversion of resist patterns was performed by blank exposure for 40 s under the Flood-E mode. The trench patterns were obtained after development for 45 s.

The two types of samples were adhered on 6-inch wafers using vacuum grease to ensure good heat conduction between samples and the bottom electrode platen for dry etching in ICPRIE system (STS Multiplex ASE-HRM).

3 Results and discussion

The statistical results from the orthogonal experiment shown in Fig. 2a, b indicated that the etching rates of trench structures were greater than those of ridge structures under the same process conditions, which is attributed to

Table 1 Level design for the factors

Code	Factors assigned	Levels		
		1	2	3
A	Pressure (mTorr)	10	20	30
B	C_4F_8 flow rate (sccm)	60	90	120
C	Bias power (W)	20	40	60
D	O_2 flow rate (sccm)	0	13	26

Table 2 Orthogonal array (L9) and signal-to-noise ratios of experiments

Test no.	Factor assigned				Etching rate (μm/min)		Sidewall verticality (°)		Sidewall roughness (nm)	
	A	B	C	D	V_R	V_T	θ_R	θ_T	R_R	R_T
1	1	1	1	1	1.22	1.23	108	103	32.8	25.6
2	1	2	2	2	0.92	0.93	87.7	87	23.1	16
3	1	3	3	3	0.72	0.74	88.3	88.2	6.18	12.6
4	2	1	2	3	1.48	1.58	120	112	16.7	23.3
5	2	2	3	1	1.05	1.19	86.4	86.6	9.5	25.1
6	2	3	1	2	0.66	0.75	87.7	87.5	3.24	6.25
7	3	1	3	2	1.54	1.87	99.7	106	20.6	24.2
8	3	2	1	3	0.98	1.25	88	87.7	4.3	16.4
9	3	3	2	1	0.73	0.96	89.3	88.3	2.4	5.3

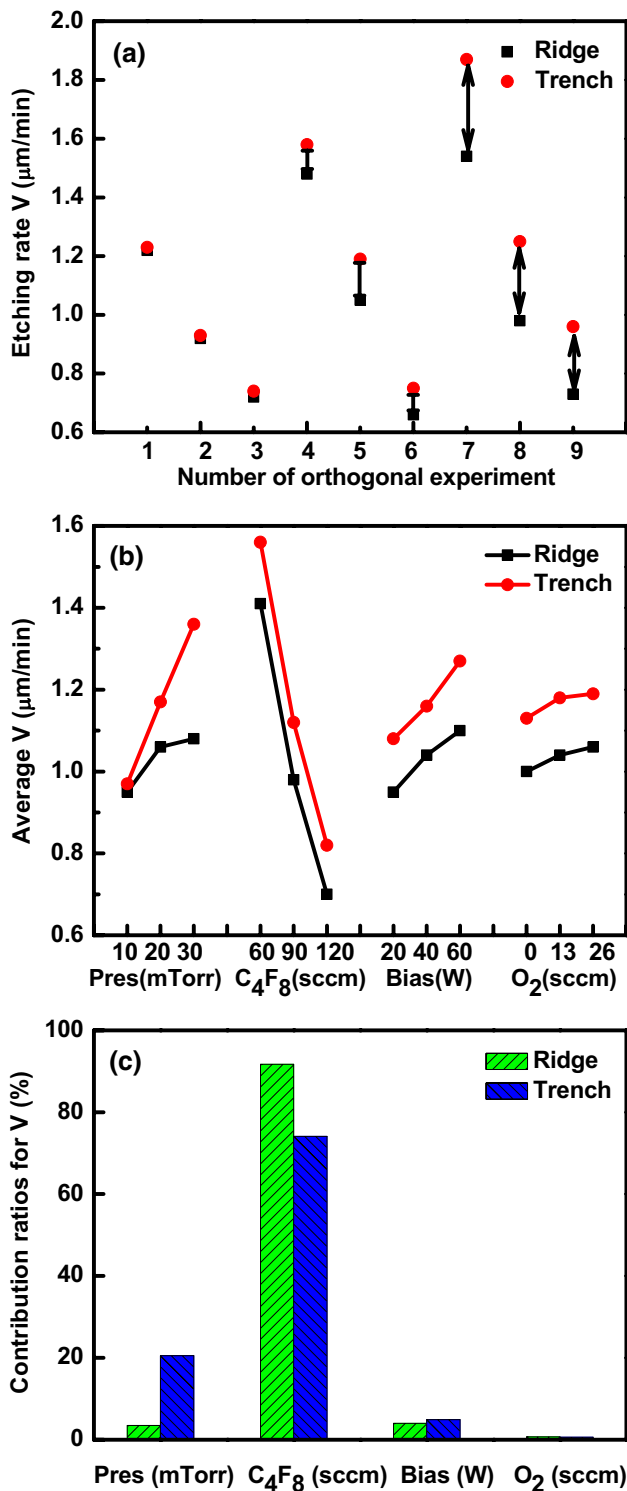Subscript "R" represents ridge profile, and "T" represents trench profile

Fig. 2 a The distributions of etching rate for different etching recipes, **b** the effects of factors levels on average etching rate, and **c** the contribution ratios of factors to etching rate
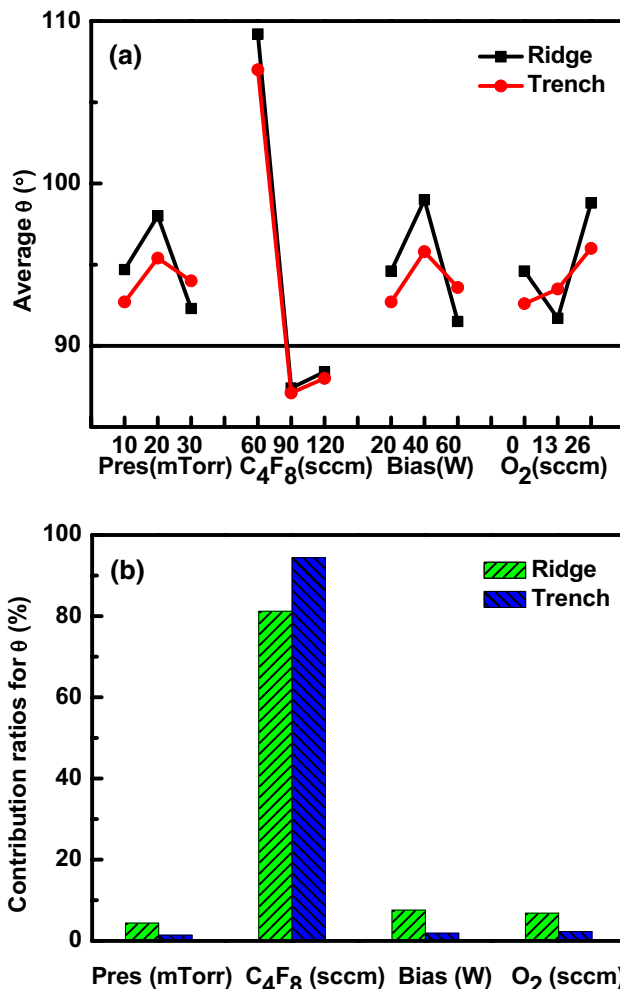

Fig. 3 a The effects of factor levels on average sidewall verticality, and **b** the contribution ratios of factors to sidewall verticality

significant loading effect under high pressure condition, which is in good consistence with Hedlund et al. (1994). For etching the ridge structures with large loading areas, increasing pressure led to depletion of active species, thus limiting the increase of etching rate. Therefore, the pressure was a contributing factor more influential on the etching rate of trench structures than that of ridge structures, whereas the situation of the C_4F_8 flow rate was just opposite as shown in Fig. 2c.

The effects of factor levels on average sidewall verticality and the contribution ratio are shown in Fig. 3, indicating that the most influential factor was the C_4F_8 flow rate, which protected sidewalls from lateral etching by F-radicals. Figure 4 illustrated overcut and undercut profiles for low and high flow rates of C_4F_8, respectively, when the SF_6 flow rate was fixed at 130 sccm. For a high flow rate ratio of SF_6/C_4F_8, excess etching led to the overcut profile due to the nature of isotropic chemical

the loading effect due to the differences of exposed silicon areas and the average lifetime of active species (Mogab 1977; Tian et al. 2000). The experiment showed more
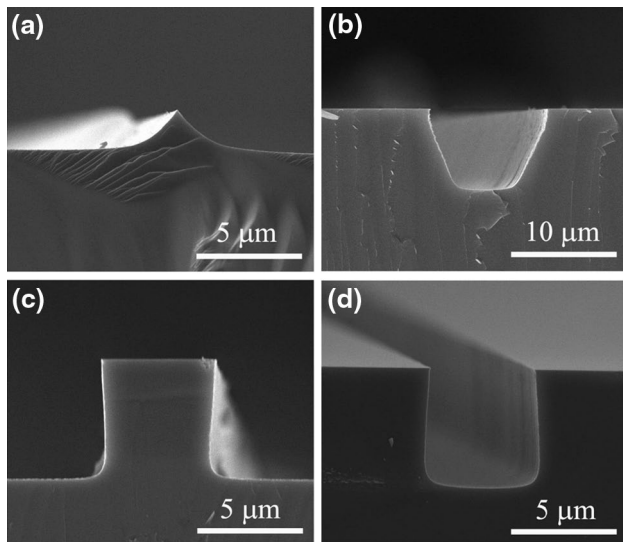
Fig. 4 The SEM images of **a** a ridge structure with overcut profile from test no. 4 ($SF_6/C_4F_8 = 2.2$), **b** a trench structure with overcut profile from test no. 4 ($SF_6/C_4F_8 = 2.2$), **c** a ridge structure with undercut profile from test no. 8 ($SF_6/C_4F_8 = 1.4$), and **d** a trench structure with undercut profile from test no. 9 ($SF_6/C_4F_8 = 1.1$)

reaction (Li et al. 2008). For a low flow rate ratio of SF_6/C_4F_8, a passivation layer formed on the sidewall prevented the sidewall from lateral etching, which resulted in the formation of slight undercut profile. The etching anisotropy increased with increasing C_4F_8 flow rate (Shul and Pearton 2000). The influence of the C_4F_8 flow rate was greater on the sidewall verticality of the trench structure than that of the ridge structure due to the loading effect, but the angular difference between these two types of structures was less than 1° for cases in absence of excess etching.

As illustrated in Fig. 5b, the C_4F_8 flow rate was the most significant factor for the sidewall roughness of both types of structures. The sidewall roughness decreased with increasing C_4F_8 flow rate as shown in Fig. 5a, because a high ratio of SF_6/C_4F_8 led to nonuniform passivation layer containing large-size cavities due to incomplete deposition of passivation layer in sidewall areas (Richter et al. 2001). A low ratio of SF_6/C_4F_8 benefited complete deposition of passivation layer and smooth sidewall morphology. Since the local distribution of passivation layer was relatively flatter in the large opening of ridge structures than that in the small opening of trench structures, the sidewall roughness of ridge structures was smaller as well. As shown in Fig. 5a, such loading effect became more significant as the pressure was raised from 10 to 20 mTorr, when active species was getting depleted. Meanwhile, the addition of oxygen plasma from 13 to 26 sccm increased the density of passivation gas for the ridge structures due to the prominent effect of oxide deposition layer.
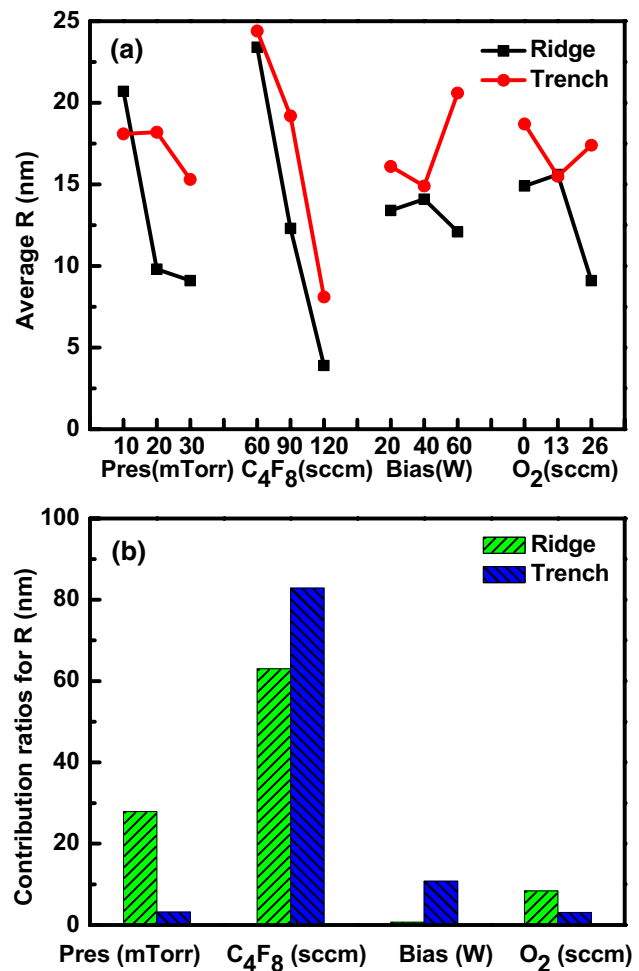

Fig. 5 **a** The effects of factor levels on average sidewall roughness, and **b** the contribution ratios of factors to sidewall roughness

The relatively strong sensitivity of the sidewall roughness of ridge structures to the pressure was also shown in Fig. 5b. However in contrast, the sidewall roughness of trench structures was relatively sensitive to the bias power. The sidewall morphology was more readily affected by ion sputtering in structures with small opening. In the trench etching with small opening, the intensive ion bombardment was induced by large bias power as the bias power increased from 40 to 60 W, and it was observed that the over-bombardment deteriorated the sidewall morphology.

In order to verify the results of the orthogonal array experiment, the shallow silicon microstructures were fabricated by optimized process settings. Considering the trade-off between the sidewall quality and the etching rate, the bias power 20 W and the pressure 30 mTorr were preferentially chosen as optimal parameters. At the C_4F_8 flow rate, 130 sccm, the ridge structure was etched down for 4.18 µm with an etching rate of 0.52 µm/min, a sidewall verticality of 90.6° and a RMS sidewall roughness of 3.61 nm

Fig. 6 The SEM images at cross-sectional view and the AFM images of sidewall morphology for the optimized ridge (**a**, **b**) and trench (**c**, **d**)
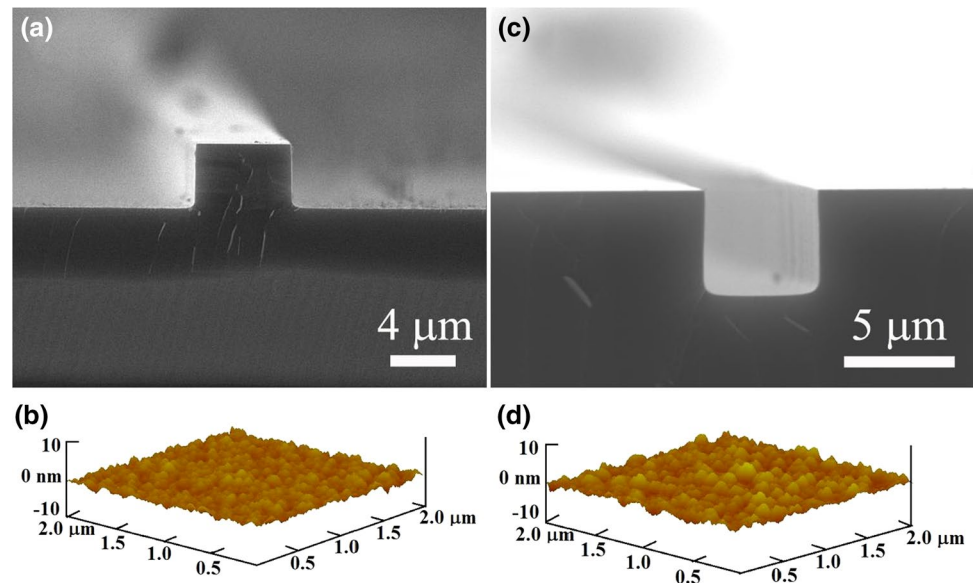
obtained in $2 \times 2 \ \mu m^2$ measurement area. At flow rates of C_4F_8, 140 sccm and O_2, 13 sccm, the trench structure was etched down for 4.8 μm with an etching rate of 0.6 μm/min, a sidewall verticality of 89.4° and a RMS sidewall roughness of 4.7 nm. The SEM and AFM images of these samples were shown in Fig. 6.

4 Conclusion

The orthogonal array experiment was conducted to optimize the single-step continuous dry-etching process of shallow silicon microstructures for the etching rate, the sidewall verticality and the sidewall roughness. The bevel-cut sample technique was developed to enable sidewall roughness measurement by direct scanning using conventional AFM tips. The etching rate was faster for the trench than the ridge due to the loading effect which became more significant under higher pressure. Likewise, the sidewall roughness was larger for the trench than that for the ridge under the same process parameter settings. The sidewall verticality difference between them was less than 1° for the recipes without excess etching. The C_4F_8 flow rate was the most prominent control factor for all three quality factors. The pressure was more influential for trench etching than ridge etching on the etching rate but opposite on the sidewall roughness. The bias power was more influential for trench etching than ridge etching on the sidewall roughness. After optimization being done, the RMS sidewall roughnesses of 3.61 and 4.7 nm and the sidewall verticalities of 90.6° and 89.4° were obtained for the ridge and trench structures with depth greater than 4 μm, respectively. The optimized continuous etching process has great advantage for fabrication of fine silicon patterns with shallow profiles.

References

Choi CG (2004) Fabrication of optical waveguides in thermosetting polymers using hot embossing. J Micromech Microeng 14:945–949

Choi CG, Han SP, Kim BC, Ahn SH, Jeong MY (2003) Fabrication of large-core 1 × 16 optical power splitters in polymers using hot-embossing process. IEEE Photon Technol Lett 15:825–827

Gao F, Wang Y, Gao G, Jia X, Zhang F (2005) Improvement of sidewall surface roughness in silicon-on-insulator rib waveguides. Appl Phys B 81:691–694

Gao F, Wang Y, Cao G, Jia X, Zhang F (2006) Reduction of sidewall roughness in silicon-on-insulator rib waveguides. Appl Surf Sci 252:5071–5075

Gao F, Ylinen S, Kainlauri M, Kapulainen M (2014) Smooth silicon sidewall etching for waveguide structures using a modified Bosch process. J Micro/Nanolith MEMS MOEMS 13:013010-1–013010-5

He H, Chen C, Liu S (2012) Microstructured silicon with two impurity bands for solar cells. J Appl Phys 111:043102-1–043102-7

Hedlund C, Blom HO, Berg S (1994) Microloading effect in reactive ion etching. J Vac Sci Technol A 12:1962–1965

Jang KS, Kim ES, Kim CS, Jeong MY (2012) Design and fabrication of an imprinted wavelength-independent coupler. Opt Eng 51:085003-1–085003-6

Jeong S, Wang S, Cui Y (2012) Nanoscale photon management in silicon solar cells. J Vac Sci Technol A 30:060801-1–06080111

Li R, Lamy Y, Besling WFA, Roozeboom F, Sarro PM (2008) Continuous deep reactive ion etching of tapered via holes

for three-dimensional integration. J Micromech Microeng 18:12503-1–12503-8

Miles RN, Degertekin L, Cui W, Su Q, Homentcovschi D, Fredrick B (2013) A biologically inspired silicon differential microphone with active Q control and optical sensing. In: Proceedings of meetings on Acousics'13, Montreal, pp 1–8

Miwa K, Nishimori Y, Ueki S, Sugiyama M, Kubota T, Samukawa S (2013) Low-damage silicon etching using a neutral beam. J Vac Sci Technol B 31:051207-1–051207-6

Mogab CJ (1977) The loading effect in plasma etching. J Electrochem Soc 124:1262–1268

Mouro J, Gualdino A, Chu V, Conde JP (2013) Microstructure factor and mechanical and electronic properties of hydrogenated amorphous and nanocrystalline silicon thin-films for microelectromechanical systems applications. J Appl Phys 114:184905-1–18490512

Qiu C, Sheng Z, Li H, Liu W, Li L, Pang A, Wu A, Wang X (2014) Farication, characterization and loss analysis of silicon nanowaveguides. J Lightwave Technol 32:2303–2307

Richter K, Orfert M, Schuhrer H (2001) Variation of etch profile and surface properties during patterning of silicon substrates. Surf Coat Tech 142–144:797–802

Shul RJ, Pearton SJ (2000) Handbook of advanced plasma processing techniques. Springer, New York

Solehmainen K, Aalto T, Dekker J, Kapulainen M, Harjanne M, Kukli K, Heimala P, Kolari K, Leskelä M (2005) Dry-etched silicon-on-insulator waveguides with low propagation and fiber-coupling losses. J Lightwave Technol 23:3875–3879

Tian C, Weigold JW, Pang SW (2000) Comparison of Cl_2 and F-based dry etching for high aspect ratio Si microstructures etched with an inductively coupled plasma source. J Vac Sci Technol B 18:1890–1896

Wang YJ, Lin ZL, Zhang CS, Gao F, Zhang F (2005) Integrated SOI rib waveguide using inductively coupled plasma reactive ion etching. IEEE J Sel Top Quant 11:254–259

Yoon KB, Choi CG, Han SP (2004) Fabrication of Multimode Polymeric Waveguides by Hot Embossing Lithography. Jpn J Appl Phys 43:3450–3451