

# Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour

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**Abstract** In this paper, a novel device structure called transparent gate recessed channel MOSFET (TGRC-MOSFET) is proposed to alleviate the hot carrier effects for the advanced nanometer process. TGRC-MOSFET involving a recessed channel and incorporates indium tin oxide as a transparent gate. TCAD analysis shows that the performance of TGRC-MOSFET surpasses conventional recessed channel (CRC)-MOSFET in terms of high  $I_{ON}/I_{OFF}$  ratio and better carrier transport efficiency in comparison to CRC-MOSFET. This simulation divulges the reduction in hot-carrier-effects metrics like electron velocity, electron temperature, potential, and electron mobility. Furthermore, the effect of gate length is observed on the analog behavior of TGRC-MOSFET. All the simulations have been done using DEVEDIT-3D and ATLAS device simulator. The work proposes the novel design for reduced hot carrier and low power switching applications.

## 1 Introduction

Hasten in semiconductor manufacturing techniques and more and more demand for high speed and more complicated integrated circuits (ICs) have driven the associated

metal oxide semiconductor field effect transistor (MOSFET) sizes close to their physical limits. On the other hand, it is difficult to scale-down the supply voltage used to perform these ICs consistently due to compatibility problem with earlier generation circuits, power, noise margin and delay requirements, and not scaling of threshold voltage and subthreshold slope (Torabi et al. 2013; Gautam et al. 2013). While the successive increase in internal electric fields in aggressively scaled MOSFETs comes with the additional ameliorate of increased carrier velocities, and hence increased switching speed, it also presents higher reliability complications for the long period of operation of these devices.

As devices are scaled down, the benefits of higher electric fields saturate while the associated reliability problems get worse. The presence of large electric fields in MOSFETs implies the presence of high energy carriers, referred as “hot-carriers”, in such devices (Arora 2007). The presence of this kind of mobile carriers in the oxide creates some physical damages which may change device characteristics for a long time. The aggregation of damage can ultimately be the reason of circuit failure. The aggregation damage of the hot carrier results in deterioration of device behavior (Orouji and Kumar 2005; Pan et al. 1994; Krieger et al. 2001). The need of superior performance of ICs has led to the scaling of MOSFETs down to 30 nm and below.

The hot-carrier dilapidation becomes a stringent limitation to the reliability of 100-nm devices and VLSI packing density (Chaujar et al. 2008a, b). Under the influence of high lateral fields in short-channel MOSFETs, carriers in the channel and pinch-off regions of the transistor reach non-equilibrium energy distributions. The generation of these hot-carriers is the primary source of several reliability problems. Hot-carriers can acquire sufficient energy to

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surmount the energy barrier at the Si–SiO<sub>2</sub> interface or tunnel into the oxide.

From the last several decades, the hot carrier reliability performance in a MOS device has been studied since MOS device is scaled and suffered from hot carrier effect which also pervert analog circuit desideratum. When we scaled the device, the ameliorates of higher electric fields impregnate while associated reliability problems get worse. When electric field will be large in MOSFETs, then carrier will have high energy and these carriers are hot carriers. To abate these hot-carrier effects in CRC-MOSFET, instead of metallic gate we are using indium tin oxide (ITO). ITO (tin-doped indium oxide) is a solid solution of indium oxide (In<sub>2</sub>O<sub>3</sub>) and tin oxide (SnO<sub>2</sub>). It is transparent and colorless in thin layers. ITO is one of the most widely used transparent conducting oxides. By using ITO, we improve  $I_{ON}$  which causes the decrease in device power consumption (Salehi and Gholizadeh 2011). The In<sub>2</sub>O<sub>3</sub> phase itself contributes free electron for electrical conductivity (Pammi et al. 2011). When tin (Sn) is diffused, then some of the oxygen vacancies may be created by SnO<sub>2</sub> which creates free electrons to enhance the concentration of carriers and hence increase conductivity and decrease the resistivity with temperature.

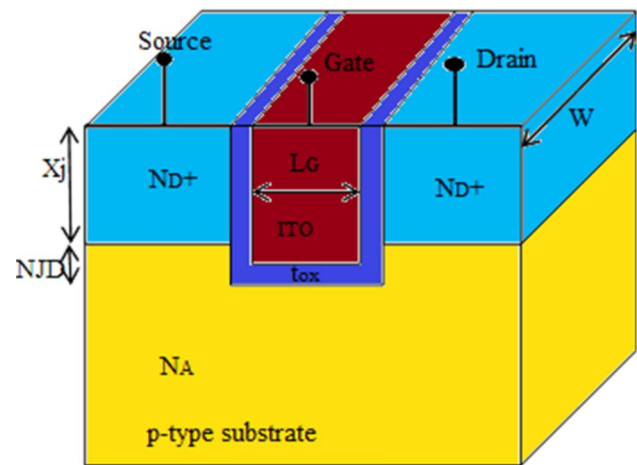
## 2 Device structure and its parameters

The simulation device structure i.e. TGRC-MOSFET consists of gate which is made by transparent conducting material ITO as shown in Fig. 1. The total gate length is 30 nm and thickness of oxide is 2.0 nm. In this case, substrate doping is p-type with concentration of  $1 \times 10^{16} \text{ cm}^{-3}$ ; source and drain are n-type with uniform doping profiles is  $1 \times 10^{19} \text{ cm}^{-3}$ .

All simulations have been performed using ATLAS and DEVEDIT 3D device simulator. In gate electrode, we are replacing metal gate by transparent conducting material ITO, but source electrode and drain electrodes are remain metal. Bias voltage  $V_{gs} = 0.7 \text{ V}$  and  $V_{ds} = 0.5 \text{ V}$  are applied in all the results except  $V_{ds} = 0.8 \text{ V}$  given when calculating DIBL. Design parameters of CRC-MOSFET and TGRC-MOSFET are given in Table 1.

## 3 Computer simulation results of transparent gate recessed channel MOSFET

The present analysis is carried out for a channel length,  $L_G = 30 \text{ nm}$ , uniformly doped source/drain,  $N_D$  with doping density of  $1 \times 10^{19} \text{ cm}^{-3}$ , p-type substrate doping,  $N_A$  with a doping density of  $1 \times 10^{16} \text{ cm}^{-3}$ , SiO<sub>2</sub> thickness,  $t_{ox} = 2.0 \text{ nm}$ . The gate work function ( $\Phi_{ITO}$ ) is 4.7 eV.



**Fig. 1** Simulated device: TGRC-MOSFET

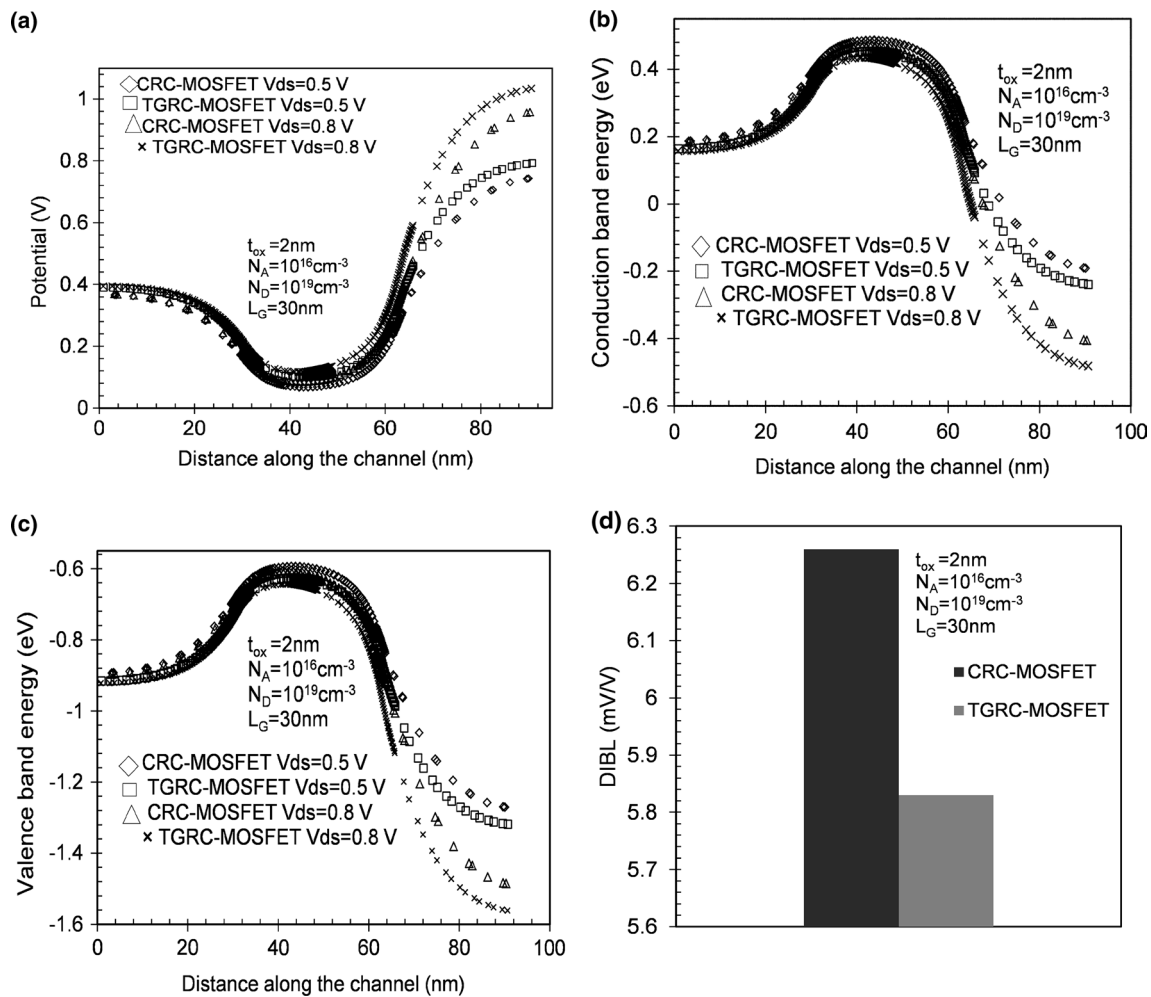
**Table 1** Design parameters of CRC-MOSFET and TRGC-MOSFET device designs

Channel length ( $L_G$ )	30 nm
Device width	200 nm
Groove depth	38 nm
Source/drain junction depth	30 nm
Negative junction depth (NJD)	10 nm
Substrate doping ( $N_A$ )	$1 \times 10^{16} \text{ cm}^{-3}$
Source/drain doping ( $N_D^+$ )	$1 \times 10^{19} \text{ cm}^{-3}$
Physical oxide thickness ( $t_{ox}$ )	2 nm
Permittivity of SiO <sub>2</sub>	$\epsilon_{ox} = 3.9$
Gate to source voltage ( $V_{gs}$ )	0.7 V
Drain to source voltage ( $V_{ds}$ )	0.5 V
Work function for TGRC-MOSFET ( $\Phi_{ITO}$ )	4.7 eV
Work function for CRC-MOSFET ( $\Phi_M$ )	4.1 eV

### 3.1 Surface potential, conduction band energy, valence band energy and DIBL

Figure 2a shows the variation of surface potential along the channel for CRC-MOSFET and TGRC-MOSFET at two different drain voltages  $V_{ds} = 0.5 \text{ V}$  and  $0.8 \text{ V}$ .

Figure 2b and c shows the conduction band and valence band energy profiles along the channel length for CRC-MOSFET and TGRC-MOSFET. The lowering of barrier potential at source side indicates that the DIBL effect is less observed in this device, as it is evident from Fig. 2d (Shee et al. 2014; AI-Mistarihi et al. 2013). The improvement in DIBL effect is more in case TGRC-MOSFET, as it incorporates the non-stationary effects such as velocity overshoots. The improvement in DIBL effect is due to the step in conduction band energy profile in the channel



**Fig. 2** **a** Surface potential as a function of position along the channel for CRC-MOSFET and TGRC-MOSFET at  $V_{ds} = 0.5$  V and  $V_{ds} = 0.8$  V. **b** Conduction band energy as a function of position along the channel for CRC-MOSFET and TGRC-MOSFET at

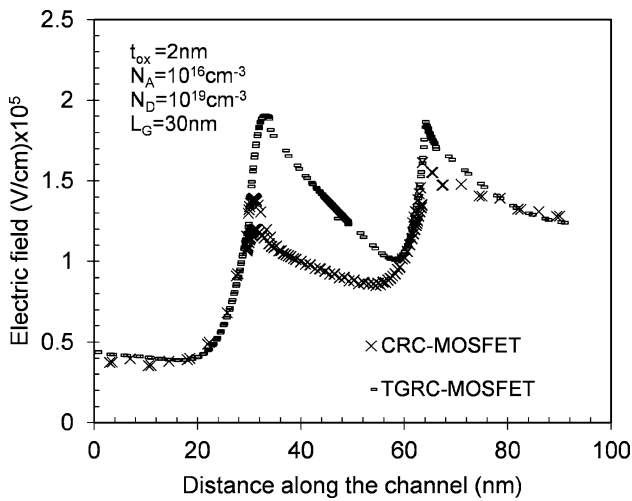
$V_{ds} = 0.5$  V and  $V_{ds} = 0.8$  V. **c** Valence band energy as a function of position along the channel for CRC-MOSFET and TGRC-MOSFET at  $V_{ds} = 0.5$  V and  $V_{ds} = 0.8$  V. **d** DIBL for CRC-MOSFET and TGRC-MOSFET at  $V_{ds} = 0.5$  V and  $V_{ds} = 0.8$  V

region, which is resulting from transparent gate. DIBL is more pronounced in conventional MOSFET, which is calculated from the difference of conduction band energy between  $V_{ds}$  of 0.8 and 0.5 V. Variation of the bending energy gap due to the threshold voltage variation ( $\Delta V_{th}$ ) is mainly governed by the increase of the drain voltage. Its effect is called the DIBL (Al-Mistarihi et al. 2013; Shee et al. 2014).

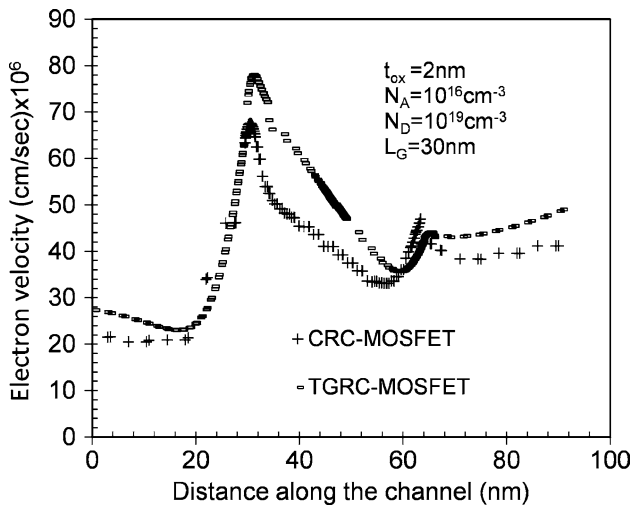
### 3.2 Electric field, electron velocity and ON current

Figure 3 shows the variation of electric field along the channel. It can be seen that in the TGRC-MOSFET, the electric field peak near the source side is higher compared to drain side. The reduction in electric field at the drain end can be interpreted as a reduction in hot carrier effects, lower impact ionization and higher breakdown

voltage. Figure 4 shows the variation of electron velocity of TGRC-MOSFET and CRC-MOSFET along the channel. Here the electron velocity is more at source side in TGRC-MOSFET in compare to CRC-MOSFET. As Fig. 4 shows electron velocity at drain side is lower in TGRC-MOSFET in comparison to CRC-MOSFET which reduces hot carrier effects. Figure 5 shows high ON current in TGRC-MOSFET in comparison to CRC-MOSFET which favors its pertinence in switching applications as compared to CRC-MOSFET. In ITO,  $In_2O_3$  contributes many free electrons which increases the electrical conductivity and decreases the resistivity. As a result, the electron velocity near the source side is higher in TGRC-MOSFET which magnifies the source carrier injection into the channel. Thus, the trans-conductance and drive current of TGRC-MOSFET will be more than CRC-MOSFET (Chaujar et al. 2008; Long and Ken 1997).



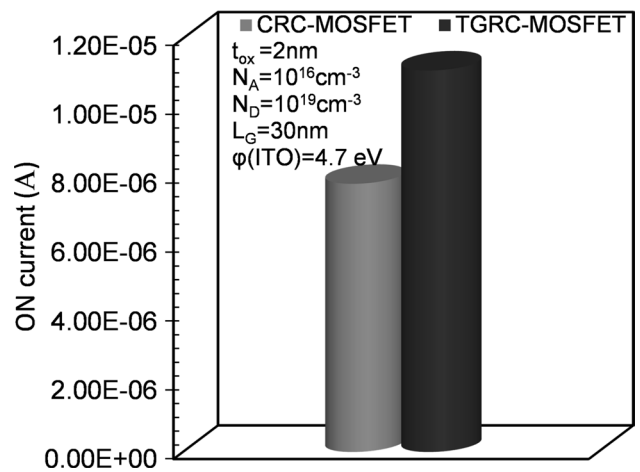
**Fig. 3** Electric field as a function of position along the channel for CRC-MOSFET and TGRC-MOSFET at  $L_G = 30$  nm,  $V_{ds} = 0.5$  V and  $V_{gs} = 0.7$  V



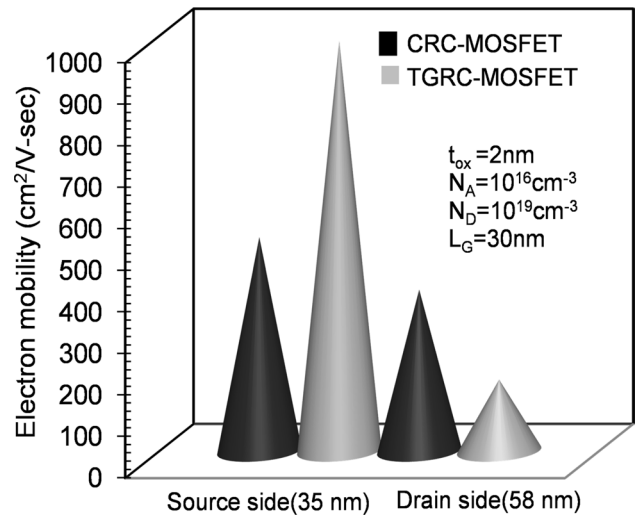
**Fig. 4** Electron velocity as a function of position along the channel for CRC-MOSFET and TGRC-MOSFET at  $V_{ds} = 0.5$  V and  $V_{gs} = 0.7$  V

**3.3 Electron mobility and electron temperature**

Figure 6 shows the variation of electron mobility of TGRC-MOSFET and CRC-MOSFET along the channel. Here the electron mobility is high at source side in TGRC-MOSFET in comparison to CRC-MOSFET. Figure 6 shows that electron mobility at drain side is higher in CRC-MOSFET in compare to TGRC-MOSFET which reduces hot carrier effects. The mobility of charge carriers in ITO thin films is largely stimulated by four scattering mechanisms: lattice scattering, ionized impurity scattering, neutral impurity scattering, and grain boundary scattering (Thilakan



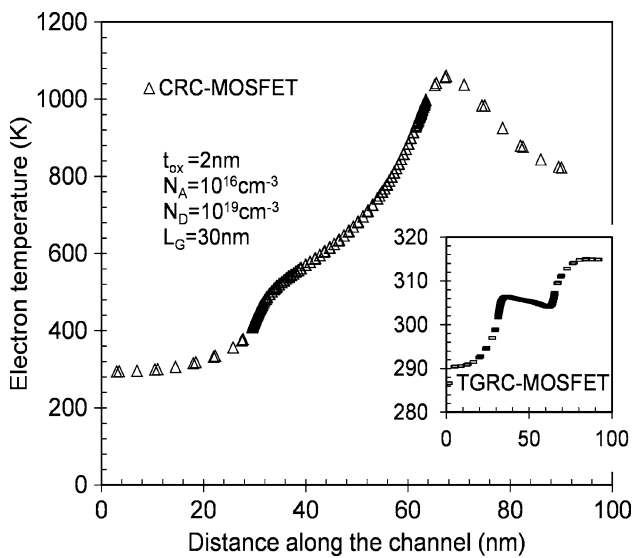
**Fig. 5** ON current for CRC-MOSFET and TGRC-MOSFET at  $V_{ds} = 0.5$  V and  $V_{gs} = 0.7$  V



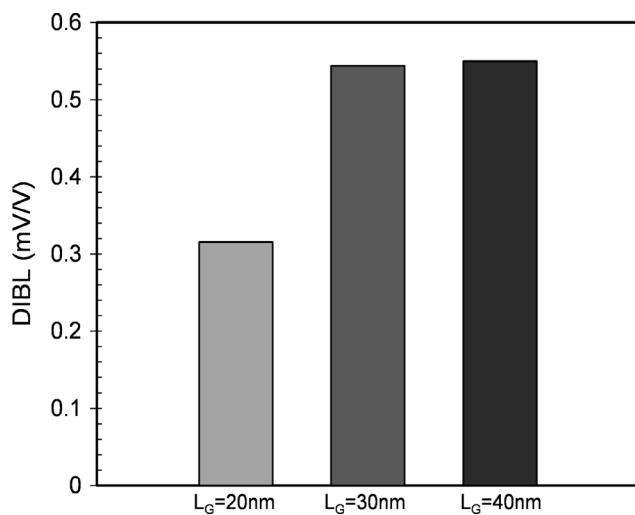
**Fig. 6** Electron mobility of TGRC-MOSFET and conventional RC-MOSFET at 35 and 58 nm along the channel at  $V_{ds} = 0.5$  V and  $V_{gs} = 0.7$  V

and Kumar 1997). In ITO, tin oxide creates more electrons, thereby increasing the carrier concentration and hence decreasing the mobility at drain side and increasing at source side.

Figure 7 shows the variation of electron temperature across the channel length of MOSFET. In CRC-MOSFET high electron temperature at the drain side ostentation that hot carrier effect is more in CRC-MOSFET as compared to TGRC-MOSFET. When we use ITO as a transparent conducting material, mobility and carrier concentration is directly dependent upon temperature. When carrier concentration increases and mobility decreases, then the increase in electron temperature is less in TGRC-MOSFET



**Fig. 7** Electron temperature as a function of position along the channel for CRC-MOSFET at  $V_{ds} = 0.5$  V and  $V_{gs} = 0.7$  V. Inset Electron temperature as a function of position along the length for TGRC-MOSFET at  $V_{ds} = 0.5$  V and  $V_{gs} = 0.7$  V



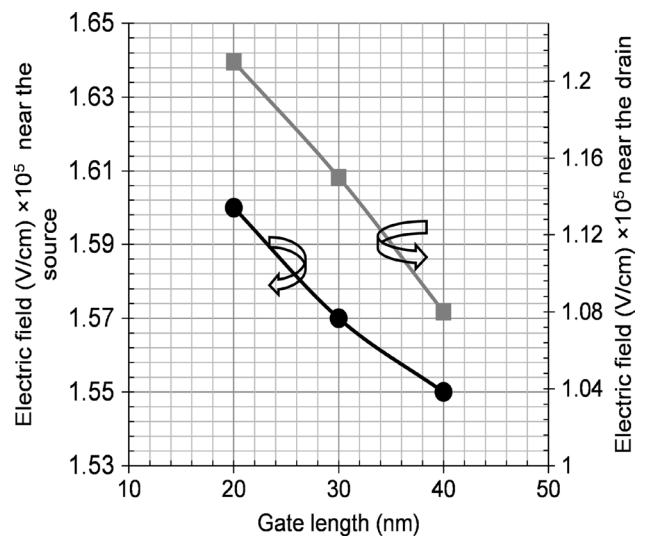
**Fig. 8** DIBL variation for TGRC-MOSFET at different gate lengths

compared to CRC-MOSFET. Increase in electron temperature may cause the device damage and hot-carrier degraded performance.

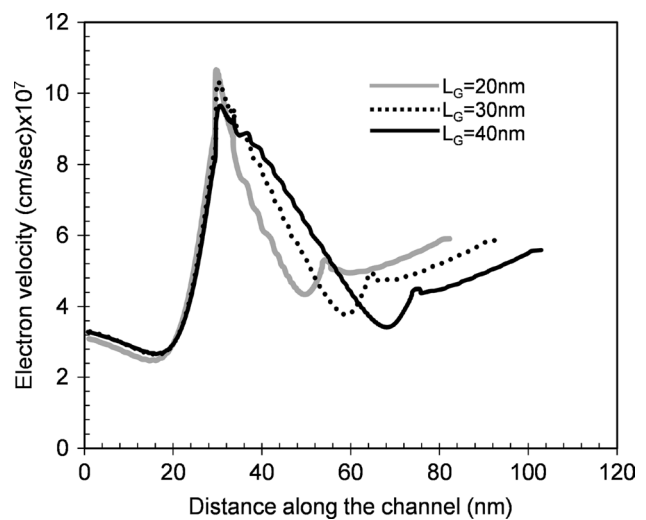
#### 4 Effect of gate length variation

##### 4.1 Drain induced barrier lowering (DIBL)

Figure 8 shows the impact of gate length variation on DIBL for  $V_{ds} = 0.5$  V and  $V_{gs} = 0.8$  V. It is clearly evident from the figure that when the gate length reduces from



**Fig. 9** Electric field variation along the channel for TGRC-MOSFET at different gate lengths



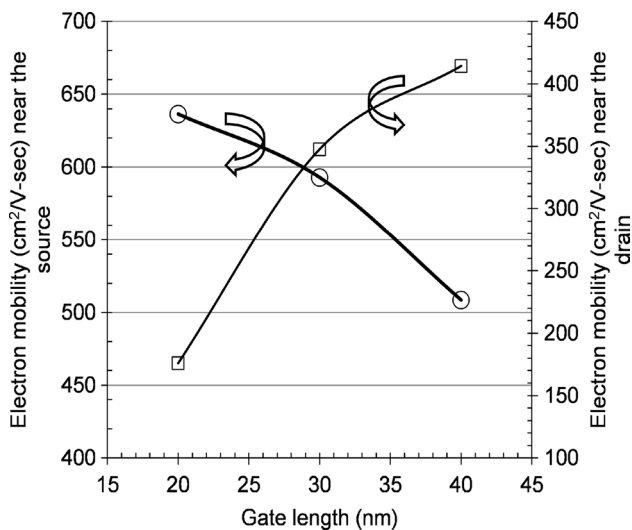
**Fig. 10** Electron velocity variation along the channel for TGRC-MOSFET at different gate lengths

40 to 30 nm, reduction in DIBL is 1.8 % and when gate length reduces from 30 to 20 nm, the reduction in DIBL is 71.4 %. Thus TGRC-MOSFET shows significant reduction in DIBL as the gate length approaches sub 100 nm regime.

##### 4.2 Electric field

Figure 9 shows that the variation of gate length from 40 to 30 nm enhances electric field at source side as compare to the drain side. A further reduction in gate length from 30 to 20 nm results in a significant enhancement in electric field. At the drain side, electric field is lower as compared





**Fig. 11** Electric field variation along the channel for TGRC-MOSFET at different gate lengths

to source side when the gate length is reduced. The reduction in electric field at the drain end can be interpreted as a reduction in lower impact ionization, hot carrier effects, and higher breakdown voltage (Hajjiah and Huang 2004).

### 4.3 Electron velocity and electron mobility

Electron velocity of TGRC-MOSFET is observed with the gate length variation from 40 to 30 nm and from 30 to 20 nm as shown in Fig. 10. Electron velocity is higher at  $L_G = 30$  nm as compared to  $L_G = 40$  nm. Further reducing the gate length from 30 to 20 nm results an improvement in electron velocity at the source side as compared to drain side in TGRC-MOSFET (Gomez et al. 2009). Thus, enhancement in electron velocity at the source side makes the device faster hence; it is suitable for switching applications. Reduction of electron velocity at drain side interpreters less impact ionization hence, hot carriers reduced in TGRC-MOSFET.

Figure 11 shows the impact of gate length variation on electron mobility in TGRC-MOSFET. It is clearly evident from the figure that Electron mobility increases near the source and decreases near the drain with reducing the gate length. When gate length decreases from 40 to 30 nm then electron mobility enhances 16.7 % and a further reduction in the gate length from 30 to 20 nm increases the electron mobility increase by 7.3 % at the source side.

## 5 Conclusion

Here we focus on Transparent Gate architecture in which transparent gate is incorporated on conventional recessed

channel MOSFET for improved hot-carrier reliability of scaled MOS devices. Intensive 3-D TCAD device simulations have been performed to probe the internal transport conditions of CRC MOSFET and TGRC-MOSFET, and substantial interpretation is given to the internal behaviors observed in all the devices investigated. TCAD simulation reveals the deterioration in hot-carrier effects metrics such as electron velocity, potential, electron mobility and electron temperature. Further the gate length variation shows enhanced property when gate length reduces from 40 to 20 nm. This work presents TGRC-MOSFET a reliable device for high performance applications in CMOS technology.

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