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TECHNICAL PAPER

Performance enhancement of FINFET and CNTFET at different node technologies

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Abstract Developing technologies need smaller and faster IC's, hence transistor size has to be scaled down. In order to satisfy this, transistor size in a chip has been decreased drastically from micro range to nano-range. MOSFET was the mass element in any IC at micro size, but when scaled down to nano regime performance degrades because of short channel effects. It is shown here that the FinFET, which gives the better performance and scalability, will replace it. However in 14 nm node and beyond, FinFET also has certain disadvantages; hence some performance enhancement techniques have been introduced to yield good results in 14 nm node. Such techniques include changing the channel materials, use of high-K gate dielectric, etc. We used parameters defined in ITRS update 2013 to simulate FinFET in 14 nm node and we adapted various techniques. Finally the performance enhancement of both finFET and CNTFET for 14 nm node is shown.

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1 Introduction

As Gordon Moore predicted, over the last three decades number of transistors in a single chip has been increased significantly from thousand to several billion. A result of these advancements in technologies gave us high-speed multicore processor technology, huge size memory devices, etc. Yet, today's emerging advanced robotic systems and embedded systems need higher speeds, smaller sized IC's to push boundaries of their performance and current IC technologies are unable to deliver their requirement. Hence development of such systems remains a challenge. To support development of such systems, it is necessary for IC technology to scale down the transistors and increases the speed and performance. Metal Oxide Semiconductor Field Effect Transistor (MosFET) allowed us to build everyday advanced systems such as Smart Phones, Laptops, etc., which is prior to the 22 nm node. In 22 nm node further scaling down of MosFET has become impossible due to increased Short Channel Effects (SCE) such as Drain Induced Barrier lowering (DIBL), Impact Ionization,velocity saturation, Channel length modulation, Oxide breakdown, etc. Hence for advancements in 22 nm node most of the foundries introduced new type of transistor called Fin Field Effect Transistor (FinFET), which has less SCE's, and better control over the channel; this transistor structure is being used in 16 and 14 nm node also. However it is found that in 14 nm node FinFET has serious issues, which will degrade the performance of the IC. Carbon Nano Tube Field Effect Transistor (CNTFET) is one of the emerging transistor technologies, showing great promise for future IC technology. It is also mentioned as the future of transistors in every International Technology Road map for Semiconductors (ITRS) updates. This paper is organized as follows; in Sects. 2 and 3 we've covered

the FinFET and CNTFET technology and its issues, Sect. 4 covers details about simulation works. All performance enhancement techniques are also covered in this section and results are discussed in Sect. 5.

2 Finfet device and issues

InFinFET source and drain are connected by the thin fin which forms the channel and the gate wraps around the channel to control current flow preciously; hence transistor entered into 3D form from the planar form (Fossem and Trivedi 2013). Since more than one gate can be used to control the channel, leakage current reduces significantly and it is also helps to overcome the scaling issues. After a long time FinFET was first implemented by Intel Corporation in 2011 with the name '3D Tri-Gate Transistor' in 22 nm process node (Lundstrom and Guo 2006). FinFET can be made as bulk FinFET by extending bulk substrate as fin and using Shallow Trench Insulation (STI) and Silicon on Insulator (SOI) FinFET by separate fin and substrate regions with oxide region in between them. FinFET's also can have different gating methods: double gate, tri-gate and gate-all-around. Tri-gate FinFET's are used by most of the foundries due to process simplicity and less additional costs (Colinge 2008). Figure 1 shows the structure of SOI-FinFET with three gates.

However, FinFET holds some disadvantages due to vertical structure of its fin such as corner effects, parasitic capacitance and process-induced variability. Corner effects are caused due to corners in rectangular fins of FinFET; which results in degraded performance. Parasitic capacitance include source and drain capacitance and capacitance that exist between two regions of FinFET, which lead to poor performance and some reliability issues. Process induced variability includes Random Discrete Dopants (RDD) and Line Edge Roughness (LER) (Seoane et al. 2014). Ion implantation process with high temperature annealing produces discrete dopants that are distributed randomly over the entire region causing RDD. LER is caused by the minute structure of photo resist used in the lithography process; this resist has rough surfaces which produces variations in the edge of the gate while patterning

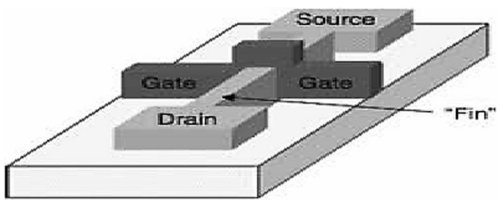

Fig. 1 Structure of FinFET showing source drain, gate and fin regions

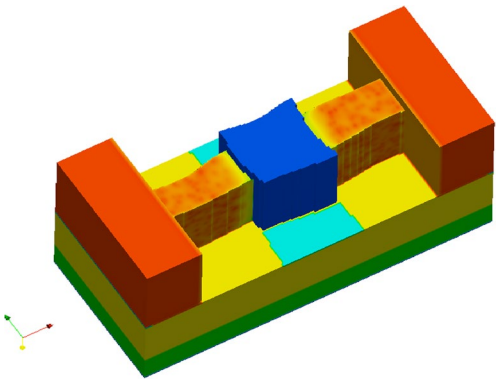

Fig. 2 Electron density with combined effect of RDD and LER in FinFET

the gate. Electron density of the FinFET with combined effect of RDD and LER simulated by Gold Standard Simulations (GSS) Ltd is shown in Fig. 2. Fin and gate roughness of the FinFET can be clearly seen from figure.

3 CNTFET device and issues

Unlike FinFET's, CNTFET's are ballistic devices with high mobility Carbon Nano Tube (CNT) as channel. It has the ability to minimize sub-threshold slope and hence SCE's. Different types of CNTFET's are proposed since the invention of CNT's; such as MosFET like CNTFET, Schottky barrier type CNTFET, surrounded gate CNTFET, suspended CNTFET, vertical CNTFET, etc. MosFET like CNTFET has the advantages of CMOS process compatibility, less variation to changing gate length, high ON current, etc. It is still in the research phase because of its reliability issues. Surrounded gate CNTFET also one of the suggested architectures which has the advantage of better control over the channel, but there are several challenges to realize this advantage which are controlling band gap energy, gate dielectric deposition, low resistance contact formation, placing of nano tubes, etc. In the last 5 years major advancements have been made in the fabrication of CNTFET's such as fabrication of carbon nano tube computer with 178 transistors (Usmani and Hasan 2010), fabrication CNTFET based CMOS inverter, fabrication of CNTFET with high ON current. These shows CNTFET's are potential devices for future VLSI applications but all challenges should be faced carefully. MosFET like CNTFET with top gate is shown in the Fig. 3 (Shulaker 2013).

4 Related work

As device is scaled to Nano-size, it is difficult to model the device due to effect of quantum mechanics coming into the

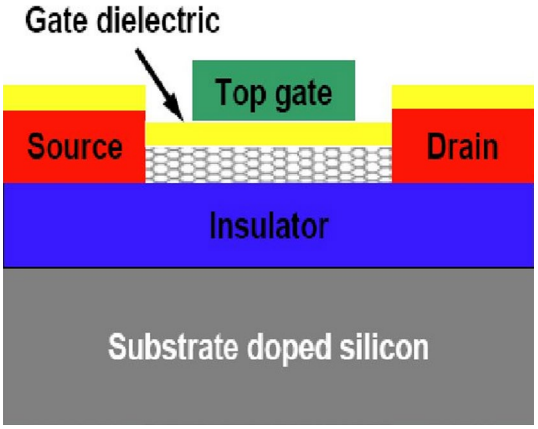

Fig. 3 Structure of MosFET like CNTFET with *top gate*

Table 1 Device parameters under taken for simulation study

Parameters	Technology nodes	
	22-nm	14-nm
Channel length (L_G) (nm)	22 [20–25]	16.8
Oxide thickness (T_{OX}) (nm)	1	0.77
Fin thickness (T_{FIN}) (nm)	10 [10–12]	6.7
Fin height (H_{FIN}) (nm)	40 [24–50]	30 [14–40]
Gate height (H_{GATE}) (nm)	40	40
Channel doping concentration (N_{CH}) (cm^{-3})	10^{15}	10^{15}
Source and drain doping concentration (N_{SD}) (cm^{-3})	10^{20}	10^{20}
Supply voltage (V_{DD}) (V)	0.95	0.85

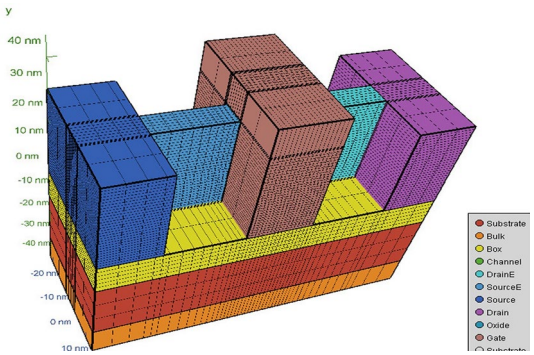

Fig. 4 Simulated structure of FinFET

scope. Classical approaches such as Drift Diffusion method is not suitable for accurate simulation of the device because such method will not model the quantum transport taking place inside the device. Hence it is necessary to model the device using quantum mechanical simulations. However quantum mechanical approaches require multi core system to compute complex and iterative equations. It also requires a great deal of time to perform the simulation. Hence an approximate approach is to do simulation using one of the classical approaches coupled with some quantum correction model. In ITRS update 2013 (Usmani and Hasan 2010) it is mentioned that major challenges in TCAD modeling are to do quantum simulation with atomistic models. It also mentions that results taken by the classical approaches will not be valid for device with parameters defined for 14-nm node and beyond. Hence we have performed the simulations in GTS Framework using density gradient model, effect of Impact Ionization; band to band tunneling, band gap narrowing and oxide tunneling are taken into account with quantum correction. We carried out the FinFET simulation using parameters defined for 14-nm node in ITRS update 2013 (Swahn and Hassoun 2006) and for 22-nm node we used industrial standard parameters. Table 1 lists the parameters used for simulation for 22-nm and 14-nm node. The simulated device structure is shown in Fig. 4.

Since our goal is to enhance the performance of the FinFET, using different techniques we have completed the simulation in techniques suggested by ITRS update 2013. These techniques are described below:

4.1 Using different material for channel

Silicon (Si) has less carrier mobility compared to material such as Germanium (Ge), Silicon–germanium (SiGe), Indium gallium arsenide (InGaAs), etc. Since current in the device is directly proportional to the carrier mobility, these materials will give the good performance when used as a channel material for the device. In ITRS update 2013 this point is further stressed and challenges to implement this technique are described. It goes on to state that Ge is the most acceptable option for channel although it has some issues regarding manufacturing process. Hence we have simulated the FinFET with Ge and another good candidate SiGe as the channel. Results are discussed in Sect. 5.

4.2 Using High-k materials as insulator

The concept of using High-k dielectric materials is already implemented in CMOS process; the same can be used to enhance the performance of FinFET. Since current is directly proportional to dielectric constant of gate dielectric, use of material with high dielectric constant as gate insulator will give the good performance. Hafnium based dielectric materials (Usmani and Hasan 2010), i.e., hafnium oxide (HfO_2), Zirconium oxide (ZrO_2) and Titanium oxide (TiO_2) are the proposed materials because of their high dielectric constant and stability. In ITRS update 2013 use of these materials as dielectric and related issues have been discussed. It's reported that

major issues in the implementation of these materials are: controlling and maintaining the thickness of the dielectric and their variations, effect of channel roughness to their reliability and effect of reduction or elimination of SiO_2 interfacial layer to their mobility. Once these challenges are overcome these materials are ultimate options as gate dielectric and thereby to increase the performance of the device. In this context we simulated FinFET with these materials.

4.3 Implementation of Gate-all-around structure

Tri-gate FinFET's are used to make IC's in most of the foundries, but when they are scaled down below 14 nm, there will be increase in the SCE's which will degrade the performance. Implementation of Gate-all-around structure in FinFET is a good solution; this technique is also discussed in ITRS update 2013. Implementation of such technique will also enhance the performance of the FinFET in 14-nm node. Hence we simulated the Gate-all-around FinFET with SiO_2 and HfO_2 as gate dielectrics.

Implementation of CNTFET also discussed in ITRS update 2013 (Usmani and Hasan 2010; Manoj and Ramgopal Rao 2007; ITRS 2013a, b). In 14-nm technology node and beyond this device is listed as one of the options to achieve better performance. In this context we simulated CNTFET for 22-nm and 14-nm node. We have taken main parameters defined for 14-nm node and simulated CNTFET using the Stanford CNFET model (Usmani and Hasan 2010). In order to compare the performance of CNTFET with FinFET we carried out the simulation using both SiO_2 and HfO_2 as gate dielectric. All these results are discussed in the next section.

5 Results and discussions

First we carried out the simulation for 22-nm node and then repeated the simulation for 14-nm node. Figure 5 shows the I–V characteristics of FinFET in both technology nodes. We found that FinFET will give more OFF current in 14-nm node without any performance enhancement technique. This increased OFF current of FinFET in 14-nm can be easily seen from the graph. As next step we simulated FinFET with all performance enhancement techniques described in previous section. ON current (I_{ON}), OFF current (I_{OFF}) and I_{ON}/I_{OFF} ratio of the FinFET in all simulations are listed in Table 2.

It can be clearly observed from the table that using all listed techniques I_{ON} of FinFET is increased, I_{OFF} of FinFET is decreased and hence I_{ON}/I_{OFF} ratio is increased compared to earlier simulated FinFET with low-k dielectric (SiO_2). And also I_{ON}/I_{OFF} ratio is significantly increased

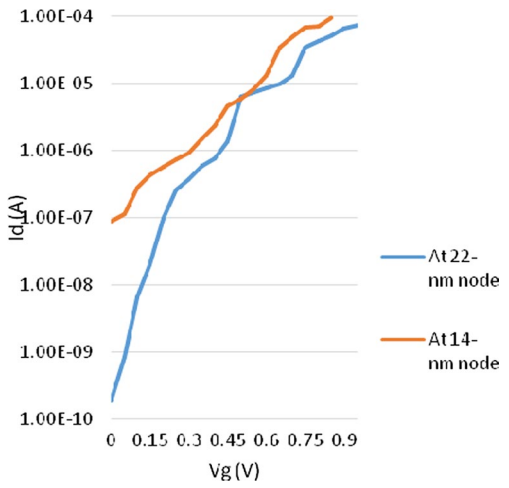

Fig. 5 I-V characteristics of FinFET for 22-nm and 14-nm node

Table 2 Results obtained in FINFET simulations

	I_{ON} (μA)	I_{OFF} (nA)	I_{ON}/I_{OFF} ratio
FinFET with three gates, Si as channel and SiO_2 as gate dielectric			
	94.3	88.6	1.06E + 3
FinFET with different materials as channel			
Ge	169.3	1.09	1.55E + 5
SiGe	187.8	0.576	3.26E + 5
FinFET with different gate dielectrics			
HfO_2	241.7	0.57	4.24E + 5
TiO_2	431.3	0.385	1.12E + 6
ZrO_2	235.6	0.593	3.97E + 5
Gate all around FinFET with different gate dielectrics			
SiO_2	189.7	0.124	1.52E + 6
HfO_2	317.14	0.079	4.01E + 6

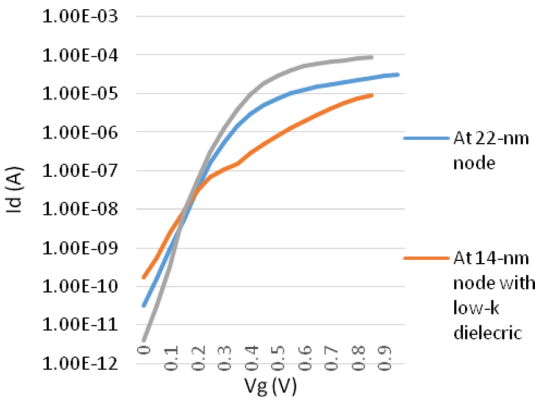

Fig. 6 I-V characteristics of CNTFET in 22-nm and 14-nm

in FinFET with High-k gate dielectric and with Gate-all-around geometry. Figure 6 shows the contour plots of electric field in channel region of the simulated FinFET with

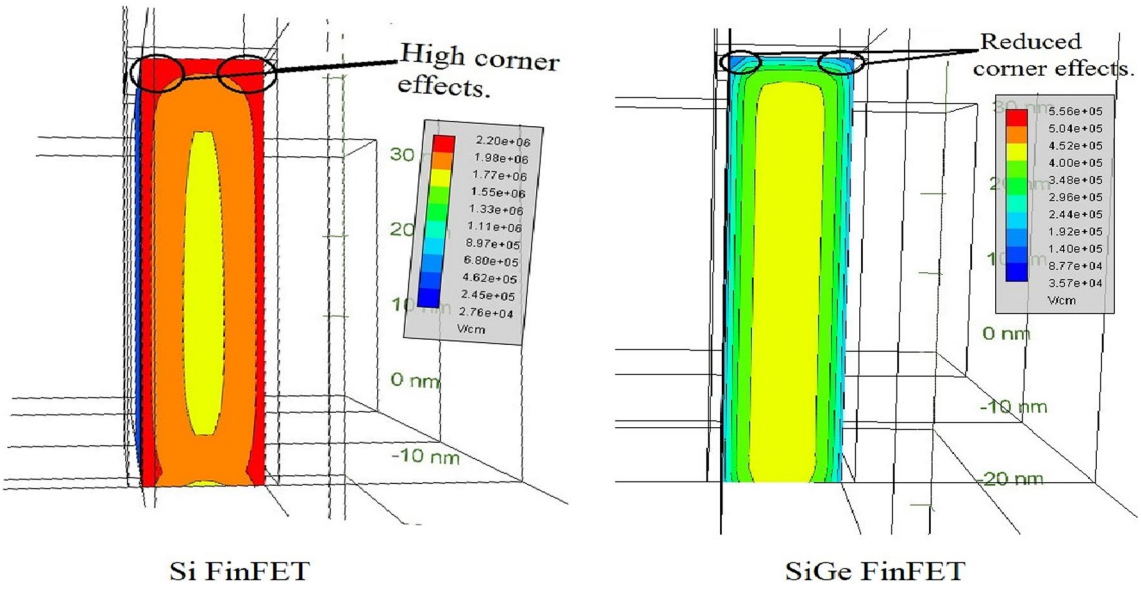

Fig. 7 *Contour plots* of electric field in the fin region of Si and SiGeFinFET at ON state ($V_g = 0.85$ V) showing Corner effects

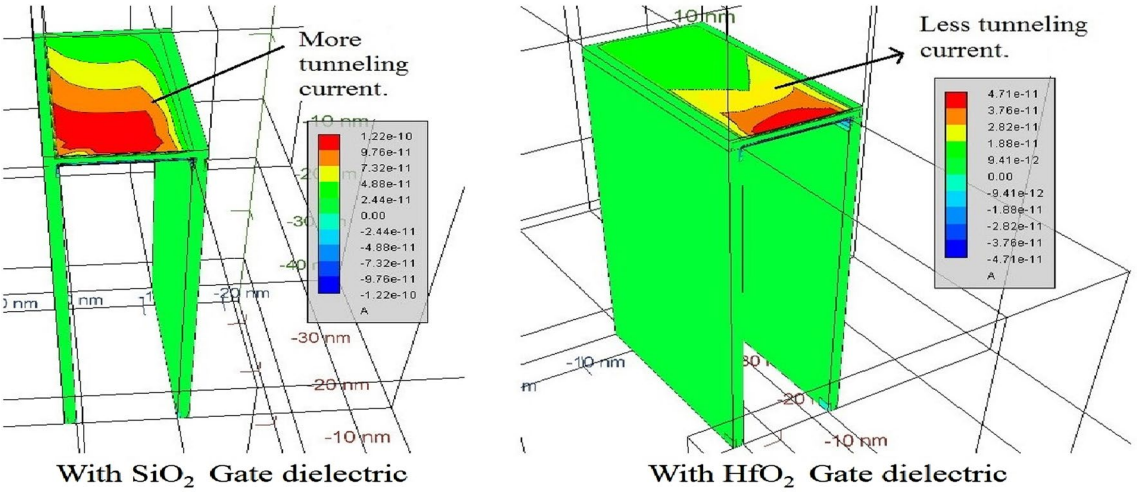

Fig. 8 *Contour plots* showing the tunneling current through oxide region of FinFETat ON state ($V_g = 0.85$ V) with SiO_2 and HfO_2 as gate dielectric

Si and SiGe as the channel. As stated in earlier section one of main disadvantages of FinFET is corner effect; because of this effect, maximum electric field is situated at the corner of the fin which lead to leakage and hence degrade the performance. It can be easily seen from the figure that with SiGe as channel this effect is minimized. HenceSiGe is the good candidate for channel material to minimize the corner effects. Figure 7 shows the contour plots of tunneling current in the oxide region of the simulated FinFET with SiO_2 and HfO_{-2} as gate dielectrics. This tunneling current occurs due to scaling of oxide thickness, which is major source for leakage current. It can be easily seen from the figure that HfO_2 gives less tunneling current hence it is the most suitable choice for enhanced operation of FinFET. I–V characteristics obtained from CNTFET simulation described in earlier section are shown in Fig. 8 for both 22-nm and 14-nm node. It is clearly indicated from the figure that CNTFET shows less variation in the performance as result of scaling. In this case use of High-k material (HfO_2) dielectric will increase the I_{ON}/I_{OFF} ratio. Finally results of FinFET and CNTFET simulation with different gate dielectrics are tabulated in the Table 3. It is clear from the table that CNTFET shows better performance compared to FinFET.

Table 3 Results comparison between FINFET and CNTFET

14-nm node	I_{ON}/I_{OFF} ratio	
	FinFET	CNTFET
With Low-k dielectric material (SiO_2)	1.06E + 03	5.30E + 04
With High-k dielectric material (HfO_2)	4.24E + 05	2.27E + 06

6 Future scope

As stated earlier device modeling can be accurately done using quantum simulation; hence simulating the FinFET and CNTFET with quantum transport approach will give exact results. FinFet variability analysis also can be done to understand the design issues. Further, simulation for node less than 14-nm can also be performed for more research on FinFET and CNTFET.

7 Conclusion

Various simulations of FinFET were carried out with different channel materials, with different gate dielectrics and with Gate all-around geometry for 14-nm technology node. We found that performance of the FinFET increase by use of channel material other than Si, using High-k materials as gate dielectric and with Gate all-geometry. These three cases are proposed as the performance enhancement techniques for FinFET for 14-nm node and beyond. Using any of the techniques or all techniques, performance of FinFET can be enhanced. Simulations of CNTFET were also carried out for 14-nm node. We found that CNTFET shows better performance compared to FinFET; hence this device is proposed as an alternative to FinFET in 14-nm node and beyond. As mentioned in ITRS update 2013, there are also some issues to be faced in the implementation of mentioned techniques. These issues should be handled carefully to deliver IC's with increased speed and performance.

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