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TECHNICAL PAPER

# A new design of multi-bit RF MEMS distributed phase shifters for phase error reduction

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**Abstract** In this paper, the major source of phase error for multi-bit MEMS distributed phase shifters, the mismatch between adjacent bits, is investigated. A quantitative account of the phase deviation with the effect of mismatch considered is presented by the simulated results as well as theoretically calculated results. A novel multi-bit distributed MEMS phase shifter aimed to eliminate this error source is proposed. The basic concept for the structure is that, by controlling the phase shifter from the unit cell level, performance deterioration resulted from multiple reflection of the signal in the device in the phase state switching process is avoided. To verify the feasibility of the proposed structure, two X-band 5-bit distributed phase shifters are designed and simulated. Compared with the traditional structure, the average phase errors in all phase states of the two are improved by 28.22 and 36.52 % at 10 GHz. The average RMS phase errors in the bandwidth of 1–12-GHz of 56 frequency points are 1.23° and 1.85°. The improvements of the return loss and insertion loss are also exhibited. Furthermore, the aperiodic distributed phase shifter using different unit cells is introduced to demonstrate that the proposed structure can also be used to decrease the number of MEMS switches of multi-bit MEMS distributed phase shifters.

**Abbreviations**

| | |
|---|---|
| RF MEMS | Radio frequency micro-electromechanical system |
| MAM | Metal–air–metal |
| DMTL | Distributed MEMS transmission line |
| DC | Direct current |
| RMS | Root mean square |
| CPW | Coplanar waveguide |

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## 1 Introduction

RF MEMS phase shifters attracted much attention due to their excellent performance including low loss, high linearity and slight DC power consumption (Rebeiz et al. 2002). They bring about system optimization and performance improvements utilized in phased-array applications for satellite communications and radar systems.

There are mainly two kinds of RF MEMS phase shifter. One is the phase shifter based on RF MEMS switches (Tan et al. 2003; Morton and Papapolymerou 2008; Gong et al. 2011). This MEMS switch with many different kinds of structures is one of the most wildly studied MEMS devices (Hyman et al. 1999; Al-Dahleh and Mansour 2010; Yamane et al. 2011). The other is using DMTL (distributed MEMS transmission line) which is initially advanced in 1998 (Barker and Rebeiz) and then more research has been done (Janardhana et al. 2008; Hayden and Rebeiz 2003; Goel and Vinoy 2011). MEMS bridges in each bit show two states (the up-state position and the down-state position) by applying a signal bias.

Compared with phase shifters based on RF MEMS switches, MEMS phase shifters based on DMTL are easier to achieve standardized design process, precise design, process error control of mass production and a short experimentation cycle.

Typically, phased arrays consist of multiple stationary radiating elements, each of which is fed by tunable phase or time-delay control units to steer the beam. Electronic

phase shifters could vary the insertion phase of the incoming signals. One of figures of merit for phased arrays is Beam-pointing error, where RMS phase error of phase shifters is a decisive factor (Caekenberghe 2009). Therefore, the phase error of phase shifters is critical for it determines the scan accuracy of phased arrays.

However, the phase error of distributed MEMS phase shifters is not very satisfactory, especially for multi-bit 0–360° phase shifters (Liu et al. 2000; Lakshminarayanan and Weller 2007; Perruisseau-Carrier et al. 2006), which will delay their use in the system demanding higher precision. The sources of phase error for MEMS distributed phase shifters include parasitic parameters, stability of MEMS bridges, the process error causing height changes of MEMS bridges and dielectric layer flatness error etc. Hayden and Rebeiz propose the structure of MAM capacitor and MEMS bridge in series connection to ensure the capacitance ratio in two states of MEMS bridge and increase the phase shift accuracy (Hayden and Rebeiz 2003). This approach is an effective and simple optimization program and currently applied in a wide range of RF MEMS devices including digital tunable capacitors (Topalli et al. 2008; Zou et al. 2009; Park et al. 2008).

Sources of phase error mentioned previously can be solved through accumulation of fabrication experiences, the structure of MAM capacitor or the accurate modeling. But for multi-bit MEMS distributed phase shifters, the major source of phase error is the mismatch between adjacent bits, which cannot be avoided due to their working mechanism and will be demonstrated in this paper.

Considering the particularity of multi-bit distributed phase shifters, this paper will analyze the mismatch comprehensively, and get the closed-form expression of the phase shift. Abandoning the concept that the distributed phase shifter is constructed by bits, the proposed configuration is controlled from the unit cell level to avoid the mismatch between adjacent bits. This paper also presents the mechanism and design considerations of the proposed structure. The 5-bit distributed phase shifters adopted the periodic design with 31 same unit cells and the aperiodic design with 16 unit cells are designed and simulated to verify the improvements of the proposed design. The 5-bit distributed phase shifters result in the average phase errors in all phase states being reduced by 28.22 and 36.52 % at 10 GHz.

## 2 The phase error for N-bit digital MEMS distributed phase shifters

An N-bit digital phase shifter providing $2^N$ unique phase states from 0° to $360 \cdot (1 - \frac{1}{2^N})°$ is composed by $\frac{360°}{2^{N-1}}$ bit, $\frac{360°}{2^{N-2}}$ bit, $\frac{360°}{2^{N-3}}$ bit…. and $\frac{360°}{2}$ bit in a certain order. Every bit of N-bit RF MEMS distributed phase shifter is constructed by cascading different numbers unit cells. $2^N$ unique phase states are obtained by combination of bits with different state. When switching in different phase states, the entire distributed N-bit digital phase shifter can be considered as N sections of DMTL cascading, whose characteristic impedance switches between $Z_u$ and $Z_d$ and phase constant switches between $\beta_u$ and $\beta_d$. With MEMS bridges of all unit cells cascaded in the same bit keeping in the same state position, *ABCD* matrix of the bit can be expressed as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos(\beta_{u/d} l) & jZ_{u/d} \sin(\beta_{u/d} l) \\ j\frac{1}{Z_{u/d}} \sin(\beta_{u/d} l) & \cos(\beta_{u/d} l) \end{bmatrix} \quad (1)$$

where the DMTL is an ideal transmission line without parasitic parameters to consider. $Z_{u/d}$ refers to characteristic impedance in up or down state, $\beta_{u/d}$ refers to phase constant in the corresponding state, $l$ refers to its physical length. In the phase states switching process, the characteristic impedance of two ports for every bit will be in five cases due to the state switching of adjacent bits, as shown in Fig. 1. The changes of ports characteristic impedance for the bit located at the output or input position are also considered. $Z_0$ refers to terminated impedance of the device.

Mismatch between adjacent bits and its diversity, as shown above, will lead to irregular deviation of phase shift for distributed phase shifters. In the case of multi-bit distributed phase shifters (when N increases), this effect is more significant, causing multi-level reflection leading to a sharp decline in accuracy of phase shift shown in Fig. 2.

In order to alleviate the mismatch between adjacent bits to the minimum, thereby reducing phase shift error in various phase states, $Z_u$ and $Z_d$ should be designed as close as possible. However, the mechanism of distributed phase shifters is that the phase shift obtains according to the changes of characteristic impedance and phase constant. The decrease of $Z_u$ and $Z_d$ difference is bound to increase the physical length $s$ in order to ensure the required phase shift. The physical length $s$ and the

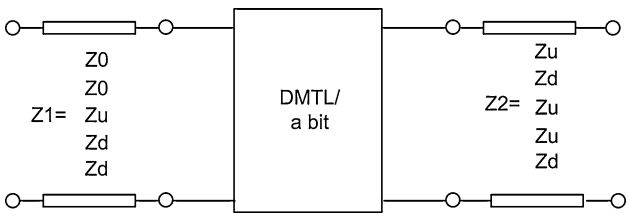


**Fig. 1** Five cases of ports characteristic impedance of a bit in the distributed phase shifter

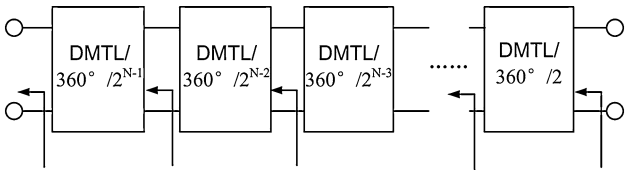


**Fig. 2** Multiple reflection within the N-bit digital MEMS phase shifter constructed by cascading N sections of DMTL

difference of $Z_u$ and $Z_d$ is a contradiction when other design parameters are decided, as shown in:

$$s\left(\frac{1}{Z_d}-\frac{1}{Z_u}\right)=\frac{\Delta\phi c}{2\pi f Z_0\sqrt{\varepsilon_{eff}}} \tag{2}$$

This can be deduced from phase shift expression of DMTL. For the miniaturization of the device, $Z_u$ and $Z_d$ will be different. Therefore, the phase shift error caused by the diversity of the mismatch between adjacent bits cannot be avoided. To carry out quantitative analysis of the effect of switching characteristic impedance of adjacent bits on insertion phase shift of a certain bit, $S_{21}$ of the DMTL shown in Fig. 1 can be derived by deduction of $Z$ matrix:

$$S_{21}=\frac{2}{\sqrt{\frac{Z_2}{Z_1}}\cos\beta l+\frac{jZ_{Insertion}\sin\beta l}{\sqrt{Z_1Z_2}}+j\frac{\sin\beta l\sqrt{Z_1Z_2}}{Z_{insertion}}+\sqrt{\frac{Z_1}{Z_2}}\cos\beta l} \tag{3}$$

where $Z_1$ and $Z_2$ refer to characteristic impedance of two ports, which are illustrated in Fig. 1. When this bit is switching between up and down states, the differential phase shift considered ports impact, is given by:

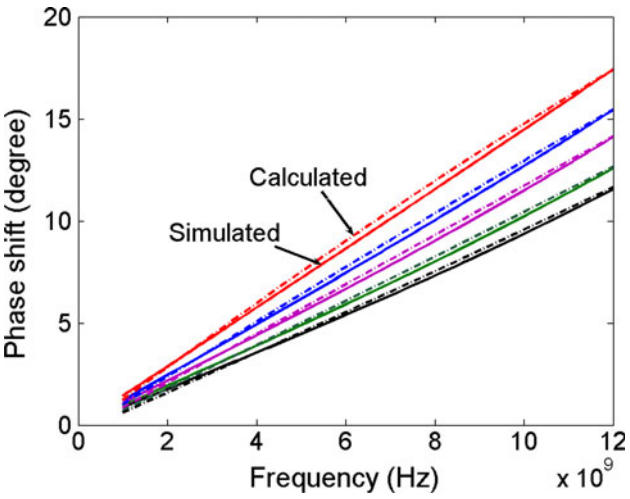


**Fig. 3** Phase shift for a single bit in the distributed phase shifter when the characteristic impedance of two ports is in five cases due to the state switching of adjacent bits

$$\begin{aligned}\Delta\phi &= \arg(S_{21},down)-\arg(S_{21},up)\\ &= \arctan\left[-\frac{\frac{Z_d}{A}+\frac{A}{Z_d}}{B+\frac{1}{B}}\tan\beta_d l\right]-\arctan\left[-\frac{\frac{Z_u}{A}+\frac{A}{Z_u}}{B+\frac{1}{B}}\tan\beta_u l\right]\end{aligned} \tag{4}$$

where $A=\sqrt{Z_1Z_2}.,B=\sqrt{\frac{Z_1}{Z_2}}$, $\beta=\omega\sqrt{L_t(C_t+\frac{C_{load}}{s})}$. where $L_t$, $C_t$ refer to per unit length capacitance and inductance of CPW, $C_{load}$ is the loaded capacitance. Figure 3 shows the variation of phase shift for a single bit in a distributed phase shifter. When characteristic impedance of both ports is 50 Ω, the phase shift of the bit is exactly 11.25°, in which $Z_u$ and $Z_d$ are 66 Ω and 42 Ω respectively. It is seen from the Fig. 3 that the phase shift deviation is obvious when the structure sizes stay the same but the ports characteristic impedance changes. At 10 GHz, the average phase error in five cases reaches 1.57°, the average relative phase error is 14 %, and the maximum phase error is 3.22°. It can be believed that the phase error will deteriorate when the difference between $Z_u$ and $Z_d$ increases. This indicates that the diversified port characteristic impedance caused by adjacent bits is a significant factor affecting the phase error. Figure 3 also shows phase shift changes calculated by Eq. (4). From the observed agreement between calculations and simulations, it can be seen that the above equation can accurately predict the effect of mismatch between adjacent bits on phase shift of a certain bit. After parasitic parameters being considered, this phase shift calculation approach still works, with only specific forms being changed.

## 3 The proposed distributed phase shifters for reduction of phase error

### 3.1 Working principle

This paper presents a novel distributed phase shifter through increasing bias pads to reduce phase error. Instead of controlling from the bit level of the N-bit digital phase shifter, the bias line is exerted from the unit cell level to minimize internal reflection of the transmitted signal in the device resulted from mismatch between adjacent bits. The MEMS bridge in a unit cell is controlled by the biased signal through the bias pad and bias line. In order to ensure the only one discontinuity of characteristic impedance within the device, the control permission for each bias pad and the configuration of the bias is determined according to a certain designed structure of phase shifter, which will be discussed in the following. The top view of the schematics and the bias configurations of the proposed distributed phase shifters are shown in Fig. 4a, b.

When this kind of N-bit distributed phase shifter switches in phase shift states, it is cascaded by two transmission lines.

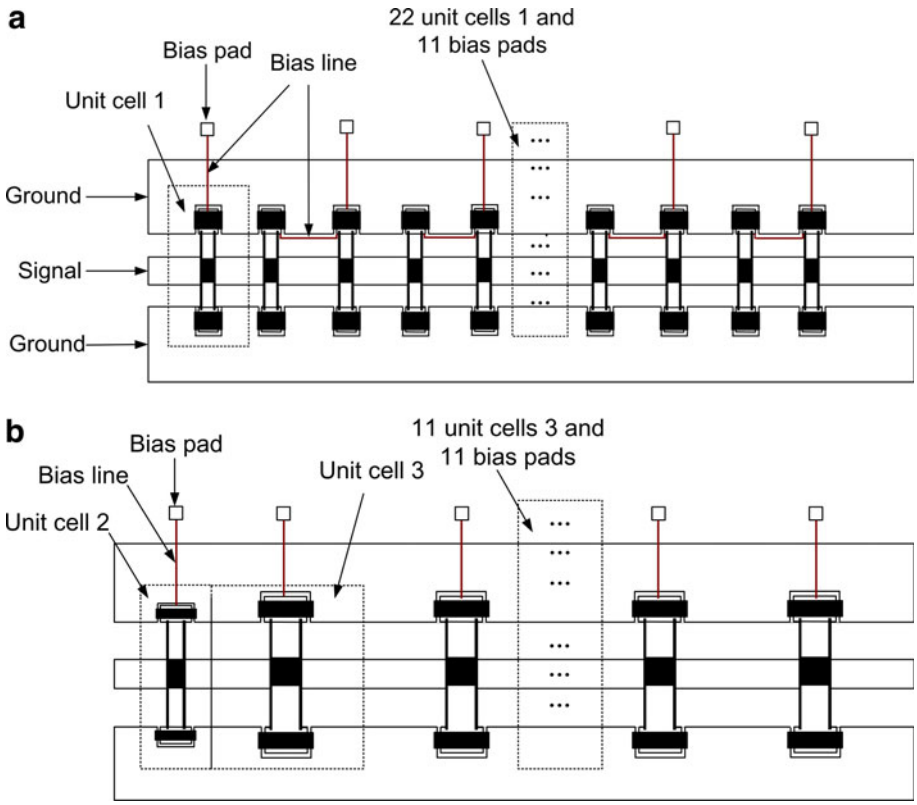


**Fig. 4** Schematics and the bias configurations of the novel 5-bit distributed phase shifters with 16 bias pads **a** the periodic design with 31 same unit cells, **b** the aperiodic design with 16 unit cells

The two transmission lines have different impedance of $Z_u$ and$Z_d$, and the physical length puts up a relation of ebb and flow. In the phase state of $11.25 \times n$, the expression of relationship between the electric length $\beta_1$ and $\beta_2$ of the two transmission lines is given by:

$$\begin{aligned}\beta_1 + \beta_2 &= |\alpha_{totall}| + 11.25 \times n, \beta_1 - \beta_2 \\ &= \frac{2|\alpha_{totall}|}{31} \times n - |\alpha_{totall}| + 11.25 \times n \end{aligned} \quad (5)$$

where $\alpha_{totall}$ is the phase shift of the device when all MEMS bridges are kept in the up state. The phase shift is deduced as:

$$\arg(S_{21}) = \arctan\left[\frac{A \cdot \sin(\beta_1 + \beta_2) + B \cdot \sin(\beta_1 - \beta_2)}{C \cdot \cos(\beta_1 + \beta_2) + D \cdot \cos(\beta_1 - \beta_2)}\right] \quad (6)$$

$$\begin{aligned} A &= \frac{1}{4Z_0}(Z_u + Z_d) + \frac{Z_0}{4}\left(\frac{1}{Z_u} + \frac{1}{Z_d}\right) \\ B &= \frac{1}{4Z_0}(Z_u - Z_d) + \frac{Z_0}{4}\left(\frac{1}{Z_u} - \frac{1}{Z_d}\right) \\ C &= \frac{1 + \frac{Z_u}{Z_d} + \frac{Z_d}{Z_u}}{4}, D = \frac{1 - \frac{Z_u}{Z_d} - \frac{Z_d}{Z_u}}{2} \end{aligned} \quad (7)$$

The N-bit distributed phase shifter in this working mechanism, on the one hand, improves the phase shift accuracy, for avoiding the unpredictable phase shift deviation caused by the mismatch between bits; on the other hand, flexible combination of the unit cells can be arranged to achieve the optimal performance. Furthermore, due to reduction of reflection in the cascading composition, the deterioration of the return loss is limited. The contradiction of miniaturization and return loss is alleviated to some extent, so shorter physical length can be obtained in the design of the unit cell, which is particularly important for distributed phase shifters in lower frequency. Besides, it also allows increasing the amount of phase shift of one unit cell to reduce the number of MEMS bridges in 0°–360° phase shifters. Based on this point, abandoning the periodic structure, the aperiodic distributed phase shifter shown in Fig. 4b is presented, in which unit cells realizing different phase shift are adopted.

### 3.2 Design and simulation

X-band 5-bit distributed phase shifters adopted two design schemes are designed and simulated to demonstrate the proposed distributed phase shifter structure. The first is a periodic design in which 31 same unit cells with the phase shift of 11.25° cascaded to achieve 5-bit phase shifter. The unit cell located at input or output port is individually controlled by a bias pad. The control right of this bias pad is 11.25° and all of the other pads control two unit cells.

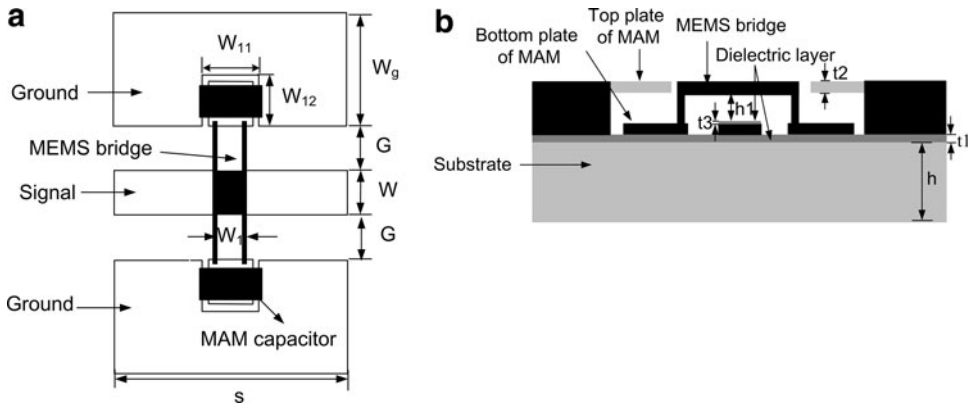


**Fig. 5** **a** *Top* and **b** *cross-sectional view* of the unit cell with MAM capacitor of distributed phase shifters

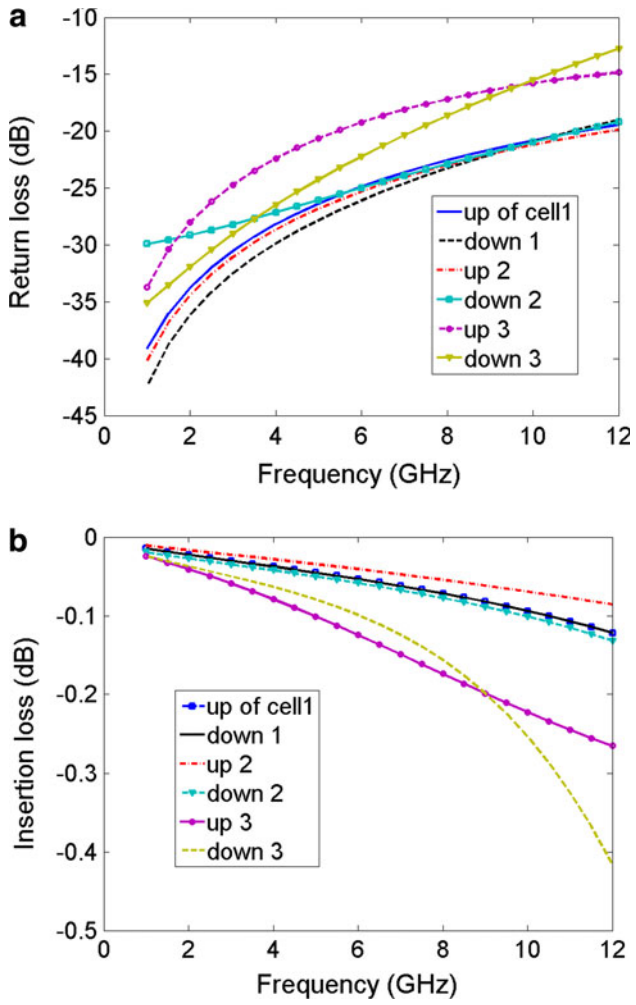


**Fig. 6** RF characteristics of the three types of unit cells **a** return loss, **b** insertion loss

The control right of these pads is 22.5°, which is realized by connecting MEMS bridges of the two unit cells as shown in Fig. 4a. The second design is aperiodic by cascading 16 unit cells. There are two types of unit cell as shown in Fig. 4b. The unit cell located at input or output port has phase shift of 11.25°, other 15 unit cells have the phase shift of 22.5°. Each unit cell is controlled by a bias pad. The control rights of the bias pads connected to the two types of unit cell are also 11.25° and 22.5°, respectively.

In the two design schemes of X-band 5-bit distributed phase shifters, three unit cells are designed and optimized firstly. The unit cell consists of CPW, MEMS bridge and MAM capacitor, as shown in Fig. 5. Unit cell 1, unit cell 2 and unit cell 3 are used to represent the unit cell of the phase shift of 11.25° in the periodic design scheme, the unit cell of the phase shift of 11.25° and 22.5° in the aperiodic design scheme. Figure 6 shows the S-parameters of the three unit cells in two design schemes, which are simulated by 3-D Full-Wave EM simulator Ansoft HFSS. At 10 GHz, for the unit cell 1 and unit cell 2, the return loss is below than −20.8 dB and the worst case of the insertion loss is −0.1 dB, when MEMS bridges are either in down-state position, or in up-state position. For the unit cell 3, the return loss and the the insertion loss are better than −15.5 dB and −0.22 dB. The dimensions and design parameters of three types of unit cells in periodic and aperiodic design are given by Table 1. $C_L$ refers to the equivalent loaded capacitances.

As for unit cell 3 of bigger phase shifter, the Bragg frequency $f_B$ should be taken into account in design to ensure that it is far away from the operation bandwidth. Ignoring the effect of inductance and resistance, $f_B$ of DMTL can be calculated by (Rebeiz 2003):

$$f_{bragg} = \frac{1}{\pi s\sqrt{L_t(C_t + \frac{C_b}{s})}} \tag{8}$$

where $C_b$ is the loaded capacitance when all MEMS bridges are in down-state position. Based on the current MEMS process, the sacrificial layer $h_1$ is confirmed to be 2.0 m and silicon dioxide is used as dielectric layer with the thickness of 200 nm. The phase shifters will be fabricated on 400-m-thick high resistivity silicon substrate whose surface was grown by a thermal oxide. By applying fixed–fixed flexures shown in Fig. 5, the actuation voltages

**Table 1** The dimensions and design parameters of two types design

| Dimensions | $G/W/G$ (μm) | $S$ (μm) | $W_1$ (μm) | $W_{12}$ (μm) | $W_{11}$ (μm) | $C_L$ (fF) | |
|---|---|---|---|---|---|---|---|
| | | | | | | Up | Down |
| Unit cell 1 in the periodic design | 90/50/90 | 660 | 100 | 138 | 130 | 27.52 | 138.84 |
| Unit cell 2 in the aperiodic design | 110/50/110 | 630 | 135 | 98 | 190 | 33.52 | 153.14 |
| Unit cell 3 in the aperiodic design | 110/50/110 | 1,300 | 200 | 138 | 240 | 58.06 | 258.21 |

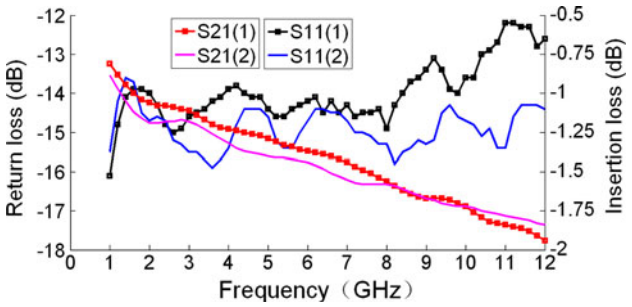


**Fig. 7** The average return loss and insertion loss in 32 unique phase states of the two 5-bit RF MEMS distributed phase shifters, the first is the aperiodic design and the second is the periodic design

simulated by ANSYS of the three types of unit cells are 30.1, 20.1 and 15.5 V, respectively.

We apply Agilent-ADS to do a circuit model parameters fitting on the two states respectively of the unit cells designed and optimized above and then do the simulation of RF characteristics of 5-bit distributed phase shifters by cascading the built circuit models. Figures 7 and 8 presented the average return loss, insertion loss and the phase shift of the two designed 5-bit RF MEMS distributed phase shifters, which are simulated by ADS. At 10 GHz, two phase shifters show the average insertion loss of −14.7 and −13.6 dB, the same return loss of −1.72 dB.

Based on the design parameters and the Eq. (8), the calculated $f_B$ of the two designs are above 18 and 35 GHz. For the aperiodic design, $f_B$ is calculated by the design parameters of the periodic part. To illustrate the effect of $f_B$, Fig. 9 shows the return loss and insertion loss of the two 5-bit RF MEMS distributed phase shifters when all MEMS bridges are actuated in down-state position, which are simulated by Ansoft HFSS. For the periodic design, below 30 GHz, the return loss and the insertion loss are better than −9.5 and −4 dB respectively. For the aperiodic design, below 16 GHz, the return loss and the insertion loss is better than −9.8 and −3 dB respectively. The linearity of phase shifts is also satisfactory. However, because of $f_B$, the performance of two designs will degrade sharply above 16 and 30 GHz.

MEMS distributed phase shifters are true time-delay phase shifters, whose phase steps increase linearly versus frequency. The RMS phase errors of the 5-bit distributed

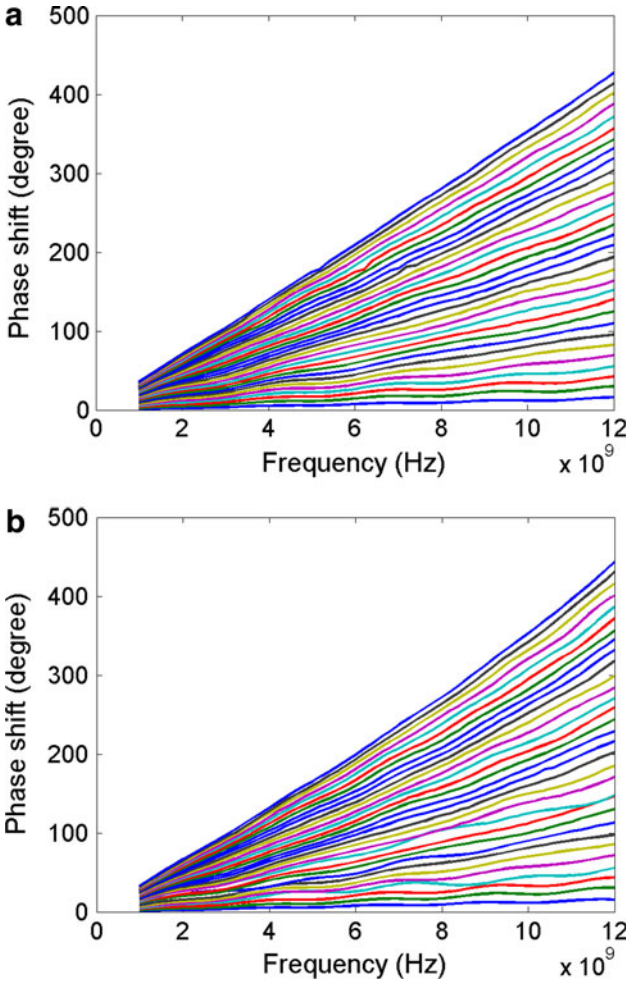


**Fig. 8** The phase shifts for 31 unique phase states (excluding the phase state of 0°) for the 5-bit MEMS phase shifter. **a** the periodic design, **b** the aperiodic design

phase shifters biased from the bit level and the unit cell level is presented in Fig. 10. The RMS phase error across all states at a given frequency point is based on:

$$\Delta\phi_{TTD.n} = \arg(S_{21.n}) - \left(\frac{f}{f_0}\right) \times \frac{360}{2^N} \times n \tag{9}$$

The average RMS phase errors of 1.23° and 1.85° in a 1-12-GHz bandwidth with 56 frequency points have been achieved.

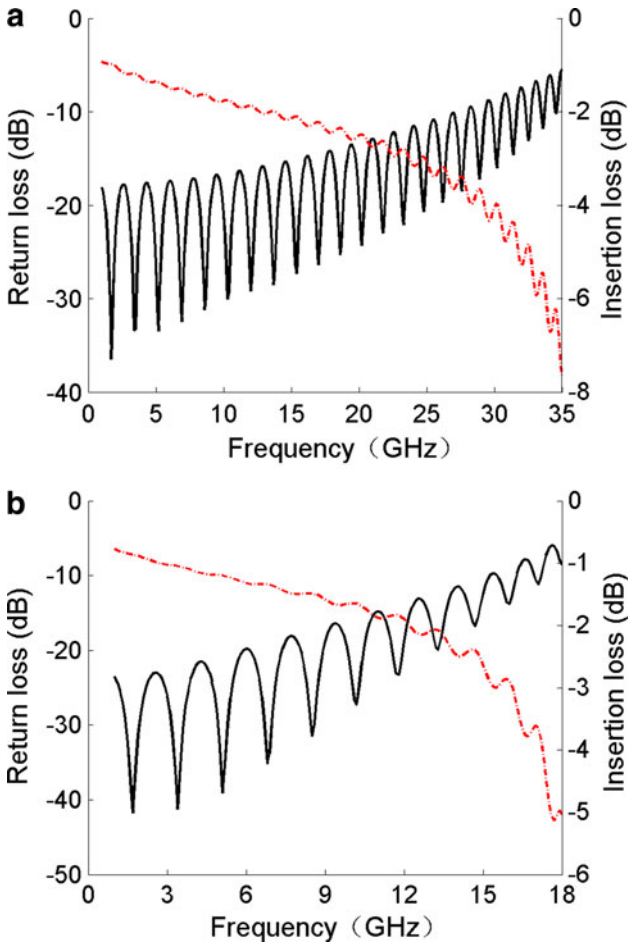


**Fig. 9** The return loss and insertion loss of 5-bit RF MEMS distributed phase shifters when all MEMS bridges are actuated in down-state position **a** the periodic design, **b** the aperiodic design

As seen, the periodic design with 31 same unit cells has better return loss and insertion loss compared with the aperiodic design. This is due to the loaded capacitance of the periodic design is smaller and therefore the discontinuity arisen by the loaded MEMS structure is weaker. The declined phase shift linearity of the aperiodic design will

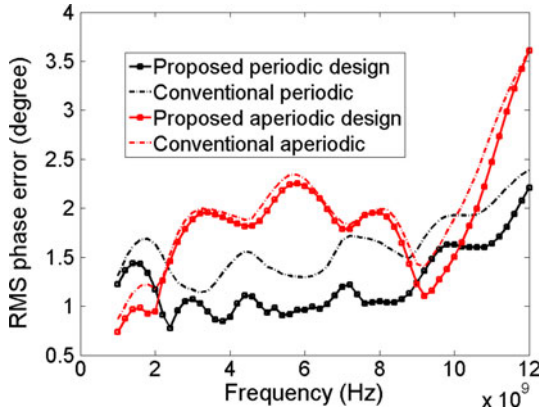


**Fig. 10** RMS phase error of 5-bit true time delay phase shifters

results in the narrower bandwidth, which is illustrated in the variation of RMS phase error. The reason is that, in the aperiodic design, to increase the phase shift of unit cell, the loaded capacitance becomes bigger and varies more evident according to the working frequency. The effect of the loaded capacitance value on the bandwidth should be considered in the wideband design. However, near the operation frequency of 10 GHz, the obvious reduction of RMS phase error is still observed.

Compared with traditional phase shifters controlled from the bit level with the same design parameters and the number of unit cells, the average phase errors in all phase states of the new type phase shifters are improved by 28.22 and 36.52 %, which can be reduced to 2.67° and 2.26° on average, while the relative phase errors are improved by 40.94 and 55.87 %, which can be reduced to 1.76 and 1.09 % on average. Besides the fact that the accuracy of phase shift is increased, both the average return loss and insertion loss are improved.

Table 2 summarizes the performance comparison of the distributed phase shifters with different concepts at 10 GHz as well as over the frequency from 1 to 12 GHz.

**Table 2** The performance comparison for the distributed phase shifters controlled from the bit level and the unit cell level

| | Conventional periodic design | Proposed periodic design | Conventional aperiodic design | Proposed aperiodic design |
|---|---|---|---|---|
| At 10 GHz | | | | |
| Average phase deviation | 3.72° | 2.67° | 3.56° | 2.26° |
| Average relative phase error | 2.98 % | 1.76 % | 2.47 % | 1.09 % |
| Average RL | −14.26 dB | −14.98 dB | −12.63 dB | −13.79 dB |
| Average IL | −1.91 dB | −1.70 dB | −1.92 dB | −1.71 dB |
| From 1 GHz to 12 GHz | | | | |
| Average RMS phase error | 1.61° | 1.23° | 1.99° | 1.85° |
| Contains 56 frequency point | | | | |
| Average phase deviation | 2.55° | 1.73° | 4.26° | 3.75° |

## 4 Conclusions

The new design of multi-bits MEMS distributed phase shifters for phase error reduction is presented. This design overcomes the conflict between mismatch of bits and the physical length since it is controlled from the unit cell level instead of the bit level. The obtained closed-form expression of phase shift could predict the diversified change of phase shift caused by the state change of adjacent bits. Two designing schemes of multi-bits distributed phase shifters are simulated to achieve average RMS phase errors of 1.23° and 1.85° in a 1–12-GHz bandwidth.

By using the proposed configuration, the phase error is improved greatly, so are the return loss and insertion loss. In addition, the aperiodic design of the phase shifter contains fewer switches, reducing the destabilized factors in the process and improving the rate of finished products of distributed phase shifters. The aperiodic phase shifter could be applied to increase the design flexibility, reduce the difficulty of the release of the sacrificial layer in the process, and save the fabrication costs of mass production.

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