Elektrotechnik & Informationstechnik (2021) 138/1: 31–36. https://doi.org/10.1007/s00502-020-00859-w

Microwatt power management: challenges of on-chip energy harvesting

S. Schmickl IEEE, T. Faseth IEEE, H. Pretl IEEE, OVE

IoT devices become more and more popular which implies a growing interest in easily maintainable and battery-independent power sources, as wires and batteries are unpractical in application scenarios where billions of devices get deployed. To keep the costs low and to achieve the smallest possible form factor, SoC implementations with integrated energy harvesting and power management units are a welcome innovation.

On-chip energy harvesting solutions are typically only capable of supplying power in the order of microwatts. A significant design challenge exists for the functional blocks of the IoT-SoC as well as for the power management unit itself as the harvested voltage has to be converted to a higher and more usable voltage. Simultaneously, the power management blocks have to be as efficient as possible with the lowest possible quiescent currents.

In this paper, we provide a look at on-chip microwatt power management. Starting with the energy-harvesting from RF power or light, we then show state-of-the-art implementations of ultra-low power voltage references and ultra-low power low-dropout regulator (LDO) designs.

Keywords: LDO; photovoltaics; power management; RF energy harvesting; ultra-low power

Microwatt Power Management: Herausforderungen bei On-Chip Energy Harvesting.

IoT-Geräte werden immer verbreiterter. Wachsendes Interesse gibt es dabei an einfach wartbaren und Batterie-unabhängigen Energiequellen, da Kabel und Batterien in Applikationen, wo Milliarden von Geräten in Einsatz sind, unpraktisch sind. Um die Kosten niedrig zu halten und den kleinstmöglichen Form-Faktor zu erreichen, sind SoC-Implementierungen mit integriertem Energy Harvesting und Power-Management-Blöcken eine willkommene Innovation.

On-Chip Energy Harvesting-Lösungen können typischerweise Energie nur in der Größenordnung von Microwatt liefern. Es existiert dadurch nicht nur eine große Design-Herausforderung für die funktionalen Blöcke des IoT-SoC, sondern auch für die Power-Management-Einheiten, da die gewonnene Energie oft in eine höhere und besser nutzbare Spannung konvertiert werden muss. Gleichzeitig müssen die Power-Management-Blöcke so effizient wie möglich sein und niedrigste Ruheströme vorweisen.

In dieser Arbeit geben wir einen Einblick in vollintegriertes (On-Chip) Microwatt Power Management. Beginnend bei Energy Harvesting von RF-Energie oder Licht, zeigen wir weiters aktuelle Implementierungen von Ultra-Low-Power-Spannungsreferenzen und Ultra-Low-Power-Low-Dropout-Spannungsreglern (LDO)s.

Schlüsselwörter: LDO; Photovoltaik; Power Management; RF Energy Harvesting; Ultra-Low Power

Received October 1, 2020, accepted November 23, 2020, published online December 4, 2020

1. Introduction

With a predicted number of more than nineteen billion short-range IoT devices in 2025 [3], there is also an upcoming challenge regarding the power supply of these devices. Many of them get deployed in areas without easily-accessible wired power-supplies, and a constant replacement of batteries becomes more and more unpractical and environmentally unfriendly with rising device counts. This trend is also visible in the road map of 6G, which also aims for zero-energy devices, e.g. for environmental monitoring, structural integrity monitoring, or pervasive industrial process monitoring [24]. Such batteryless devices also have the potential to save costs due to the lack of removable parts, which also enables smaller form factors and integration into non-accessible areas.

IoT devices cover a broad range of applications, implying also specialized silicon implementations for optimized performance in relatively low quantities, e.g. for specialized medical applications or environmental monitoring. At the same time, the goal is to aim for the lowest possible product costs which leads to the reasonable consequence that mature CMOS technology nodes (like 130 nm or 180 nm) should be chosen instead of the most advanced technologies to hold the NRE (non-recurring engineering) costs low for this many different specialized applications with low quantities.

To enable such zero-energy IoT devices, power-efficient designs of the functional blocks are required, but the real door openers are the energy-harvesting techniques and the accompanying power-management units to convert the harvested energy with the lowest possible losses into the required supply rails.

In Sect. 2.1 an overview of possible on-chip RF-energy harvesting options is provided. Following, in Sect. 2.2 on-chip photovoltaics options are shown, both with exemplary circuit implementations. Further, Sect. 3.2 will detail the design of an ultra-low-power low-

Schmickl, Stefan, Johannes Kepler University Linz, Energy-Efficient Analog Circuits & Systems, Altenberger Straße 69, 4040 Linz, Austria (E-mail: stefan.schmickl@jku.at); **Faseth, Thomas,** Johannes Kepler University Linz, Energy-Efficient Analog Circuits & Systems, Altenberger Straße 69, 4040 Linz, Austria; **Pretl, Harald,** Johannes Kepler University Linz, Energy-Efficient Analog Circuits & Systems, Altenberger Straße 69, 4040 Linz, Austria

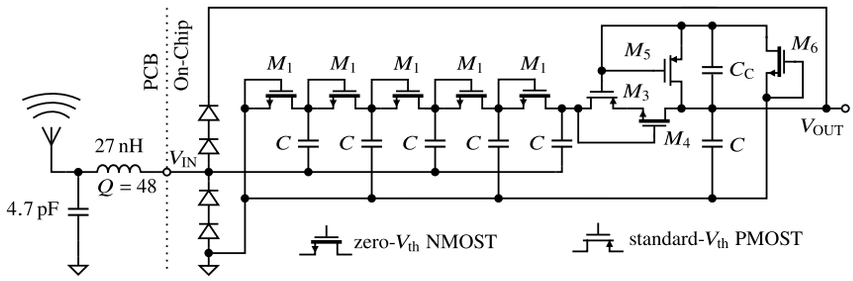

Fig. 1. Schematic of Dickson charge-pump based RF-energy harvester with zero-V_{th} MOSFETs and compensated ULPD as last stage [17], including matching network and chip-antenna [2]

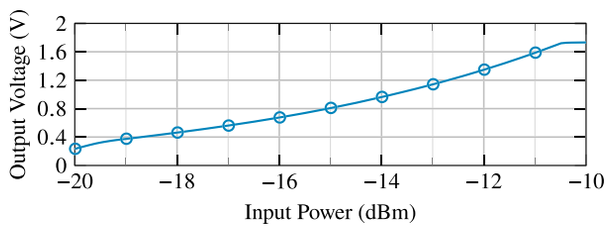

Fig. 2. DC output-voltage vs. RF input-power of RF-energy harvester with 330 kΩ load

dropout regulator and in Sect. 3.1 an ultra-low-power implementation of a reference voltage generation circuit is demonstrated.

In Sect. 4 we present an exemplary biomedical SoC which implements an RF-powered EEG sensor with wireless data transmission using most of the presented techniques. Finally, Sect. 5 summarizes and concludes the paper.

2. Energy-harvesting

Depending on the application and location of the IoT device, there are several energy sources available that can be harvested, e.g. motion with piezoelectric generators, heat differentials with thermoelectric generators, light with photovoltaic cells, or RF energy with RF-energy harvester. The focus of the following two sections is on the latter two, as they are of interest for a very wide spectrum of different applications.

2.1 RF-energy-harvesting

There are two possibilities to harvest incidental electromagnetic (EM) waves in the MHz- up to the GHz-range. First, the environmentally available EM waves, where the transmitter of the potential energy source could be located several kilometers away from the energy-harvesting system itself. In this case, the transmitter needs to have a very high RF output power in the range of kilo-watts, because of the strong decay of the EM far-field. In practice, this is best fulfilled by digital TV broadcast stations. Experimental tests show that it is possible to harvest 15 to 17 µW of power with the TV broadcast station 6.3 km away [23]. However, this test was carried out with a discrete RF charge-pump and a relatively large log-periodic antenna.

The other possibility is to use a dedicated local RF-power transmitter to energize several surrounding mobile nodes in a range of a few meters. The most practical frequencies are in the UHF ISM band (902 to 928 MHz) and the SRD band (863 to 870 MHz) because they give a good compromise between antenna size and path losses. These bands are available worldwide, and allow (at least) a maximum allowed transmitted power of 2 W ERP [4], which corresponds to a maximum available power at the receiving node of approx. 25 µW at a distance of 10 m [17].

For an on-chip RF-energy harvester, this means for both cases that the voltage level at the input is smaller than 100 mVpp (assuming 50 Ω antenna impedance), which has to be rectified and multiplied to a higher voltage level at the same time. The design challenge of such RF-to-DC rectifiers/voltage multipliers (RVMs) is to achieve the highest possible power conversion efficiency (PCE). In general, there are RVM topologies that use diodes or diode-connected transistors in differential full-wave [5, 26] or single-ended half-wave rectifiers [10, 16, 17]. Using Schottky diodes [11]—because of their lower turn-on voltage—is another possibility, but might not be available in a chosen technology. The main impact on the PCE are the threshold voltages of the used rectifying devices, which makes special compensating measures necessary. In [6] a static compensation scheme is shown which uses the higher voltage of the following stages for diode-connecting MOSFETs. While achieving good results, this method can't compensate the threshold voltage precisely. There also exist compensation techniques, which use auxiliary charge-pumps exactly subtracting the threshold voltage of the rectifying devices [15]. The more elaborate the compensation circuits get, the larger the parasitics become which degrade the PCE as well. Therefore, a promising approach is to use zero-V_{th} MOSFETs as rectifying device, keeping the circuit simple and rendering additional compensation measures unnecessary. A drawback is the large process sensitivity of this threshold voltage and therefore the risk of current back-flow due to the limited reverse isolation of the used MOSFETs, discharging the energy storage element. The work in [17] demonstrates how the concept of a simple zero-V_{th} 5-stage Dickson charge-pump can be combined with an ultra-low-power diode (ULPD) [9] in the last stage to effectively prevent current from flowing from the output buffer capacitor back into the circuit, as shown in Fig. 1. As in most technologies only n-type zero-V_{th} MOS-transistors exist, the PMOS in the ULPD is built with standard-V_{th} MOSFET, compensated with the principle of [15]. The implemented circuit is shown in Fig. 1 and is capable of generating 5 µW of dc power at 1.285 V output voltage from −12.3 dBm RF input power at a frequency of 868 MHz resulting in a PCE of 8.5% including matching losses. The associated plot of the dc output voltage versus the RF input power is shown in Fig. 2.

2.2 On-chip photovoltaic cell

Another interesting possibility to implement on-chip energy harvesting is the integration of a photovoltaic cell in a standard CMOS process. The idea is the same as with dedicated poly-silicon photovoltaic cells, namely a photo-diode with a relatively large area. Besides the theoretical solar-efficiency limit of 28.6% for crystalline sil-

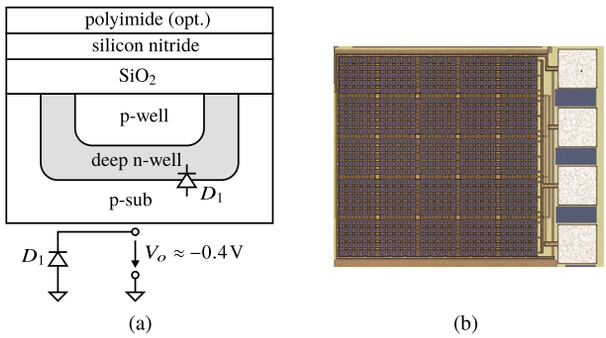

Fig. 3. On-chip photovoltaic cell in a triple-well CMOS technology; a) Stucture b) Micrograph

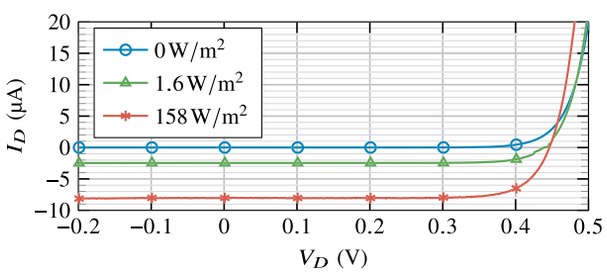

Fig. 4. Measured photo currents of photovoltaic cell at different light power levels at 300 K chip temperature

icon [14], in a standard CMOS process, more parameters (e.g. missing anti-reflective coatings and non-ideal doping concentrations) are sub-optimal for peak efficiencies. Additionally, the effective area of on-chip photovoltaic cells is comparatively small, and so the expectable power output under direct sunlight is in the order of microwatts.

In Fig. 3a the structure of a typical on-chip photovoltaic cell is shown. Theoretically, every p-n junction in a standard CMOS process can function as a photo-diode, but there are differences in efficiency. The absorption depth of light in silicon depends on the wavelength, which means that highly energetic ultraviolet and blue light gets absorbed near the surface, while lower energetic red and infrared light progresses into deeper regions. Theoretically, this would mean that shallow p-n junctions are able to harvest the most energy from the high energetic photons, but the crystal defects at the surface result in a higher recombination probability and therefore lost charge carriers. Therefore, the deeper p-n junctions tend to have higher efficiency, as has been shown in [21], and this also coincides with our own measurements. Figure 3b shows a photovoltaic cell fabricated in 180 nm CMOS, which implements the diode D_1 pictured in Fig. 3a between the p-substrate and a deep n-well. The cell consists of 25 unity cells with a total area of 0.267 mm^2 which is able to provide 2.78 µW of power at a voltage of −375 mV at direct sunlight on a sunny day (158 W/m^2) in its maximum power point, which results in an efficiency of 6.6% under this lighting conditions. Related works utilizing a comparable process in [8] and [1] report a maximum efficiency of 2.1% and 16.7% respectively, both measured with halogen light sources. The comparability is relatively difficult because of different spectral compositions of different light sources. Figure 4 shows the characteristic curve of the implemented photovoltaic cell under different levels of incident lighting. Thereby, the incident power of the sunlight was measured with a pyranometer. As the generated voltage is negative and too low for most on-chip

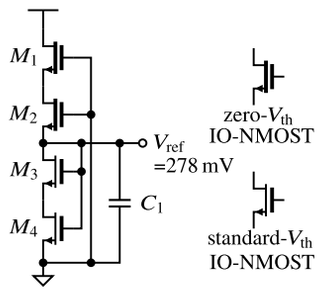

Fig. 5. Schematic of 2T-reference consuming 311 pA

applications, special charge-pump circuits are necessary, exemplary shown in the work of [21], as the diodes are not stackable, since the anode is tied to the common p-substrate.

3. Power management

Energy-harvesting solutions are not able to directly generate the needed voltage rails at exactly the time when the energy is required. The usual way is therefore to design the energy-harvesting system in a manner so that it generates a higher voltage than needed and stores it in an energy buffer. This buffer is—in most cases—too big for monolithic integration and has to be placed off-chip. Depending on the requirements, two buffer techniques are promising. Either a simple capacitor, which has the disadvantage of linear dependency between stored charge and voltage, can be used. Or, better yet, a rechargeable solid-state SMD battery (e.g. TDK CeraCharge™ [22]), available in small form factors and providing a capacity of 100 µA h while maintaining a battery-typical relatively constant voltage of ≈ 1.4 V, is a good fit for IoT applications. As the latter mentioned SMD battery has an internal resistance of ≈ 200 Ω, appropriate decoupling capacitors have to be used to buffer high peak-currents, e.g. from radio-transmitters. For many applications decoupling in the order of 100 pF is sufficient, which is possible to integrate on-chip.

The missing link in the power management is the energy-efficient regulation of the buffered, higher voltage to the constant application voltage. Consequently, an ultra-low-power, supply-voltage-independent reference voltage generator, and an ultra-low-power LDO or DC/DC-converter is needed. The latter one has as advantage the capability to use all the energy stored in the buffer-capacitor, while a LDO simply converts the excess voltage into heat. Drawback of DC/DC converters working at such low power levels is their poor conversion efficiency. To reach efficiencies > 60%, comparably complex and area consuming designs are necessary [7]. Additionally, the advantage of DC/DC-converter vanishes, when the voltage on the buffer-capacitor is near the regulated voltage, exactly the region, where highest efficiency is the most important. Therefore the following focus is on simple LDO designs.

3.1 Low-power voltage-reference design

The requirements of voltage-reference circuits for ultra-low-power IoT SoCs are quite challenging, as for many analog sensing applications a precise and stable voltage reference is inevitable. Most critical is the minimization of the consumed power, but also the line-regulation capabilities are very important, as the supply voltage from the energy buffer can vary substantially. Low noise and good temperature-stabilization are also desirable properties, but here compromises can be accepted depending on the specific use case, as, for instance, temperature compensation might not be as

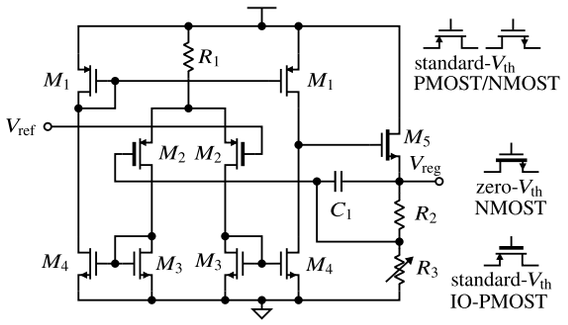

Fig. 6. Schematic of low-power LDO using native-V_{th} NMOS transistor as pass-device

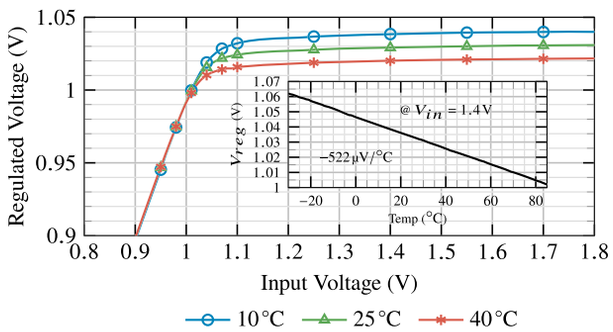

Fig. 7. Measured LDO output voltage at different temperatures

critical in body-worn devices because of rather constant body temperatures.

In [20] an ingenious circuit, named 2-Transistor (2T) voltage reference, has been shown, which has a 100× to 1000× better energy efficiency than other nanowatt voltage references, while offering a better line-sensitivity and temperature coefficient in less area, without the need of additional circuitry including operational amplifiers, biasing- or startup-circuits. Figure 5 shows an implementation of this 2T voltage reference circuit in 180 nm CMOS technology. M_1/M_2 and M_3/M_4 are series-connected maximum-length transistors, respectively. The functional principle is based on subthreshold-biased transistors with distinct V_{th} levels, in this case, a standard-V_{th} thick-oxide device (M_3/M_4) and a native-V_{th} thick-oxide device (M_1/M_2). C_1 is used for improving the noise performance. The implemented design uses 20 branches as shown in Fig. 5 in parallel to further improve the noise performance, with a total area of 0.027 mm^2 and consumes only 311 pA at a nominal voltage of 1 V, while the circuit is operable down to 0.4 V, determined by simulation as the voltage reference is not directly measurable, but only in combination with the LDO. The generated voltage is approx. 278 mV with a nominal line sensitivity of 28.4 µV/V, a temperature sensitivity of 1.67 µV/°C and an integral noise of 7.1 µV rms in 4096 Hz bandwidth.

An important note for this particular type of reference structure is to connect the generated reference voltage only to gates of thick-oxide devices, as the gate-leakage current of thin-oxide devices could disturb the reference because of its low quiescent current.

3.2 Low-power LDO design

Like the reference voltage generation circuits, also the voltage regulator circuits should be as power-efficient as possible for micro-watt energy harvesting SoCs. Interesting implementations are for example shown in [12, 13, 25]. The key for adequate performance with

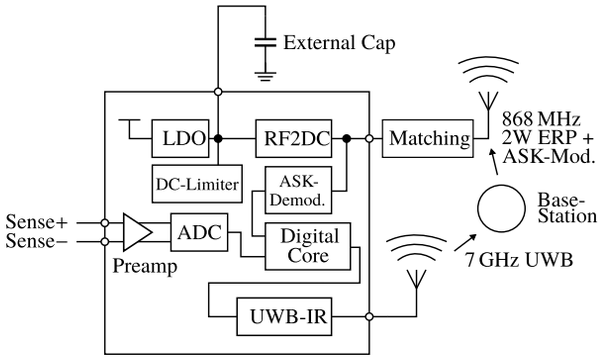

Fig. 8. Block diagram of bio-sensing SoC [17]

very-low power-drain is (again) simple circuit design and the avoidance of as much periphery as possible. Figure 6 shows an LDO circuit, implemented in 180 nm CMOS, consisting of a simple error amplifier in a symmetrical OTA topology, utilizing a 8.7 MΩ resistor for biasing and therefore avoiding separate bias current generation as there is no stable supply voltage available. Additionally, this biasing method offers a wide supply voltage range. At a nominal supply voltage of 1.2 V and a regulated output voltage of 1 V, the simulated current consumption of the error amplifier is 214 nA. Although the average power consumption of the application is very low, it surges high peak-currents, which implies requirements on the dynamic settling behavior and therefore requiring a certain gain and therefore current. The pass-transistor is realized by a native-V_{th} NMOS transistor, which is the best choice for this application case, as the NMOS offers a more stable behavior through the intrinsic load regulation of the pass-device itself. As an NMOS pass-device needs at least a drop-out voltage of V_{th}, a native type (with a threshold voltage close to zero) is chosen to ensure very low required drop-out voltages. The feedback resistors R_2 and R_3 are built out of 84 × 54 kΩ resistors in series where the bottom 20× resistors are digitally programmable with thermometer-coded shunt transistors, enabling an output voltage range of 0.74 to 1.42 V. Figure 7 shows the measured output voltage versus the input (supply) voltage with a constant 10 MΩ load at different temperatures and an output voltage versus temperature plot. The determined temperature coefficient is −522 µV/°C, equaling −502 ppm/°C. Compared to the value of [20] between 54 ppm/°C and 176 ppm/°C for their 180 nm 2T-reference our result is a bit worse, but it also contains the influence of the LDO. The line regulation is 7 mV/V, and the load regulation is 0.68 mV/µA.

4. Application example

As an exemplary application of the presented techniques an RF-powered, wireless EEG electrode is briefly discussed. This highly-integrated sensor SoC as shown in Fig. 8 and Fig. 9 is powered by the RF-harvester described in Sect. 2.1. The harvested energy is stored in an off-chip 10 µF-sized capacitor and further regulated to 1 V using the LDO presented in Sect. 3.2. Instead of a full-blown bandgap circuit the compact 2T reference voltage generator in Fig. 3.1 is used to stabilize the supply voltage. In this SoC a complete EEG signal acquisition system is realized, consisting of a pre-amplifier [19] and an ultra-low-power SAR ADC [18]. After decimation, the ADC data is protected by forward error correction and sent via an ultra-low-power impulse-radio ultra-wideband (IR-UWB) transmitter [17] with a data rate of 5.12 kbps using a double pulse interval coded alphabet. We could obtain an indoor range of ≈ 12 m with a custom built base-station. The whole system is intended to continuously operate without a battery, and fits into a

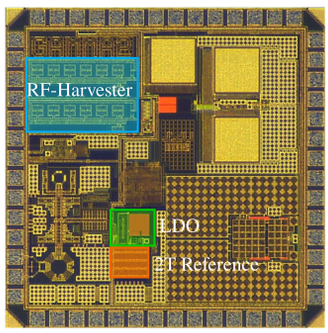

Fig. 9. Micrograph of bio-sensing SoC (1.6 × 1.6 mm^2)

power envelope of < 5 µW, enabling a buffer-time of ≈ 1.4 s assuming an usable buffer voltage overhead of 0.7 V. The shown SoC is demonstrating the potential of well-designed micro-watt power management.

5. Conclusion

This paper gives an overview of the challenges of on-chip power harvesting and power management and presents possible solutions. State-of-the-art examples in the different categories are given, complemented with own implementations. Finally, the interaction of the individual implemented blocks is shown exemplary with a wireless EEG electrode SoC.

Acknowledgements

The authors thank the Johannes Kepler University for funding the open access publication and EUROPRACTICE for access to IC design tools and fabrication.

Funding Note Open access funding provided by Johannes Kepler University Linz.

References

1. Chen, Z., Law, M., Mak, P., Martins, R. P. (2017): A single-chip solar energy harvesting IC using integrated photodiodes for biomedical implant applications. IEEE Trans. Biomed. Circuits Syst., 11(1), 44–53. https://doi.org/10.1109/TBCAS.2016.2553152.
2. Datasheet of ethertronics ISM 868 & 915 MHz Embedded Ceramic Antenna (2018): http://datasheets.avx.com/ethertronics/AVX-E_M620720.pdf.
3. Ericsson (2020): Ericsson Mobility Report, June 2020 . https://www.ericsson.com/en/mobility-report.
4. ETSI EN 302 208-1 Electromagnetic compatibility and Radio spectrum Matters (ERM) (2014): Radio Frequency Identification Equipment operating in the band 865 MHz to 868 MHz with power levels up to 2 W and in the band 915 MHz to 921 MHz with power levels up to 4 W
5. Ghovanloo, M., Atluri, S. (2008): An integrated full-wave CMOS rectifier with built-in back telemetry for RFID and implantable biomedical applications. IEEE Trans. Circuits Syst. I, Regul. Pap., 55(10), 3328–3334.
6. Hameed, Z., Moez, K. (2014): Hybrid forward and backward threshold-compensated RF-DC power converter for RF energy harvesting. IEEE J. Emerg. Sel. Top. Circuits Syst., 4(3), 335–343.
7. Jung, W., Gu, J., Myers, P. D., Shim, M., Jeong, S., Yang, K., Choi, M., Foo, Z., Bang, S., Oh, S., Sylvester, D., Blaauw, D. (2016): 8.5 A 60%-efficiency 20 nW-500 µW tri-output fully integrated power management unit with environmental adaptation and load-proportional biasing for IoT systems. In 2016 IEEE international solid-state circuits conference (ISSCC) (pp. 154–155). https://doi.org/10.1109/ISSCC.2016.7417953.
8. Law, M. K., Bermak, A. (2010): High-voltage generation with stacked photodiodes in standard CMOS process. IEEE Electron Device Lett., 31(12), 1425–1427. https://doi.org/10.1109/LED.2010.2075910.
9. Levacq, D., Liber, C., Dessard, V., Flandre, D. (2004): Composite ULP diode fabrication, modelling and applications in multi-Vth FD SOI CMOS technology. Solid-State Electron., 48(6), 1017–1025.
10. Li, C., Yu, M., Lin, H. (2017): A compact 0.9-/2.6-GHz dual-band RF energy harvester using SiP technique. IEEE Microw. Wirel. Compon. Lett., 27(7), 666–668.
11. Li, P., Bashirullah, R. (2007): A wireless power interface for rechargeable battery operated medical implants. IEEE Trans. Circuits Syst. II, Express Briefs, 54(10), 912–916.
12. Liu, C., Chen, C. (2013): An ultra-low power voltage regulator for RFID application. In Proc. IEEE 56th int. midwest symp. Circuits and systems (MWSCAS) (pp. 780–783).
13. Majidzadeh, V., Schmid, A., Leblebici, Y. (2009): A fully on-chip LDO voltage regulator for remotely powered cortical implants. In Proc. ESSCIRC 2009 (pp. 424–427).
14. Mertens, K. (2020): Photovoltaik Lehrbuch zu Grundlagen, Technologie und Praxis, 4 aktualisierte auflage edn. München: Carl Hanser Verlag GmbH & Co. KG.
15. Nakamoto, H., Yamazaki, D., Yamamoto, T., Kurata, H., Yamada, S., Mukaida, K., Ninomiya, T., Ohkawa, T., Masui, S., Gotoh, K. (2007): A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-µm technology. IEEE J. Solid-State Circuits, 42(1), 101–110.
16. Papotto, G., Carrara, F., Palmisano, G. (2011): A 90-nm CMOS threshold-compensated RF energy harvester. IEEE J. Solid-State Circuits, 46(9), 1985–1997.
17. Schmickl, S., Faseth, T., Pretl, H. (2020): An RF-energy harvester and IR-UWB transmitter for ultra-low-power battery-less biosensors. IEEE Trans. Circuits Syst. I, Regul. Pap., 67(5), 1459–1468.
18. Schmickl, S., Faseth, T., Pretl, H. (2020): An untrimmed 14-bit non-binary SAR-ADC using 0.37 fF-capacitors in 180 nm for 1.1 µW at 4 kS/s. In 2020 27th IEEE international conference on electronics, circuits and systems (ICECS). To be published.
19. Schmickl, S., Schumacher, T., Fath, P., Faseth, T., Pretl, H. (2020): A 350-nW low-noise amplifier with reduced flicker-noise for bio-signal acquisition. In 2020 austrochip workshop on microelectronics (austrochip) (pp. 9–12).
20. Seok, M., Kim, G., Blaauw, D., Sylvester, D. (2012): A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V. IEEE J. Solid-State Circuits, 47(10), 2534–2545.
21. Steffan, C., Greiner, P., Deutschmann, B., Kollegger, C., Holweg, G. (2015): Energy harvesting with on-chip solar cells and integrated DC/DC converter. In 2015 45th European solid state device research conference (ESSDERC) (pp. 142–145).
22. TDK CeraCharge™ solid-state SMD battery. https://www.tdk-electronics.tdk.com/en/ceracharge. Accessed 2020-09-27.
23. Vyas, R. J., Cook, B. B., Kawahara, Y., Tentzeris, M. M. (2013): E-WEHP: a batteryless embedded sensor-platform wirelessly powered from ambient digital-TV signals. IEEE Trans. Microw. Theory Tech., 61(6), 2491–2505.
24. Wikström, G., Peisa, J., Rugeland, P., Johansson, N., Parkvall, S., Girnyk, M., Mildh, G., Da Silva, I. L. (2020): Challenges and technologies for 6G. In 2020 2nd 6G wireless summit (6G SUMMIT) (pp. 1–5).
25. Wu, C., Lou, J., Deng, Z. (2018): An ultra-low power capacitor-less LDO for always-on domain in NB-IoT applications. In Proc. IEEE int. conf. applied system invention (ICASI) (pp. 137–140).
26. Zöscher, L., Herkess, P., Grosinger, J., Muehlmann, U., Amschl, D., Bösch, W. (2017): A differential threshold voltage compensated RF-DC power converter for RFID tag ICs. In 2017 integrated nonlinear microwave and millimetre-wave circuits workshop (INMMiC) (pp. 1–3).

Authors

Stefan Schmickl
was born in Linz, Austria 1990. He received the B.Sc. and M.Sc. degree in Electronics and Information Technology from the Johannes Kepler University (JKU) in Linz, Austria, in 2014 and 2016. His master thesis addressed the design of an integrated current-steering digital-analog converter. In October 2016 he joined the Institute for Integrated Circuits (IIC) at the Johannes Kepler University Linz working towards his Ph.D. degree. His current research focuses on ultra-low-power RF transceiver design, impulse-radio ultra-wide-band transmitter, RF-power-harvesting and ultra-low-power ADC-design for battery-less bio-sensing SoCs and wireless sensor networks for IoT applications. He is recipient of the 2019 ReSMiQ best paper award at the IEEE NEWCAS conference.

Thomas Faseth
received the Dipl.-Ing. (M. Sc.) and Dr. techn. (Ph.D.) degrees from the Vienna University of Technology in the years 2006 and 2012. His career started at the Institute of Electrodynamics, Microwave and Circuit Engineering in the year 2006. Since then he worked in the course of several research projects, especially with the main focus on RFID, localization methods, general RF measurement technology, switched power amplifiers, antenna measurements, as well as material and device characterization. From 2014 till 2016, he was the co-leader of the Microwave Engineering Group at the Institute of Electrodynamics, Microwave and Circuit Engineering at Vienna University of Technology in close cooperation with Asst. Prof. Dr. Holger Arthaber. Since 2016, Thomas Faseth is with the Institute for Integrated Circuits at Johannes Kepler University Linz and contributes to the Departments of Medical Electronics and Energy-Efficient Circuits and Systems Departments. He is author and co-author of about 30 publications.

Harald Pretl
was born in Linz, Austria, in 1972. He received the Dipl.-Ing. degree in electrical engineering from the Graz University of Technology, Austria, in 1997 and the Dr. techn. degree from the Johannes Kepler University (JKU) in Linz, Austria, in 2001, for his work on first-generation direct-conversion transceivers for 3G.
From 2000 to 2011 Dr. Pretl has worked at Infineon Technologies as Director and Senior Principal Engineer, and from 2011 to 2019 at Intel as Senior Principal Engineer contributing to several generations of cellular RF transceivers and mobile communications platforms, spanning from 2G to 5G, as analog circuit designer, project lead and RF systems architect. Since 2015 he is a full professor at the Institute for Integrated Circuits (IIC) at the JKU, Linz, where he is heading the Energy-Efficient Analog Circuits & Systems Group.
Harald Pretl was a member of the technical program committee (TPC) of the ISSCC in 2010 – 2012 and has published more than 50 papers at international conferences and journals in the area of RF transceivers and analog circuits, in addition to more than 25 issued and filed patents. His current research interests are focused on highly integrated GSM/UMTS/LTE/5G transceivers, integrated CMOS power amplifiers for mobile communications and IoT, wireless sensor networks and micro-power RF SoC. He is a co-recipient of the first place in the 2015 MTT-S PAWR student paper competition, the 2019 ReSMiQ best paper award at the IEEE NEWCAS conference, and the 2019 APMC student prize. He is also a co-recipient of the Intel Achievement Award in 2019. He is a member of the Austrian Electrotechnical Association (OVE).