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ORIGINAL ARTICLE

Design of tunnel FET architectures for low power application using improved Chimp optimizer algorithm

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Abstract

An improved Chimps optimizer algorithm is proposed in this paper and is applied for the performance optimization of tunnel FET architectures for use in low power VLSI circuits. The steep subthreshold characteristics of TFET improves device performance and make it suitable for low power digital and memory applications. Classical Chimps optimizer has poor convergence and problem to stuck into local minima for high dimensional problems. This research focuses on mathematical model of divergent thinking and sensual movement of chimps in four different forms named attacker, barrier, chaser, and driver for simulation. The improved variant of Chimps optimizer has been proposed in this research and named as Imp-Chimp. To validate the efficacy and feasibility of the suggested technique, it has been examined for standard benchmarks and multidisciplinary engineering design problems to solve non-convex, non-linear, and typical engineering design problems. The suggested technique variants have been evaluated for seven standard unimodal benchmark functions, six standard multi modal benchmark functions, ten standard fixed dimension benchmark functions and engineering design problems (i.e., TFET, BTBT). The outcomes of this method have been compared with other existing optimization methods considering convergence speed as well as for searching local and global optimal solutions. The testing results show the better performance of the proposed method. The paper also demonstrates the tunnel field effect transistor (TFET) as a promising device for low power electronic circuits and an engineering problem where the Imp-Chimp optimizer can be implemented for performance improvement. The TFET is based on the carrier generation using the quantum mechanical process of the band-to-band tunneling (BTBT). TFET can meet the requirements of a device that can perform on low supply voltage with reduced leakage currents and low sub-threshold swing. TFET can be optimized to give similar performance as MOSFET, but with much lower power consumption.

Keywords Tunnel FET · Narrow bandgap material · BTBT tunnelling · Improved Chimp optimizer · Heterojunction · Junction less TFET

1 Introduction

Artificial intelligence as well as machine learning are rapidly increasing because it is easy to implement to solve real-life issues which are continuous or discontinuous, constrained or unconstrained [1. , 2.]. For handling these characteristics using conventional approaches such as quasi-Newton method, sequential quadratic programming, fast steepest and conjugate gradient etc. faced difficulties to solve them [3. , 4.]. In existing research, all these methods were tested experimentally and noticed they are not exactly sufficient to obtain effectual solutions to non-continuous, non- differential problems and real life multi-model problems [5]. Thus, meta-heuristics algorithm came into picture which is very simple to understand and easily be implemented to handle several issues. Generally, in optimization, techniques depend on inhabitants to find out solution on optimal and sub optimal which is closer to exact optimal value, located at nearest point. In this algorithm the optimization process starts unless population set of the individuals are generated and then relaying on optimization method every individual

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act for candidate solution for the problem. Thus, by updating present location with best position, the population will be up to date by reaching maximum iterations. In modern research the meta-heuristics algorithm which gives better efficiency, less expensive and successful in implementation is given prior importance to utilize.

With such qualities embedded, a new hybrid meta-heuristics optimization technique, Imp-Chimp-SHO algorithm proposed in this paper relies on nature-lead and mathematical formulation of search functions were developed to give good competition to already existing meta-heuristics optimizers. The intention to design this optimization technique is motivated by individual intelligence and sensual movement of social carnivores, named Chimps for their mass hunting mannerism in targeting the prey [6]. Hence, a stochastic and meta-heuristic mathematical model intended to handle various optimization problems and is verified by testing experimentally in this research work.

It is a fact that Optimization technique is an extensive field of study and rapid progress in work is visualized as researchers are implementing new methods to give better solutions to various problems targeting challenges and can succeed in findings. In research, past methods ladder to new methods exhibiting their hybrid novel approach to reduce low efficient methods from present. A collection of research papers is presented in literature review to enlist the shortcomings of recent algorithms in this proposed study.

Broadly speaking meta-heuristics are of two types, named single-solution based m-heuristics and population solution based meta-heuristics. Improved Chimp algorithm (ICHIMP) variant belongs to swarm intelligence-based algorithm of the categories of population meta-heuristics, which is combined along with newly introduced swarm intelligence-based algorithm called Spotted Hyena Optimizer algorithm and named as Improved Chimp-Spotted Hyena Optimizer (ICHIMP-SHO) algorithm which is introduced in this paper. Overall, this algorithm is simple to apply and involves very less operators than other population-based algorithms with minimum computational efforts.

2 Literature review

Since few years meta-heuristics techniques came into usage widely because of its efficiency when compared to other existing techniques. These algorithms give better solution to real-life optimization issues. Hence, to solve these optimization issues there is a need of new meta-heuristics algorithm to introduce. As well in ever increasing utilization of engineering applications, meta-heuristics optimization algorithms (MOAs) have its importance. Very rapidly the necessity of latest MOAs is increasing because of solving complicated problems. It acquires distinct profits as: (i) Its plain algorithmic structure helps to implement it easily; (ii) This suits real-life problems in engineering as it is derivation-free mechanism; (iii) When compared to traditional optimization algorithms, this have better ability to minimize local optima; (iv)This is flexible to apply on different problems as its structure doesn't need any particular changes; (v) Because of its simplicity and efficiency, this can be applied simultaneously in hardware applications as well as in computing applications (like (FPGA)-field programmable gate array) [6]. To limit the drawbacks of classical methods, the meta-heuristics search algorithms were introduced. Few such algorithms are biography algorithm [7], artificial bee colony [8], differential evolution (DE) [9], genetic algorithm [10], cuckoo search algorithm [11], bacterial foraging algorithm [12], flower pollination algorithm [13], chemical reaction optimization [14], firefly algorithm [15], immune algorithm [16], teaching learning algorithm [17], particle swarm optimization algorithm (PSO) [18], grey wolf optimization [19], social spider algorithm [20], gravitational search algorithm [12], bat algorithm [21]. How meta-heuristics algorithms are classified is explained in [22, 23], and with reference to this [24, 25], meta-heuristics algorithms are considered by natural behaviour and divided as single solution based for example variable neighbourhood search [26], Vortex search algorithm (VS) [27], Simulated Annealing (SA) [28], genetic algorithm (GA) [10], Tabu search (TS) [29] is an emerging way to find solution for combinatorial real world problems in covering and scheduling, and cuckoo search algorithm [11], gravitational search algorithm (GSA) [12] are population-based algorithms. Evolutionary programming (EP) [30] is a fast and classical evolutionary programming's were performed on real world problems, generated a Gaussian random number rather than a Cauchy random number. Harmony search (HS) [31] is inspired by using music production cycle analogy. HS may not need the initial values of the variables for decision. Forest optimisation algorithm (FOA) [32] is for finding maximum value and minimal value with a real application, and found that the FOA can typically find solutions correctly and the reliability of the fruit fly swarm search route obviously has to do with the quantity of fruit fly. Grey wolf optimizer algorithm (GWO) [33] work was inspired by a Swarm intelligence optimization through the grey wolves and the suggested model imitated the grey wolves' social hierarchical and hunting behaviour. Moth flame optimizer (MFO) [34] here, key influence of this optimizer is the moth navigation system called transverse orientation in nature. Moths migrate in darkness by keeping a pre-set moon angle, a very effectual method for long distance flying in a straight line. But such fancy insects are stuck around artificial lights in a useless/deadly spiralling course. Stochastic Fractal Search Algorithm (SFS) [35] centred on random fractals to address global optimization problems with continuous variables,

both constrained and unconstrained. In the entire optimization if only one solution carries then it is known as single solution-based algorithm and if there are many different solutions in the whole optimization phase then it is population-based algorithm, and as such the solution may coincide to the optimum very nearly. Optimization problems can find solutions by nature inspired MOAs physical or biological behaviour implementation. They are classified into four main classes [24, 36]: swarm intelligence based algorithm, evolutionary algorithms (EAs), human-based, physics-based algorithms. Evolutionary algorithms replicate features of biological generation like recombining, mutation and selecting process [22]. The famous Evolutionary algorithms are differential evolution (DE) [37] presented the minimization of potentially nonlinear and non-differentiable continuous space functions. It only requires some strong control variables, taken from a perfectly-defined number interval, evolutionary strategy (ES), Biogeography-based optimization (BBO) [38] made analysis of biological species geographical distribution, can be used to deduce algorithms suitable for optimization. Evolutionary Programming (EP), and Genetic algorithm (GA) which is drawn from Darwinian theory. As per [36, 39] physics-based algorithms analogous natural physical laws. The famous algorithms are quantum mechanics based (QMBA), gravitational search (GSA) [40] is influenced by the Gravitational Law and the theory of mass interaction. GSA utilizes Newtonian mechanics theory, and its search agent is the set of masses, central force optimization (CFO), charged system search (CSS), electromagnetism like algorithms (ELA), lightning attachment procedure optimization (LAPO). Big-Bang Big-Crunch (BBBC) [41], adaptive best-mass gravitational search algorithm (ABMGSA) [42]. Thirdly, MOAs are inspired by natural human behaviour. The best examples of them are teaching learning based optimization (TLBO) [25] which comprises of 2 phases, teaching phase and learner phase to interact with both is possible with only tuning and the problem must be rectified in a power system, imperialist competitive algorithm (ICA) [43], socio evolution and learning optimization (SELO) [44]. Fourthly, MOAs imitate social behaviour of organisms like swarms, shoals, flocks or herds [45]. For illustration particle swarm optimization (PSO), hybrid MLP and Salp swarm algorithm (MLP-SSA) [46], bat algorithm (BA), ant colony optimization (ACO), improved monarch butterfly optimization (MBO) algorithm, cuckoo search algorithm (CSA), krill herd (KH) [47], grey wolf optimizer (GWO), Grasshopper optimization approaches, binary salp swarm algorithm (BSSA), ant lion optimizer (ALO) [48], hybrid binary, artificial bee colony (ABC), hybrid dragonfly optimization algorithm and MLP (DOA-MLP) [49], improved whale trainer (IWT) [50]. Harris Hawks optimizer (HHO) [51] is being introduced to tackle different tasks of optimization. The strategy is influenced by nature's cooperative activities and by the patterns of predatory birds chasing, Harris' hawks. Henry gas solubility optimization algorithm (HGSO) [52] imitates the procedures of Henry's rule. HGSO, aimed at matching the production and conservation capabilities of check room and stop optima local. Photon search algorithm (PSA) [40] Inspired by the properties of photons in the field of physics. Strong ability of global search and convergence. Chaotic krill herd algorithm (CKH) [53] combined chaos theory with Krill herd optimization procedure to speed up global convergence. Bird swarm algorithm (BSA) [54] depends on social interactions of swarm intelligence with bird swarm. Lightning search algorithm (LSA) [55] is a m-heuristic technique used to resolve problems on constraint optimization by following lightning phenomenon applying the concept of fast moving particles called projectiles. Multiverse optimizer (MVO) [56] a environment lead heuristic algorithm relays on 3 stages named: wormhole, black hole, white hole. Virus colony search (VCS) [57] is a environment inspired method that affects spreading and infection stages of the host cells followed by virus for its survival in the cell environment. To find solutions for real time problems, grasshopper optimization algorithm (GOA) [58] follows grasshopper swarms behaviour. Based on the thinking ability of chicken swarm, chicken swarm optimization algorithm (CSO) [59] came into existence. Grey wolf optimizer-sine cosine algorithm (GWO-SCA) [60] is a meta-heuristics optimizer correlating the nature of wolf with mathematical sine cosine concepts. crow particle swarm optimization algorithm (CPO) [61] is a hybrid combination of crow search algorithm and particle swarm optimization. Whale optimization technique (WOA) [62] is a hybridized combinatorial meta-heuristics technique of Whale and swarm human based optimizers for finding perfect exploratory and convergence capabilities. Spotted hyena optimizer (SHO) [63] is a new meta-heuristic algorithm encouraged by the natural collaborative behaviour of spotted hyenas in searching, encircling, attacking the prey. Multi-objective spotted hyena optimizer (MOSHO) [64] is developed to reduce multiple objective functions. Modified adaptive butterfly optimization algorithm (BOA) [65] is developed based on butterfly observation that produces its own fragrance when travelling in search of food from one place to another place. Binary spotted hyena optimizer (SHO) [66] is a meta-heuristic algorithm introduced on the basis of hunting behaviour of spotted hyena which deals with discrete optimization problems. Hybrid Harris Hawks pattern search algorithm (hHH-PS) [67] is a meta-heuristic optimizer developed to figure out newer version Harris Hawks for finding solution in local and global search. Hybrid Harris Hawks-sine cosine method (hHH-SCA) [68] is influenced by virtuous behaviour of Harris Hawks which added up with mathematical concepts of sine and cosine to increase its ability in exploration and exploitation phases (Fig. 1). Bernstrain-search differential

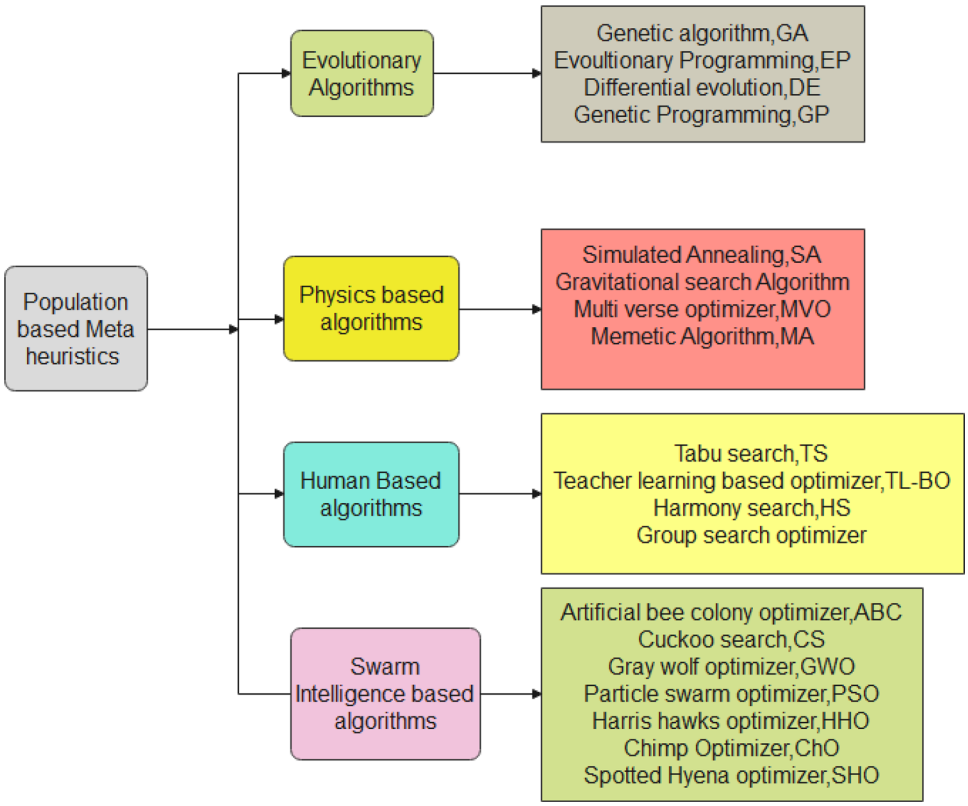


Fig. 1 Population based meta-heuristics classifications with few algorithms

evolution algorithm (EBSD) [69] belongs to family of universal differential evolution algorithms, which is proposed based on mutation and crossover operators. Reliability based design optimization algorithm (RBDO) [70] deals with the uncertainty factors like global convergence, complicated design variables. Basically the two main components of meta-heuristics are exploitation and exploration [24]. Exploration extends searching widely to produce many different solutions, whereas exploitation focuses searching in a specified area assuming that area is the best for present. It is very much important and necessary to balance these two components exploitation and exploration in MOA to keep away the fluctuations in the rate of convergence, as well preventing local and global optimum [71, 72]. Exploitation indicates single solution based meta-heuristics and exploration indicates populated solution based meta-heuristics.

Spotted Hyena optimizer (SHO) is a new upcoming optimizer influenced by the trapping behaviour of spotted hyena. This technique benefits upon other meta-heuristics as:

(i) implementation of algorithm is easy because of its simplicity structure.
(ii) it makes smooth continuous solutions in local optimum.
(iii) it has finer local and global search capability.
(iv) due to continued diminution of search space, SHO convergence rate ids faster. And this solves many types of engineering design problems [66].

Data mining feature selection and unit commitments are the major discrete optimization issues. To solve these problems SHO is used. Feature selection targets unnecessary features and removes them from data set and minimizes computation requirement, dimensionality and results in better accuracy. In practical, the real-time problems may have huge number of features with relevant and irrelevant features. At that time, it is difficult for finding solution. Then, the characteristic selection is treated as combinatorial optimization problem. To solve this selection feature problem binary meta-heuristics algorithms are used. Few examples are binary gravitational search algorithm (BGSA) [73], binary gray wolf optimizer (BGWO) [74], binary bat algorithm (BBA) [75, 76], binary particle swarm optimization (BPSO) [77]. Hybrid particle swarm and spotted hyena optimizer algorithm (HPSSHO) [78] is a novel meta-heuristic algorithm developed to improve convergence speed. Chimp optimization algorithm (ChoA) [6] is designed based on intelligence ability of Chimps in group hunt. This algorithm is developed to solve slow convergence speed, trapping in high-dimensional problems.

A task towards identifying solutions throughout issues for optimization is a hot theme. Is if range of optimization parameters keeps increasing, its sophistication of the optimization problems will be enormous. In addition, several deterministic proposed methods are subject to local optima trapping. The meta-heuristic (MA) nature-inspired optimization techniques are designed to overcome such problems (Table 1). The major elements with these methodologies are

population dependence and the absence of initial assumptions. Even so, there's really no optimization technique that can fix yet all optimization issues [79]. This thought initiated to propose a meta-heuristic hybrid variant optimizer named as improved chimp-spotted hyena optimizer (ICHIMP-SHO). It is tested on seven standard unimodal benchmark functions, six standard multi model benchmark functions, ten standard fixed dimension benchmark functions and eleven types of multidisciplinary engineering design problems. The results noticed are excellent than other existing algorithms.

The remaining part of present article contains concepts of improved chimp optimizer (IChimp) algorithm, spotted hyena optimizer (SHO) algorithm, proposed IChimp-SHO algorithm, standard benchmark functions, engineering-based optimization design problems, numerical results and discussions, outcomes of proposed algorithm, conclusion.

3 Proposed improved chimp optimizer

Chimps hunt very cleverly remembering the previous track of their attacks and are very closely related to swarm intelligence strategy and based on this behaviour a innovative algorithm known as Chimp Optimization Algorithm (ChoA) is introduced. Chimps hunt in a group very intelligently based on two phases namely exploration and exploitation. Chimps are divided into four parties specifically named as driver, barrier, chaser, and attacker. They streamline themselves by chasing, driving, blocking, and attacking in trapping the prey.

The mathematical Eqs. (1) and (2) represents driving and chasing of the prey.

$$\vec{D} = \left|\vec{C}\vec{Y}_{\text{Prey}}(\text{iteration}) - \xi \cdot \vec{Y}_{\text{Chimp}}(\text{iteration})\right|, \tag{1}$$

$$\vec{Y}_{\text{Chimp}}(\text{iteration}+1) = \vec{Q}_k + \vec{Y}_{\text{Prey}}(\text{iteration}) - \vec{A} \cdot \vec{D}. \tag{2}$$

Here, $\vec{A}$, ξ, and $\vec{C}$ is the coefficient vectors, t is the number of current iterations, Chimp location vector is the $\vec{Y}_{\text{Chimp}}$, and $\vec{Y}_{\text{Prey}}$ is the vector of prey position.

Coefficient vectors $\vec{A}$, ξ, and $\vec{C}$ are found out using Eqs. (5)–(7).

In the improved chimp optimizer, the Eqs. (1) and (2) has been modified as follows:

$$\vec{Y}_{\text{Chimp}}(\text{iteration}+1) = \begin{cases} \vec{Y}_{\text{Prey}}(\text{iteration}) - \vec{A} \cdot \vec{D} & \text{if } \xi < 0.5 \\ \text{Chaotic\_value} & \text{if } \xi > 0.5 \end{cases}, \tag{3}$$

where ran (1) and ran (5) represents the random integer values and can be given by the following mathematical equation:

$$\text{ran(index)} = \text{randi}([1,\ \text{SAN}], 1, 3), \tag{4}$$

where SAN represents the search agent number.

$$\vec{A} = 2\vec{\eta}\nu_1 - \vec{\eta}, \tag{5}$$

$$\vec{C} = 2\nu_2, \tag{6}$$

$$\xi = \text{chaotic vector}, \tag{7}$$

$$x_{i+1} = 1.07x_i(7.86x_i - 23.31x_i^2 + 28.75x_i^3 - 13.302875x_i^4). \tag{8}$$

$\left|\vec{A}\right|$ non-linearly decreases from 2.5 to 0 in both the phases iteratively. The vectors ν_1 and ν_2 are ranged [1.]. ξ the chaotic vector serves chimps in the process of trapping.

In this hunting process usually an attacker chimp leads this operation followed by driver, barrier, and chaser. Mathematically the actions of Chimps are imitated in the sequence initially starting from attacker, driver and then barrier; chaser will give better lead to notice the position of prey. Up till now the location of Chimps is to be updated immediately and store the best positions of Chimps.

This process is reflected mathematically in the Eqs. (9)–(21).

$$\vec{D}_{\text{Attacker}} = \text{abs}\left|\vec{C}_1\vec{Y}_{\text{Attacker}} - \vec{Y}\right|. \tag{9}$$

In the modify chimp algorithm, the $\vec{D}_{\text{Attacker}}$ has been selected with the help of following equation:

$$\vec{D}_{\text{Attacker}} = \begin{cases} \left|\vec{C}\vec{Y}_{\text{Attacker}}(\text{iteration}) - \xi \cdot \vec{Y}(\text{iteration})\right| ;\ |A| < 1 \\ \left|\vec{C}\vec{Y}_{\text{Attacker}}(\text{ran}(1),\text{iteration}) - \xi \cdot \vec{Y}(\text{ran}(3),\text{iteration})\right| ;\ |A| > 1 \end{cases}, \tag{10}$$

$$\vec{D}_{\text{Barrier}} = \text{abs}\left|\vec{C}_2\vec{Y}_{\text{Barrier}} - \vec{Y}\right|. \tag{11}$$

In the modify chimp algorithm, the $\vec{D}_{\text{Barrier}}$ has been selected with the help of following equation:

$$\vec{D}_{\text{Barrier}} = \begin{cases} \left|\vec{C}\vec{Y}_{\text{Barrier}}(\text{iteration}) - \xi \cdot \vec{Y}(\text{iteration})\right| ;\ |A| < 1 \\ \left|\vec{C}\vec{Y}_{\text{Barrier}}(\text{ran}(1),\text{iteration}) - \xi \cdot \vec{Y}(\text{ran}(3),\text{iteration})\right| ;\ |A| > 1 \end{cases}, \tag{12}$$

$$\vec{D}_{\text{Chaser}} = \text{abs}\left|\vec{C}_3\vec{Y}_{\text{Chaser}} - \vec{Y}\right|. \tag{13}$$

In the modify chimp algorithm, the $\vec{D}_{Chaser}$ has been selected with the help of following equation:

$$\vec{D}_{\text{Chaser}} = \begin{cases} \left|\vec{C}\vec{Y}_{\text{Chaser}}(\text{iteration}) - \xi \cdot \vec{Y}(\text{iteration})\right| ;\ |A| < 1 \\ \left|\vec{C}\vec{Y}_{\text{Chaser}}(ran(1), iteration) - \xi \cdot \vec{Y}(\text{ran}(3),\text{iteration})\right| ;\ |A| > 1 \end{cases}, \tag{14}$$

```
PSEUDO Code for calculation of Y1
r1=rand ();
    r2=rand ();
    A1=2*a*r1-a;
    C1=2*r2;
   if abs (A1)<1
      D_Attacker=abs (C1*Y_Attacker (j)-Y (i, j));
  else
      D_Attacker=abs (C1*Y (rand_num (1), j)-Y (rand_num (3), j)
    If rand>CR
     D_Attacker=Y_Attacker(j)
   end
end
Y1=Y_Attacker(j)-A1*D_Attacker;
```

```
PSEUDO Code for calculation of Y2
r1=rand ();
    r2=rand ();
    A2=2*a*r1-a;
    C2=2*r2;
   if abs (A2)<1
      D_Attacker=abs (C2*Y_Barrier (j)-Y (i, j));
  else
      D_Barrier=abs (C1*Y (rand_num (1), j)-Y(rand_num(3),j)
    If rand>CR
     D_Barrier=Y_Barrier(j)
   end
end
Y2=Y_Barrier(j)-A2*D_Barrier;
```

(a) PSEUDO Code for Calculation of Y1 and Y2

```
PSEUDO Code for calculation of Y3
r1=rand ();
    r2=rand ();
    A3=2*a*r1-a;
    C3=2*r2;
   if abs (A3) <1
      D_Chaser=abs (C3*Y_Chaser (j)-Y (i, j));
  else
      D_Chaser=abs (C3*Y (rand_num (3), j)-Y (rand_num (2),j)
    If rand>CR
     D_Chaser=Y_Chaser(j);
   end
end

Y3=Y_Chaser(j)-A3*D_Chaser;
```

```
PSEUDO Code for calculation of Y4
r1=rand ();
    r2=rand ();
    A4=2*a*r1-a;
    C4=2*r2;
   if abs (A4) <1
      D_Driver=abs (C4*Y_Driver (j)-Y (i, j));
  else
      D_Driver=abs (C4*Y (rand_num (4), j)-Y (rand_num (1),j)
    If rand>CR
     D_Driver=Y_Driver(j);
   end
end
Y4=Y_Driver(j)-A4*D_Driver;
```

(b) PSEUDO Code for Calculation of Y3 and Y4

Fig. 2 **a** PSEUDO code for calculation of Y1 and Y2. **b** PSEUDO code for calculation of Y3 and Y4

$$\vec{D}_{Driver} = abs\left|\vec{C}_4\vec{Y}_{Driver} - \vec{Y}\right| \tag{15}$$

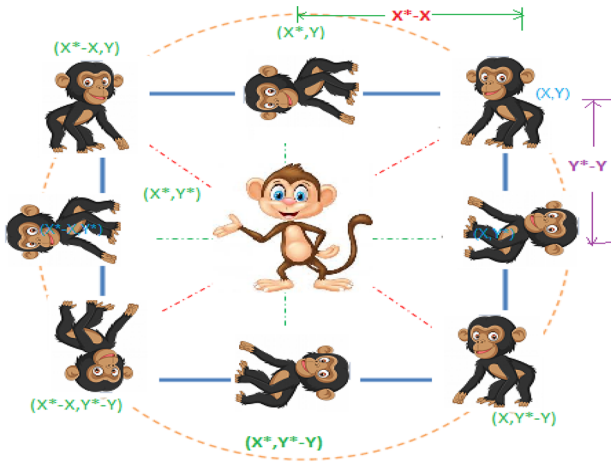
In the modify chimp algorithm, the $\vec{D}_{Driver}$ has been selected with the help of following equation:

$$\vec{D}_{\text{Driver}} = \begin{cases} \left|\vec{C}\vec{Y}_{\text{Driver}}(\text{iteration}) - \xi \cdot \vec{Y}(\text{iteration})\right| ; & |A| < 1 \\ \left|\vec{C}\vec{Y}_{\text{Driver}}(\text{ran}(1),\text{iteration}) - \xi \cdot \vec{Y}(\text{ran}(3),\text{iteration})\right| ; & |A| > 1 \end{cases} . \tag{16}$$

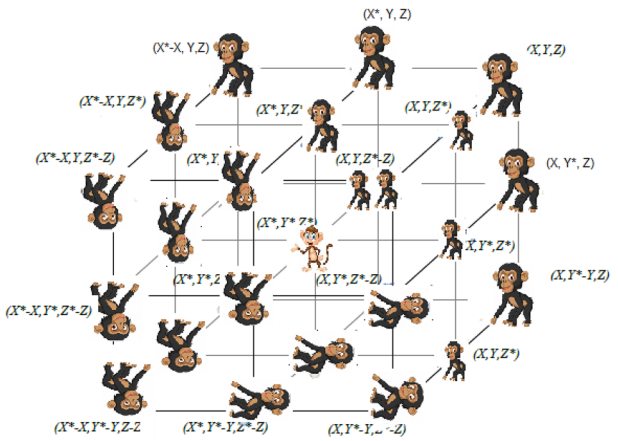
The Eq. (2) mentioned above can be used to determine the spot of attacker, barrier, chaser and driver as per Eqs. (17)–(20) respectively.

$$\vec{Y}_1 = \vec{Y}_{\text{Attacker}} - \vec{A}_1 \cdot \vec{D}_{\text{Attacker}}, \tag{17}$$

$$\vec{Y}_2 = \vec{Y}_{\text{Barrier}} - \vec{A}_2 \cdot \vec{D}_{\text{Barrier}}, \tag{18}$$



(a) 2D view for the Position of Prey and Chimp



(b) 3D view for the Position of Prey and Chimp

Fig. 3 **a** 2D view for the position of prey and chimp. **b** 3D view for the position of prey and chimp. **c** Flow chart of proposed ICHIMP-SHO algorithm

$$\vec{Y}_3 = \vec{Y}_{\text{Chaser}} - \vec{A}_3 \cdot \vec{D}_{\text{Chaser}}, \tag{19}$$

$$\vec{Y}_4 = \vec{Y}_{\text{Driver}} - \vec{A}_4 \cdot \vec{D}_{\text{Driver}}. \tag{20}$$

The overall final positions of all the chimps can be obtained by taking the mean of the attacker, barrier, chaser and driver positions as per Eq. (21):

$$\vec{Y}(\text{iteration}+1) = \frac{(\vec{Y}_1 + \vec{Y}_2 + \vec{Y}_3 + \vec{Y}_4)}{4}. \tag{21}$$

The 2-dimensional and three-dimensional view for the position of chimp from the respective prey has been depicted in Fig. 3a, b, respectively.

To generate the initial arbitrary position of search agents, the below mathematical equation can be adopted:

$$\vec{Y}_{\text{rand}} = LB_i + \xi \times (UB_i - LB_i)\,;\ i \in 1, 2, 3, \ldots, \text{Dim}\,. \tag{22}$$

The PSEUDO Code for calculations of Y_1, Y_2, Y_3 and Y_4 are given in Fig. 2a, b.

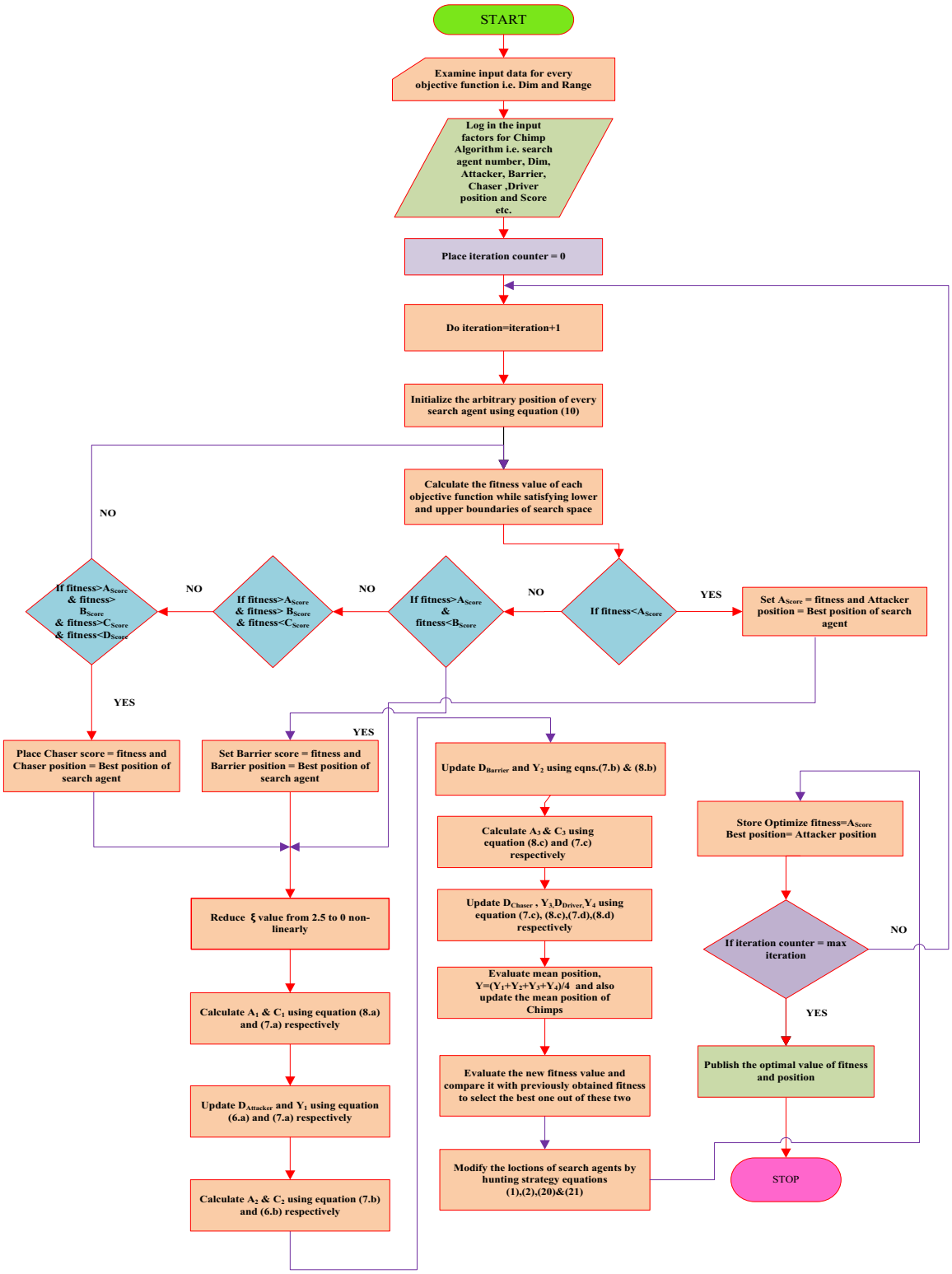
This work extends an enhanced version of hunting behaviour of Improved Chimp optimizer by means of spotted hyena as depicted in Fig. 3c. To experience this consequence, the driving and chasing Eqs. (1) and (2) of I-Chimp along with hunting behaviour of spotted hyena in Eq. (19) are considered to modify into Eq. (23). The pseudo code for the suggested ICHIMP-SHO algorithm is discussed in Algorithm 1.

$$\vec{Y}_{\text{Chimp}}(\text{iteration}+1) = \vec{Q}_k + \vec{Y}_{\text{Prey}}(\text{iteration}) - \vec{A} \cdot \vec{D}. \tag{23}$$

PSEUDO code of Improved Chimp Algorithm

Algorithm 1: Imp-Chimp algorithm

Initialize the Chimp population x_{i+1} *(i=1, 2… n)*
Initialize $\vec{\eta}$ **,** ξ **,** $\vec{A}$ ***and*** $\vec{C}$
Calculate the position of each chimp
Divide chimps randomly into independent groups
Until *stopping condition is satisfied*
Calculate the fitness of each chimp
$\boldsymbol{X}_{Attacker}$*=the best search agent*
$\boldsymbol{X}_{Chaser}$*=the second-best search agent*
$\boldsymbol{X}_{Barrier}$*=the third best search agent*
$\boldsymbol{X}_{Driver}$*=the fourth best search agent*
while *(t <maximum number of iterations)*
for *each chimp:*
Extract the chimp's group
Use its group strategy to update $\vec{\eta}$ **,** ξ ***and*** $\vec{C}$
Use $\vec{\eta}$ *,* ξ *and* $\vec{C}$ *to calculate* $\vec{A}$ *and then* $\vec{D}$
Calculate Y1 and Y2 using Pseudo Code of Fig.2(a)
Calculate Y3 and Y4 using Pseudo Code of Fig.2 (b)
Calculate Y=(Y1+Y2+Y3+Y4)/4
Update $\vec{\eta}$ **,** ξ **,** $\vec{A}$ ***and*** $\vec{C}$
Update $\boldsymbol{X}_{Attacker}$ **,** $\boldsymbol{X}_{Driver}$ **,** $\boldsymbol{X}_{Barrier}$**,** $\boldsymbol{X}_{Chaser}$
I=I+1
end while
return $\boldsymbol{X}_{Attacker}$



(c) Flow Chart of proposed ICHIMP-SHO Algorithm

Fig. 3 (continued)

4 Standard benchmark functions

A cluster of different benchmark functions [30, 83] is taken to test the efficacy of the proposed ICHIMP-SHO optimization technique. Such benchmark collection is composed of three major benchmark feature classes, such as uni-modal (UM), multimodal (MM) and fixed dimensions (FD) standard benchmarks. UM, MM, FD mathematical formulations are shown in Tables 2, 3, 4, 5 and their characteristics are shown in outcomes and discussion section. For verifying standard benchmark functions performance 30 trail runs are considered.

Thirty search agents are considered in the entire research analysis, and the suggested technique is simulated for maximum 500 iterations. The ICHIMP-SHO algorithm developed was verified on Intel ® Core TM, i7-5600 CPU@2.60 GHz.

5 Results and discussions

In this research work, the introduced improved chimp-spotted hyena optimizer algorithm is tested on three major classes of standard benchmark functions to verify the presentation of the developed ICHIMP-SHO technique. The exploitation and convergence rate of ICHIMP-SHO is tested by unimodal benchmark functions which has single minimum. As the name multimodal replicates which has more than one minimum, hence these functions are utilized to test for exploration and avoid local optimum. The design variables are obtained by the difference between multimodal and fixed dimension benchmark functions. The fixed dimension benchmark functions will store these design variables and maintain a chart of previous data of search space and compares with multimodal benchmark functions.

For comprehensive comparison analysis, a record of results of developed ICHIMP-SHO algorithm were framed which were tabulated in the criteria of mean value, standard deviation, median value, best value, worst value, and parametric tests by performing with 500 iterations and maximum runs of 30.

5.1 Evaluation of (F1–F7) functions (exploitation)

The test results for unimodal (F1–F7) benchmark functions of suggested technique were illustrated in the Tables 6, 7. The mean value, standard deviation were considered for evaluation of the test results with few newly developed metaheuristic algorithms named LSA [55], BRO [84], OEGWO [85], PSA [40], hHHO-PS [67], SHO [63], HHO [51], ECSA [86], TSO [87] and presented in Table 8. Its characteristic curves, trail runs, convergence comparative curves with other algorithms were depicted in Figs. 4, 5, 6.

5.2 Evaluation of (F8–F13) functions (exploration)

The multimodal benchmark functions (F8–F13) show the design variables in desired number in the exploration phase. The test results were tabulated in Tables 9, 10. As well the comparison of results were done with respect of mean value and standard deviation with other algorithms LSA [55], BRO [84], OEGWO [85], PSA [40], hHHO-PS [67], SHO [63], HHO [51], ECSA [86], TSO [87] and recorded in Table 11. Also its characteristics curves, trail runs, convergence comparative curves with other algorithms were depicted in Figs. 7, 8, 9.

5.3 Evaluation of (F14–F23) functions

The fixed dimensional benchmark (F14–F23) functions do not manipulate the design variables but prepares the previous search space record of multimodal benchmark functions. Tables 12, 13 are the test results of proposed algorithm and Table 14 showcases the comparative analysis of mean value and standard deviation with LSA [55], ECSA [86], TSO [87], PSA [40], hHHO-PS [67], SHO [63], HHO [51]. Figures 10, 11, 12 shows characteristics curves, trail runs, convergence comparative curves with other algorithms.

Hence, the test results for UM, MM and FD benchmarks problems are tabled in Tables 6, 7, 8, 9, 10, 11, 12, 13, 14 and the assessment of proposed optimizer with other metaheuristics search algorithms for UM, MM and FD benchmarks problems has been given in Figs. 5, 8 and 11 and trail runs solutions for UM, MM and FD benchmarks problems has been shown in Figs. 6, 9, and 12. The above result clearly shows that proposed optimizer presents much better than other algorithms. In sub-sequent sections, the proposed optimizers have been applied to 11 engineering optimizations problems.

6 Engineering design problem

As computing is having a paradigm shift from large desktop devices to battery operated, hand-held or implantable mobile devices the demand for low power electronics is growing more and more. Despite having many superior properties like high input impedance, voltage control, unipolarity, better thermal stability, high switching speed, less noise etc., the most important reason for the widespread popularity of MOSFET, is its comparatively small dimensions and easy scalability. Reduction in the length of MOS devices has many benefits like increased number per chip or high packing density, smaller gate length means smaller gate capacitance and thus high switching speed. Length scaling also leads to voltage scaling of MOSFETs and which in turn results in minimization of power consumption, which makes

it a desirable device for low power electronics [88]. However, as the dimensions are scaled further and further, controlling the OFF-state power consumption became a major challenge for MOS devices. The drain current in MOSFET flows due to the thermionic injection of charge carriers from source to channel. With the increase in gate voltage, the barrier potential between the source and the channel reduces, which leads to an increase in the drain current and gives rise to a larger OFF-state current because of subthreshold conduction and an increase in subthreshold slope. For a MOSFET the subthreshold slope may be defined as the amount gate voltage V_{GS} required to change the drain current I_D ten folds. Subthreshold slope (SS) should be as small as possible because lower SS results in a higher difference between ON and OFF state currents, thus a larger I_{ON}/I_{OFF} ratio and lesser power dissipation at the OFF state. Mathematically the subthreshold slope of MOSFET is represented as:

$$SS = \frac{dV_g}{d(\log I_d)} = \frac{kT}{q}\ln 10\left(1 + \frac{C_D}{C_{ox}}\right) \tag{24}$$

where C_D and C_{ox} are depletion and oxide capacitances of the device, respectively. From Eq. (24) the minimum possible value of SS for a MOSFET is $\frac{kT}{q}\ln 10$, which comes out to be 60 mV/dec at room temperature of 300 K. Therefore, to get an I_{ON}/I_{OFF} ratio of 10^6, we must apply a gate voltage of 6×60 mV = 0. 36 V. Thus, it would not be possible to achieve a high I_{ON}/I_{OFF} ratio without sacrificing the supply voltage scaling. These basic disadvantages of MOSFET of higher OFF state currents and high subthreshold slope limit their application in low power circuits.

A device prone to these fundamental limitations of MOSFET is the prime requirement now. One such device is the tunnel field effect transistor or TFET. It can provide the solution by controlling the BTBT tunnelling phenomenon and making it the source of drive current in place of thermionic emissions in MOS devices. Structurally TFET is very similar to MOSFET, except that the source and drain here are having opposite doping. This similarity makes TFET very much compatible with MOSFET based circuits. TFETs are found to be immune to various short channel effects which is a major limitation for MOS devices [89]. TFETs are gate-controlled, reverse-biased P–I–N diodes in which the tunnelling current is controlled by the gate voltage [90]. In TFETs steep subthreshold slope lower than 60 mV/dec can be achieved because they are not bound by kT/q, which is the fundamental limit for MOSFETs, which has also been experimentally proved [91]. The energy requirements of TFET to switch between states is also much lower than MOSFET making them better switches compared to MOSFET [92, 93]. TFETs also have very low OFF-state current and high stability to temperature variations because it relies on BTBT tunneling rather than thermionic emissions for device conduction making it one of the finest candidates for low power electronic circuits. Due to low OFF-state current, steep SS and high output resistance, SiGe source TFET can be used for making ultra-low-power cellular neural network (CNN) based associative memory (AM) as well as low power SRAM cells [94–98]. The super-low off current, reduced temperature sensitivity and high transconductance per unit bias current of TFET is exploited in ultra-low power implantable bio-medical sensors employing TFET based Operational Transconductance Amplifier (OTA) and it is found to show sub-nW operating power [99]. TFETs due to its voltage scaling also find use in the development of SRAM memory cells for ultra-low power IoT applications [100].

The major drawback in TFET is the very low ON-state current and ambipolar conduction. A huge amount of research has been done and is still going on to increase the drive current of TFET so that it may commercially be viable in MOS circuits. Embedding a low bandgap material layer (like SiGe) near-source can increase the ON current but at the cost of a rise in OFF current which can be controlled by proper selection of gate metal work function [101, 102]. The use of double gate structure with high k gate dielectric replacing SiO_2, can enhance the drive current, give better control over the channel, reduce SS and generate very few variations in device parameters on scaling of channel length [89, 103]. Insertion of dielectric pocket (DP) at the two junctions, i.e. the source-channel and channel-drain junction has led to the improvement of BTBT increasing the efficiency of the device [104]. The use of silicon on insulator (SOI) technology for the construction of TFET was found to be one of the major advances. The entire PIN structure over the buried oxide (BOX) layer can reduce the OFF-state current by reducing the bipolar parasitic conduction [105, 106]. A modified approach to SOI technology is the use of selective buried oxide (SELBOX), which has a small gap in the buried oxide. The SELBOX TFET has the added advantage of the reduction of carriers during the OFF state which is trapped by the gap. It reduces OFF-state current and ambipolarity [107, 108]. Introduction of dual gate dielectric with high k material like HfO_2 towards source end and low k dielectric like SiO_2 towards drain end helps in reducing ambipolar behaviour, enhances on current and provides for abrupt switching [109]. Another approach to reduce the subthreshold slope and enhance the ON-state current is the use of Ferroelectric oxides as gate dielectric in place of SiO_2 [107, 108]. Research has also been carried out to use various geometrical modifications in TFETs structure to enhance its efficiency. Increasing the area of the tunnelling junction also provided enhanced I_{ON}/I_{OFF} ratio and steep SS [110]. Vertical TFET or V-TFET is another modified structure that enables the device to have BTBT along a direction perpendicular to the gate called line tunnelling which further improves the on-state current [111]. Vertically grown low bandgap source over the channel with source pocket and hetero material also lead to a decrease in SS and increase of I_{ON} due to

Table 1 A brief review on few of population meta-heuristics

Year	No. of benchmark functions	Technique and reference number	Name of authors	Complication
2020	30	Chimp optimization algorithm (ChoA) [6]	M. Khishe, M. R. Mosavi	Standard benchmark functions
2019	13	Hybrid particle swarm and spotted hyena optimizer algorithm (HPSSHO) [78]	Gaurav Dhiman, Amandeep Kaur	Standard benchmark functions and real-life engineering design problem
2020	5	Reliability based design optimization algorithm (RBDO) [70]	Zeng Meng et al	Engineering problems
2020	4	Bernstrain-search differential evolution algorithm (EBSD) [69]	Hoda zamani, Mohammad H. Nadimi-Shahraki, Shokooh Taghian, Mahdis Banaie-Dezfouli	Engineering design problems
2020	23	Hybrid Harris Hawks-sine cosine algorithm (hHH-SCA) [68]	Vikram Kumar Kamboj, Ayani Nandi, Ashutosh Bhadoria, Shivani Sehgal	Standard functions, multidisciplinary engineering problems
2021	32	Hybrid Harris Hawks pattern search algorithm (hHH-PS) [67]	Ardhala Balakrishna, Sohbit Saxena, Vikram Kumar Kamboj	Standard functions, multidisciplinary engineering problems
2020	29	Binary spotted hyena optimizer (SHO) [66]	Vijay Kumar, Avneet Kaur	Standard benchmark functions
2020	14	Modified adaptive butterfly optimization algorithm (BOA) [65]	Kun Hu, Hao Jiang, Chen-Gaung Ji, Ze Pan	Standard benchmark functions
2018	30	Multi-objective spotted hyena optimizer (MOSHO) [64]	Gaurav Dhiman, Vijay Kumar	Standard benchmark functions
2017	29	Spotted hyena optimizer (SHO) [63]	Gaurav Dhiman, Vijay Kumar	Standard benchmark functions
2021	29	Whale optimization algorithm (WOA) [62]	Vamshi Krishna Reddy, Venkata Lakshmi Narayana	Standard functions, multidisciplinary engineering problems
2018	6	Crow particle swarm optimization (CPO) algorithm [61]	Ko-Wei Huang et al	Standard benchmark functions
2020	20	Chicken Swarm Optimization algorithm (CSO) [59]	Sanchari Deb et al	Standard functions, multidisciplinary engineering problems
2017	22	Grey wolf optimizer-sine cosine algorithm (GWO-SCA) [60]	N. Singh, S. B. Singh	Benchmark functions and real-life optimization
2017	19	Grosshopper optimization algorithm (GOA) [58]	Shahrzad Saremi, Seyedali Mirjali, Andrew Lewis	Multidisciplinary engineering problems
2016	30	Virus colony search (VCS) [57]	Mu Dong Li et al	Benchmark functions, engineering problems
2016	24	Multi-verse optimizer (MVO) [56]	Seyedali Mirjali, Seyed Mohammad Mirjalili, Abdolreza Hatamlou	Standard benchmark functions, engineering problems
2015	24	Lightning search algorithm (LSA) [55]	Hussain Shareef et al	Standard benchmark functions
2014	22	Binary optimization using hybrid particle swarm optimization and gravitational search algorithm (PSOGSA) [80]	Seyedali Mirjalili et al	Standard benchmark functions
2016	18	Bird swarm algorithm (BSA) [54]	Xiang-Bing Meng et al	Standard benchmark functions
2014	14	Chaotic krill herd algorithm (CKH) [53]	Gai-Ge Wang et al	Standard benchmark functions
2019	47	Henry gas solubility optimization algorithm (HGSO) [52]	F. A Hashim et al	Standard benchmark functions
2020	23	Photon search algorithm (PSA) [40]	Y. Liu and R. Li	Standard benchmark functions
2009	23	Gravitational search (GSA) [81]	E. Rashedi et al	Standard benchmark functions
1997	30	Differential evolution (DE) [37]	R. Storn and K. Price	Standard benchmark functions
2008	14	Biogeography-based optimization (BBO) [38]	D. Simon	Standard benchmark functions
2015	23	Stochastic fractal search algorithm (SFS) [35]	H. Salimi	Standard benchmark functions
1999	23	Evolutionary programming (EP) [30]	Xin Yao, Yong Liu, Guangming lin	Standard benchmark functions

Table 1 (continued)

Year	No. of benchmark functions	Technique and reference number	Name of authors	Complication
1989	NA	Tabu search (TS) [82]	Fred Glover	Real world problems
2012	13	Teaching learning based optimization algorithm (TLBO) [25]	R. V. Rao et al	Standard benchmark functions
2001	NA	Harmony search (HS) [31]	Z. W. Geem et al	Musical variables
2019	29	Harris Hawks optimizer (HHO) [51]	A. A. Heidari et al	Standard benchmark functions, engineering problems
2015	36	Moth flame optimizer (MFO) [34]	S. Mirjalili	Standard benchmark functions, engineering problems
2014	4	Forest optimisation algorithm (FOA) [32]	M. Ghaemi et al	NA
2014	32	Grey wolf optimizer algorithm (GWO) [33]	S. Mirjalili et al	Standard benchmark functions, engineering problems

Table 2 Uni-modal (UM) standard benchmark functions

Functions	Dimensions	Range	$f_{\min}$
$F_1(U) = \sum_{m=1}^{z} U_m^2$	30	[−100, 100]	0
$F_2(U) = \sum_{m=1}^{z} \lvert U_m \rvert + \prod_{m=1}^{z} \lvert U_m \rvert$	30	[−10, 10]	0
$F_3(U) = \sum_{m=1}^{z} (\sum_{n-1}^{m} U_n)^2$	30	[−100, 100]	0
$F_4(U) = \max_m \{\lvert U_m \rvert, 1 \le m \le z\}$	30	[−100, 100]	0
$F_5(U) = \sum_{m=1}^{z-1} [100(U_{m+1} - U_m^2)^2 + (U_m - 1)^2]$	30	[−38, 38]	0
$F_6(U) = \sum_{m=1}^{z} ([U_m + 0.5])^2$	30	[−100, 100]	0
$F_7(U) = \sum_{m=1}^{z} mU_m^4 + \text{random}[0, 1]$	30	[−1.28, 1.28]	0

Table 3 Multi-modal (MM) standard functions

Multi-modal (F_8–F_{13}) benchmark functions	Dim	Range	$f_{\min}$
$F_8(U) = \sum_{m=1}^{z} -U_m \sin(\sqrt{\lvert U_m \rvert})$	30	[−500, 500]	−418.98295
$F_9(U) = \sum_{m=1}^{z} [U_m^2 - 10\cos(2\pi U_m) + 10]$	30	[−5.12, 5.12]	0
$F_{10}(U) = -20\exp\left(-0.2\sqrt{\left(\frac{1}{z}\sum_{m=1}^{z} U_m^2\right)}\right) - \exp\left(\frac{1}{z}\sum_{m=1}^{z} \cos(2\pi U_m)\right) + 20 + d$	30	[−32, 32]	0
$F_{11}(U) = 1 + \sum_{m=1}^{z} \frac{U_m^2}{4000} - \Pi_{m=1}^{z} \cos\frac{U_m}{\sqrt{m}}$	30	[−600, 600]	0
$F_{12}(U) = \frac{\pi}{z}\left\{10\sin(\pi\tau_1) + \sum_{m=1}^{z-1}(\tau_m - 1)^2[1 + 10\sin^2(\pi\tau_{m+1})] + (\tau_z - 1)^2\right\} + \sum_{m=1}^{z} g(U_m, 10, 100, 4)$ $\tau_m = 1 + \frac{U_m + 1}{4}$ $g(U_m, b, x, i) = \begin{cases} x(U_m - b)^i U_m > b \\ 0 - b < U_m < b \\ x(-U_m - b)^i U_m < -b \end{cases}$	30	[−50, 50]	0
$F_{13}(U) = 0.1\left\{\sin^2(3\pi U_m) + \sum_{m=1}^{z}(U_m - 1)^2[1 + \sin^2(3\pi U_m + 1)] + (x_z - 1)^2\left[1 + \sin^2\right)\right]$	30	[−50, 50]	0

both line and point tunnelling [112]. Another geometrical modification of the conventional TFET includes a broken gate (BG) structure which reportedly reduces ambipolar current drastically resulting in lower OFF current and reduced power [113]. Use of three dimensional structures like gate-all-around (GAA) gives higher control of the drain current by the gate voltage and leads to superior performance [114]. There are also prospects of increasing the ON current by utilising III-V hetero materials for making TFET [115–117]. Newer materials like graphene [118] and Carbon nano tubes (CNT) [119] also showed promising results for implementing TFET devices in modern high density ultra-low power circuits and systems.

Table 4 Fixed-dimension (FD) standard functions

Fixed modal (FD) (F_{14}–F_{23}) standard benchmark functions	Dimension	Range	$f_{\min}$
$F_{14}(U) = \left[\frac{1}{500} + \sum_{n=1}^{2} 5 \frac{1}{n+\sum_{m=1}^{z}(U_m - b_{mn})6}\right]^{-1}$	2	[− 65.536, 65.536]	1
$F_{15}(U) = \sum_{m=1}^{11}\left[b_m - \frac{U_1(a_m^2 + a_m\eta_2)}{a_m^2 + a_m\eta_3 + \eta_4}\right]^2$	4	[− 5, 5]	0.00030
$F_{16}(U) = 4U_1^2 - 2.1U_1^4 + \frac{1}{3}U_1^6 + U_1U_2 - 4U_2^2 + 4U_2^4$	2	[− 5, 5]	− 1.0316
$F_{17}(U) = (U_2 - \frac{5.1}{4\pi 2}U_1^2 + \frac{5}{\pi}U_1 - 6)^2 + 10\,(1 - \frac{1}{8\pi})\cos U_1 + 10$	2	[− 5, 5]	0.398
$F_{18}(U) = [1 + (U_1 + U_2 + 1)_2\,(19 - 14\,U_1 + 3U_2{}^1 - 14\,U_2 + 6U_1U_2 + 3\,U_2{}^2)] \times [30 + (2U_1 - 3U_2)_2 \times (18 - 32U_1 + 12\,U_2{}^1 + 48U_2 - 36U_1U_2 + 27\,U_2{}^2)]$	2	[− 2, 2]	3
$F_{19}(U) = -\sum_{m=1}^{4} d_m \exp\left(-\sum_{n=1}^{3} U_{mn}(U_m - q_{mn})^2\right)$	3	[1, 3]	− 3.32
$F_{20}(U) = -\sum_{m=1}^{4} d_m \exp\left(-\sum_{n=1}^{6} U_{mn}(U_m - q_{mn})^2\right)$	6	[0, 1]	− 3.32
$F_{21}(U) = -\sum_{m=1}^{5}[(U - b_m)(U - b_m)^{\mathrm{T}} + d_m]^{-1}$	4	[0, 10]	− 10.1532
$F_{22}(U) = -\sum_{m=1}^{7}[(U - b_m)(U - b_m)^{\mathrm{T}} + d_m]^{-1}$	4	[0, 10]	− 10.4028
$F_{23}(U) = -\sum_{m=1}^{7}[(U - b_m)(U - b_m)^{\mathrm{T}} + d_m]^{-1}$	4	[0, 10]	− 10.5363

Table 5 Algorithm parameters for imp-chimp optimizer algorithm

Parameters name	Value	Parameter name	Value
Search agents	30	No. of population for SHO	30
Maximum iterations for benchmark functions	500	Maximum iterations for engineering design problems	1000

The present paper discusses various recent optimization techniques to obtain a suitable range of dimension and performance parameters of different TFET architectures meeting ITRS standards. Further, different transistors presented are mainly aimed at designing novel TFET models using various techniques like geometrical modifications, dielectric engineering, gate work function engineering, using asymmetric hetero materials for source and drain, playing with doping concentrations, varying the gate length for source/channel/drain underlap and overlap etc. to eliminate the fundamental limitations. Some new techniques like charge plasma-based junction less TFETs which greatly reduce fabrication complexity and leakage are also described. Further application of TFETs in biomolecule sensors and various digital circuits are also discussed.

The rest of the paper is arranged in the following order, the first section compares different optimization techniques to obtain an optimum design of TFET with improved

Table 7 Execution time for unimodal benchmark problems using ICHIMP-SHO algorithm

Function	Best time	Average time	Worst time
F1	1.4375	1.795833333	2.328125
F2	1.390625	1.759895833	1.9375
F3	1.859375	2.118229167	2.296875
F4	1.3125	1.472395833	1.671875
F5	1.34375	1.519270833	1.75
F6	1.34375	1.480729167	1.703125
F7	1.4375	1.60625	1.8125

Table 6 Test observations of (F1–F7) Functions using ICHIMP-SHOAlgorithm

Function	Mean	St. deviation	Best fitness value	Worst fitness value	Median	Wilcoxon rank sum test	*t* test	
						P value	*P* value	*h* value
F1	3.91443E−28	1.07214E−27	2.2954E−30	5.6993E−27	7.16499E−29	1.7344E−06	0.054971323	0
F2	4.70089E−17	3.86924E−17	7.04913E−18	1.59728E−16	4.01121E−17	1.7344E−06	2.69095E−07	1
F3	8.48976E−07	2.54158E−06	1.11728E−09	1.38683E−05	1.50394E−07	1.7344E−06	0.077611649	0
F4	3.64228E−08	3.08114E−08	2.77549E−09	1.26518E−07	3.2531E−08	1.7344E−06	4.36866E−07	1
F5	28.38318363	0.671703255	26.23392716	28.89070125	28.65306199	1.7344E−06	6.30357E−49	1
F6	1.481698857	0.405138911	0.742524222	2.257134021	1.732292069	1.7344E−06	1.57295E−18	1
F7	0.001127419	0.00056314	0.000275088	0.00238846	0.001036141	1.7344E−06	7.83249E−12	1

Table 8 Evaluation for (F1–F7) problems

Algorithm	Parameters	(F1–F7) uni-modal benchmark functions						
		F1	F2	F3	F4	F5	F6	F7
Lightning search algorithm (LSA) [55]	Mean	4.81067E−08	3.340000000	0.024079674	0.036806544	43.24080402	1.493275733	64.28160301
	St. deviation	3.40126E−07	2.086007800	0.005726198	0.156233023	29.92194448	1.302827039	43.75576111
Battle royale optimization algorithm (BRO) [84]	Avg	3.0353E−09	0.000046	54.865255	0.518757	99.936848	2.8731E−08	0.000368
	St. deviation	4.1348E−09	0.000024	16.117329	0.403657	82.862958	1.8423E−08	0.000094
Opposition based enhanced grey wolf optimization algorithm (OEGWO) [85]	Avg	2.49×10^{-34}	4.90×10^{-25}	1.01×10^{-1}	1.90×10^{-5}	2.72×10^{1}	1.40×10^{00}	3.63×10^{-4}
	St. deviation	7.90×10^{-34}	6.63×10^{-25}	3.21×10^{-1}	2.43×10^{-5}	7.85×10^{1}	4.91×10^{-1}	2.68×10^{-4}
Photon Search Algorithm (PSA) [40]	Mean	15.3222	2.2314	3978.0837	1.1947	332.6410	19.8667	0.0237
	St. deviation	27.3389	1.5088	3718.9156	1.0316	705.1589	33.4589	0.0170
Hybrid Harris Hawks Optimizer-Pattern Search algorithm (hHHO-PS) [67]	Avg	9.2×10^{-017}	8.31E	5.03×10^{-20}	6.20×10^{-54}	2.18×10^{-9}	3.95×10^{-14}	0.002289
	St. deviation	5E−106	4.46×10^{-53}	1.12×10^{-19}	1.75×10^{-53}	6.38×10^{-10}	3.61×10^{-14}	0.001193
Spotted Hyena Optimizer (SHO) [63]	Avg	0	0	0	7.78×10^{-12}	8.59E+00	2.46×10^{-1}	3.29×10^{-5}
	St. deviation	0	0	0	8.96×10^{-12}	5.53E−01	1.78×10^{-1}	2.43×10^{-5}
Harris Hawks Optimizer (HHO) [51]	Mean	1.06×10^{-90}	6.92×10^{-51}	1.25×10^{-80}	4.46×10^{-48}	0.015002	0.000115	0.000158
	St.Deviation	5.82×10^{-90}	2.47×10^{-50}	6.63×10^{-80}	1.70×10^{-47}	0.023473	0.000154	0.000225
Enhanced Crow search algorithm (ECSA) [86]	Mean	7.4323E−119	5.22838E−59	3.194E−102	3.04708E−52	7.996457081	0.400119079	1.30621E−05
	St. deviation	4.2695E−118	2.86361E−58	1.7494E−101	1.66895E−51	0.661378213	0.193939866	8.39859E−06
Transient search optimization (TSO) [87]	Avg	1.18×10^{-99}	8.44×10^{-59}	3.45×10^{41}	1.28E−53	8.10×10^{-2}	3.35×10^{-3}	3.03×10^{-4}
	St. deviation	6.44×10^{-99}	3.93×10^{-58}	1.26×10^{-41}	6.58×10^{-53}	11	6.82×10^{-3}	3.00×10^{-4}
ICHIMP-SHO (proposed algorithm)	Mean	3.91443E−28	4.70089E−17	8.48976E−07	3.64228E−08	28.38318363	1.481698857	0.001127419
	St. deviation	1.07214E−27	3.86924E−17	2.54158E−06	3.08114E−08	0.671703255	0.405138911	0.00056314

subthreshold performances. The next section gives the readers a basic idea about the layout and structure of TFET and compares it with the structure of MOSFET. The following section familiarises with the various performance parameters of TFET like subthreshold parameters and analog/RF performance parameters. The next section discusses some of the popular existing TFET architectures and classifies them. The following section presents a comparative study of various TFET architectures introduced in the previous section based on the performance parameters discussed earlier. The last section concludes our article based on comparative analysis. A glossary is presented at the end of the article to familiarise the readers with abbreviations used in the paper specifically for different TFET architectures.

7 Basic structure of TFET

Let us examine the basic structure of a tunnelling FET now. Section 6 will elaborate on many variations of this structure, but the working principle of the TFET is based on this basic arrangement of regions, doping and terminals. Figure 13a–c shows the basic structure of an n-channel and p-channel TFET respectively.

8 Performance parameters

8.1 Threshold voltage

The threshold voltage (V_T) may be defined as the minimum gate to source voltage required for the initiation of current conduction through the channel of a FET. For conventional MOS it is defined as the voltage required at the gate terminal to form an inversion layer at the channel so that a path for the flow of charge carriers is built between source and drain. But

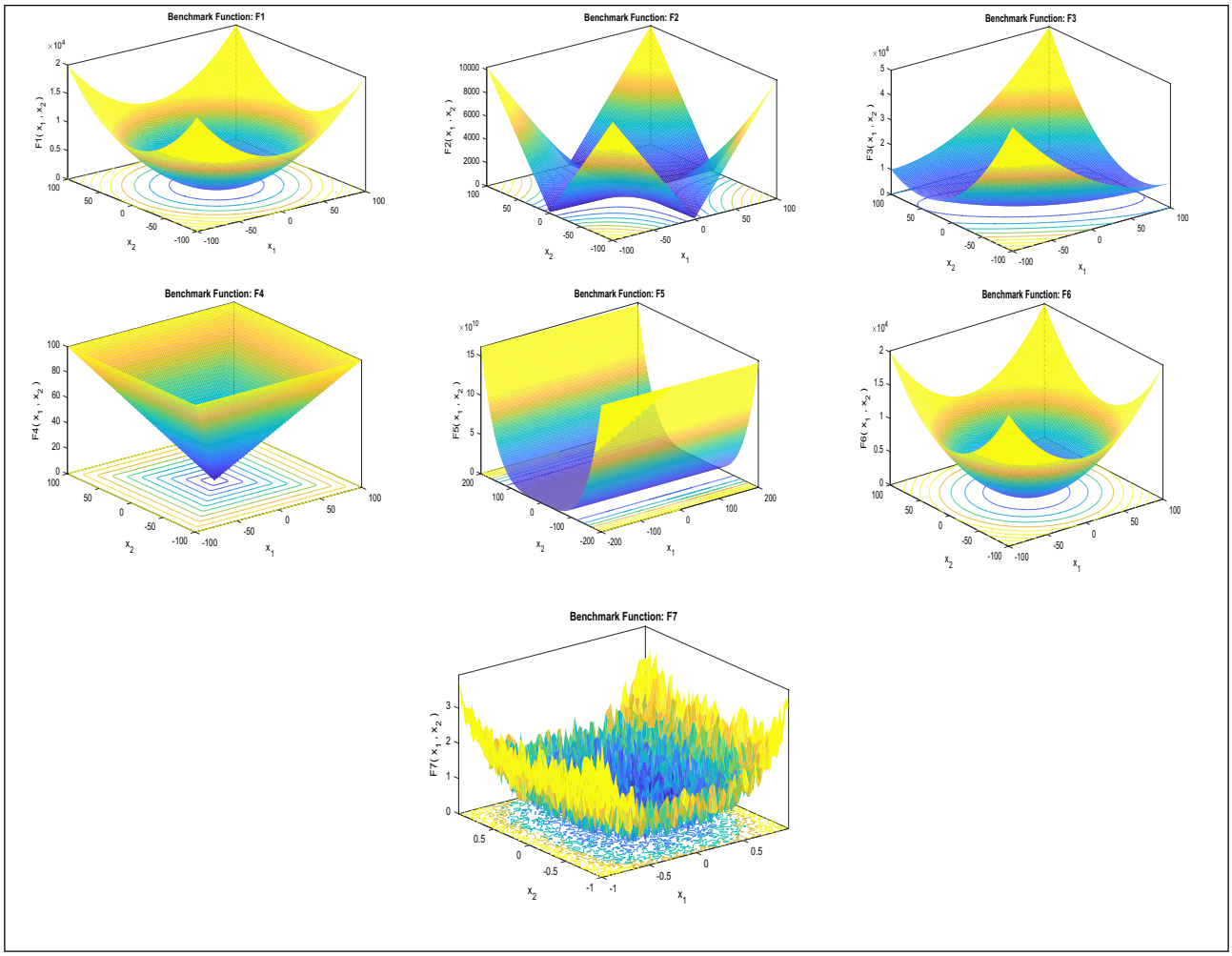


Fig. 4 3D view of uni-modal (UM) standard benchmark problems

for TFET it may be defined as the minimum gate to source voltage required to align the valence band of the source and conduction band of the channel in such a way that that band to band (BTB) tunnelling between them may be initiated. For TFET threshold voltage is independent of temperature.

8.2 Subthreshold slope

The subthreshold slope may be defined as the amount of gate voltage required to produce a unit decade change in drain current [89] in the subthreshold region. Mathematically it may be given as the ratio of change in gate voltage to change in the log of drain current as

$$S = \frac{\mathrm{d}V_{\mathrm{g}}}{\mathrm{d}\left(\log I_{\mathrm{d}}\right)}\ \mathrm{mV/dec.} \tag{25}$$

For conventional MOSFET devices, it is found to be independent of gate to source voltage and given as [101]

$$S_{\mathrm{MOSFET}} = \frac{kT}{q}\ln 10\left(1+\frac{C_{\mathrm{D}}}{C_{\mathrm{ox}}}\right) \tag{26}$$

where C_{D} and C_{ox} are depletion and oxide capacitances of the device and kT/q represents the thermal limit of MOS devices which restricts them to have a minimum subthreshold slope of 60 mV/dec at $T = 300$ K (room temperature).

But TFET devices are not restricted by the thermal barrier, rather they depend on the tunnelling barrier at the source-channel junction. The subthreshold slope for TFET is given as [102]

$$S_{\mathrm{TFET}} = \frac{V_{\mathrm{GS}}^2}{2V_{GS} + B_{\mathrm{kane}}W_{\mathrm{g}}^{3/2}/D} \tag{27}$$

Therefore, unlike MOSFET subthreshold slope of TFET is highly dependent on the gate voltage and lightly dependent upon bandgap at the tunnelling junction (source-channel

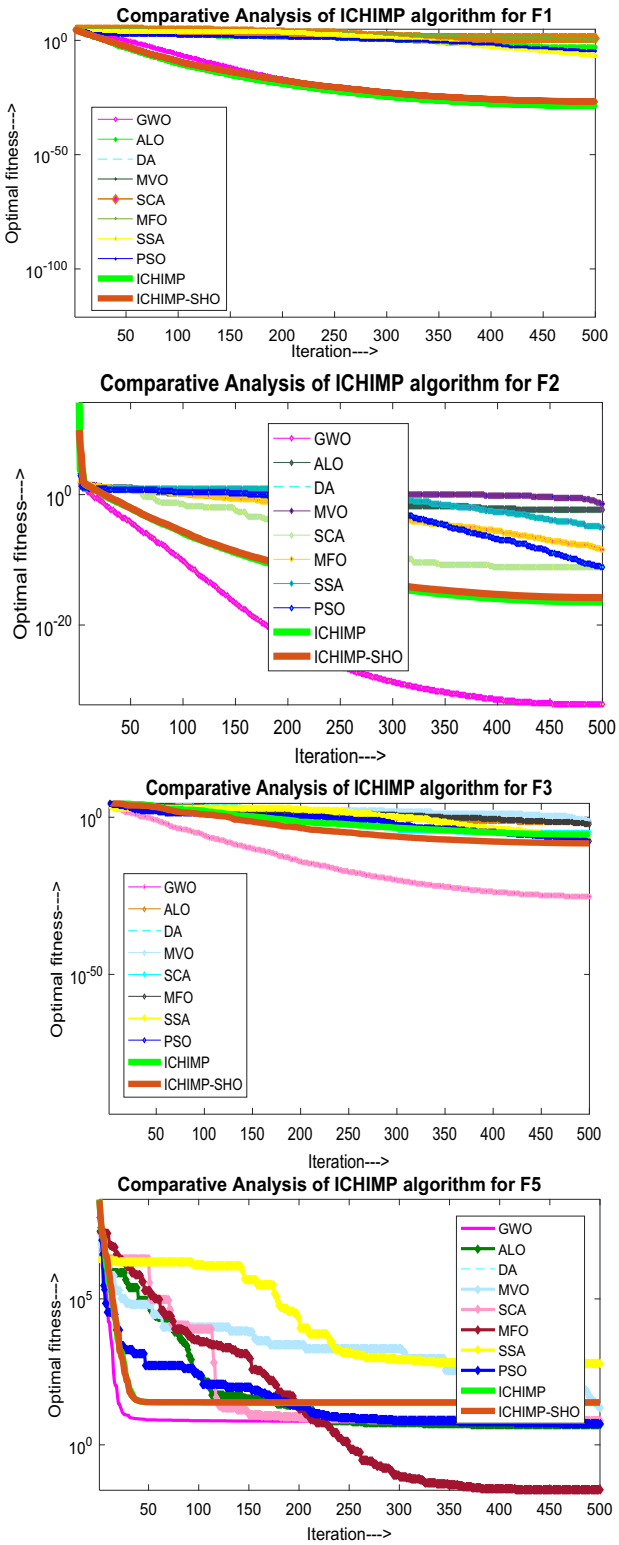


Fig. 5 Comparative curve of ICHIMP-SHO- with GWO, DA, ALO, MVO, SSA and PSO for UM standard benchmark functions

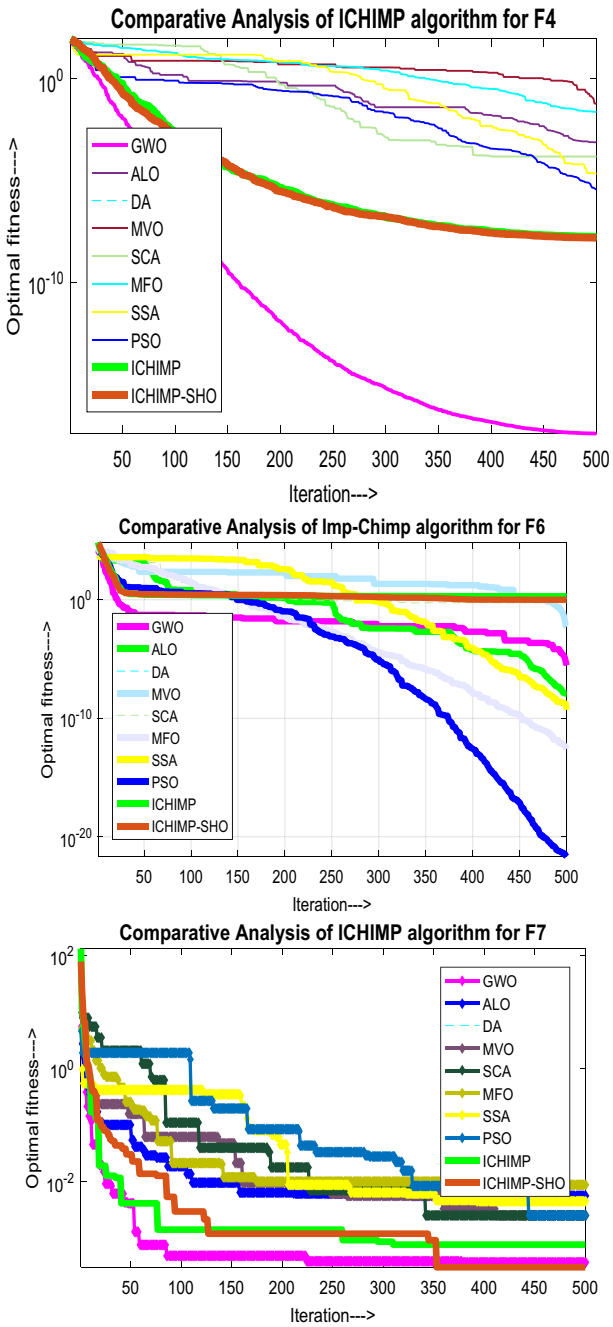


Fig. 5 (continued)

junction). So, clearly sub 60 mV/dec S value may be obtained for TFET by using low V_{GS}.

8.3 ON state current

For TFET, the ON state current I_{ON} is a very important performance evaluating parameter, it must be as high as possible for better performance. It is defined as the drain to source current I_{DS} which flows through the device when the gate to

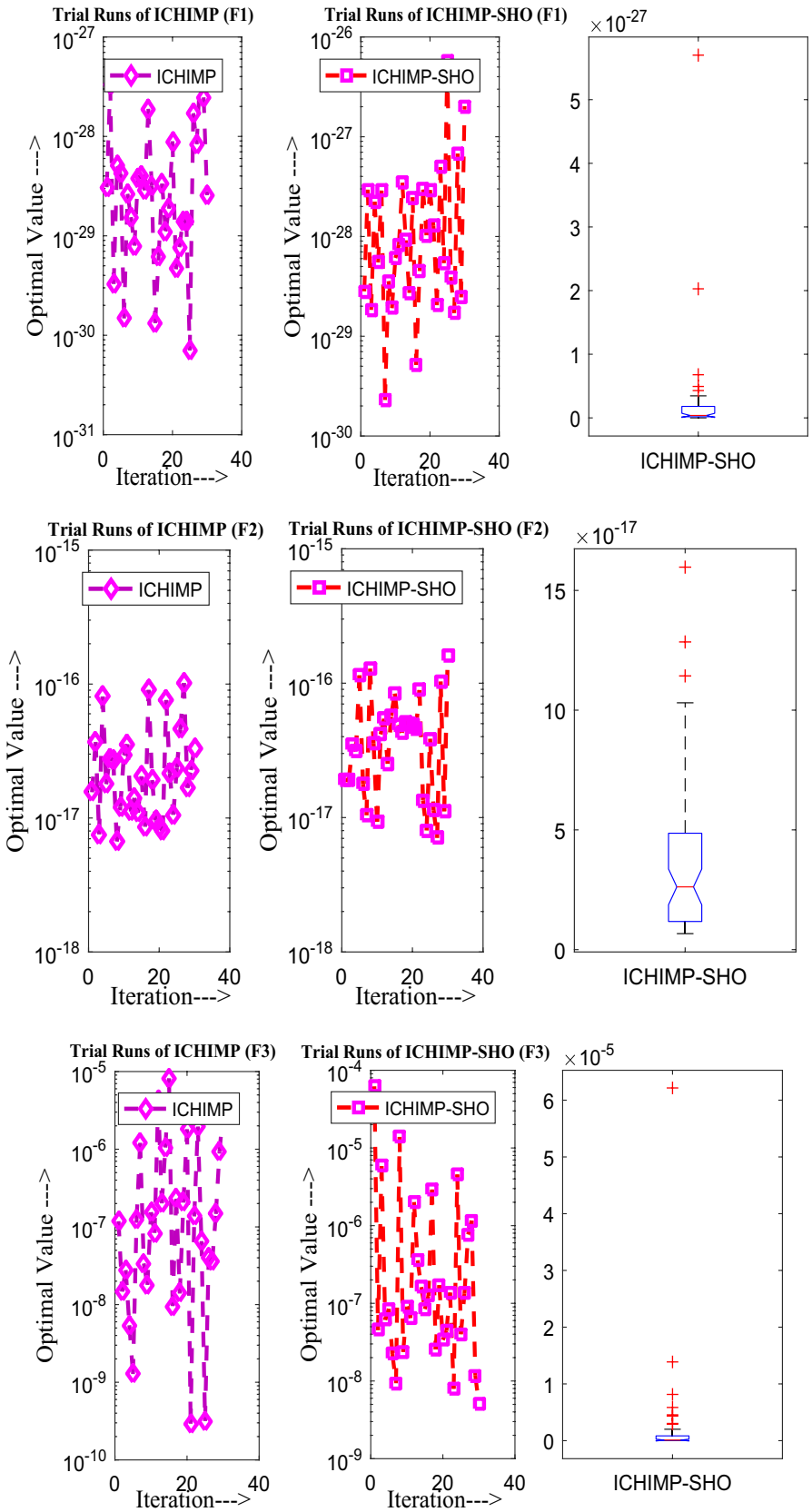


Fig. 6 Trail runs of ICHIMP and ICHIMP-SHO for UM standard benchmark functions

Fig. 6 (continued)

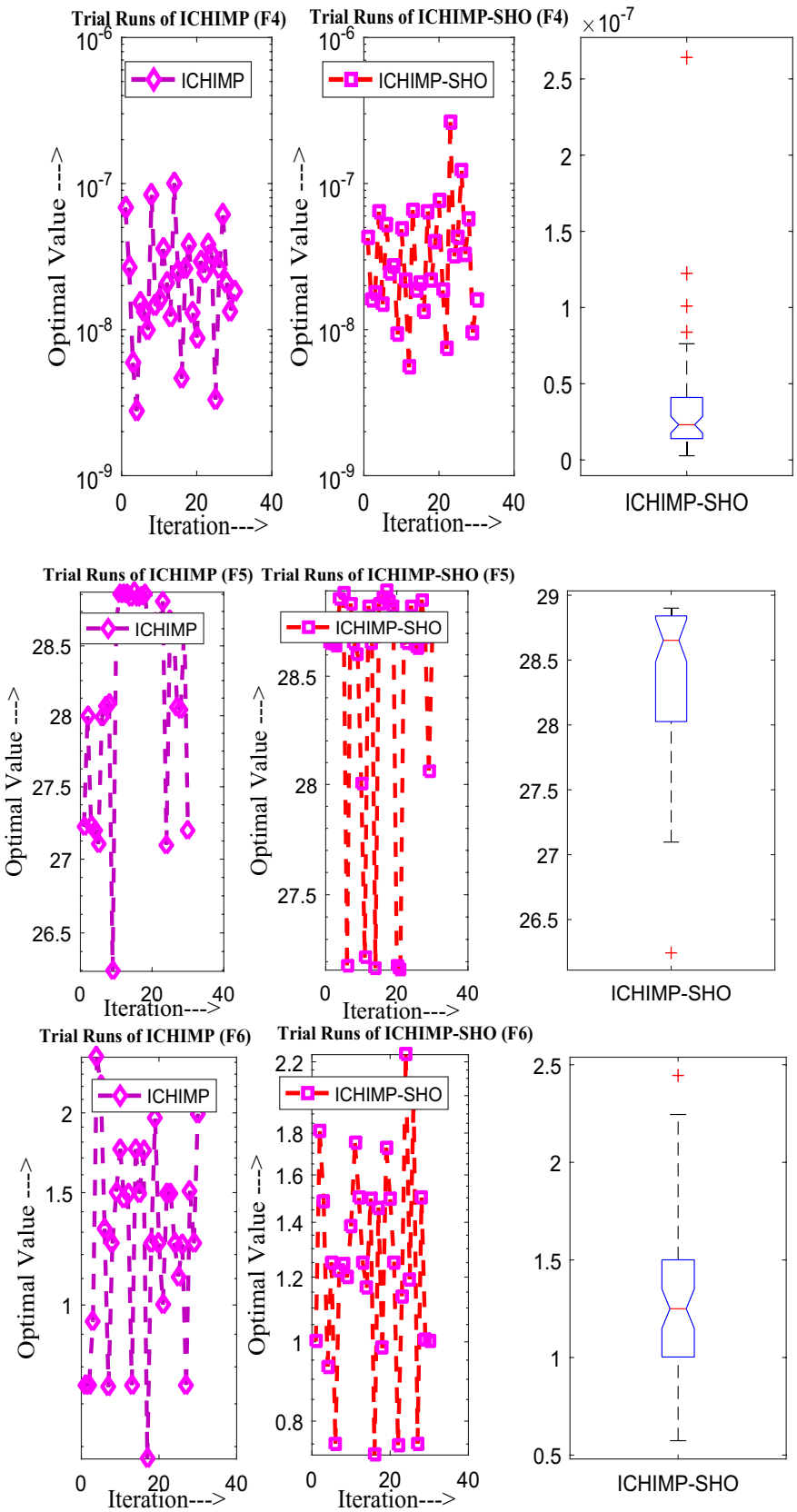


Fig. 6 (continued)

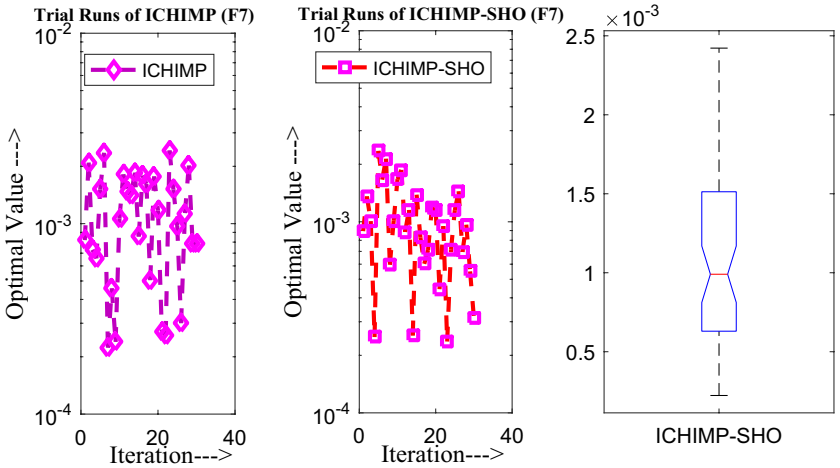


Table 9 Test results of multimodal benchmark functions using IChimp-SHO algorithm

Function	Mean value	St. deviation	Best fitness value	Worst fitness value	Median value	Wilcoxon rank sum test	*t* test	
						P value	*P* value	*h* value
F8	−5231.965502	755.2916365	−6835.710117	−3547.406759	−5099.515588	1.7344E−E−06	2.85762E−26	1
F9	7.95808E−14	5.29885E−14	0	2.27374E−13	5.68434E−14	2.89814E−06	4.53821E−09	1
F10	9.52719E−14	1.69917E−14	6.83897E−14	1.35891E−13	9.50351E−14	1.67736E−06	1.13726E−23	1
F11	0.001725278	0.004532246	0	0.015441836	0	0.125	0.045981511	1
F12	0.088180059	0.097309399	0.011803437	0.567716636	0.074592218	1.7344E−06	2.80855E−05	1
F13	1.911006715	0.317196258	1.325094518	2.527060925	1.866111264	1.7344E−06	1.49706E−24	1

Table 10 Execution time for unimodal benchmark problems using IChimp-SHO algorithm

Function	Best time	Average time	Worst time
F8	1.359375	1.510416667	1.734375
F9	1.328125	1.479166667	1.703125
F10	1.34375	1.521875	1.8125
F11	1.40625	1.5203125	1.6875
F12	1.71875	1.8515625	2.015625
F13	1.65625	1.805729167	1.921875

source voltage is greater than V_T. In other words, it is the drain current when the device is ON. The major contributor to I_{ON} is BTBT of electrons at the source-channel junction.

8.4 OFF state current

It is represented as I_{OFF}. It may be defined as the amount of current which flows between drain and source when the gate to source voltage is below threshold voltage or when then the device is considered OFF. Ideally, I_{OFF} should be tending to zero but practically it has some non-zero value due to the presence of finite subthreshold slope. I_{OFF} has some finite value due to various leakage phenomena and ambipolar behaviour of TFET, but it must be maintained as small as possible for good performance.

The ratio between ON-state current and OFF-state current is another important performance parameter. For efficient performance of the TFET I_{ON}/I_{OFF} should be as high as possible.

8.5 Drain induced barrier lowering (DIBL)

The drain induced barrier lowering (DIBL) is a type of short channel effects (SCE) it is responsible for lowering of threshold voltage at high drain biases. It must be as small as possible for better performance of the TFET. The high value of DIBL makes the ON-state current highly dependent on drain voltage rather than gate. It destroys the gate controllability of the device and renders it useless. Mathematically it is defined as the ratio between the difference of threshold voltages measured at high and low drain voltages to the difference between the high and low drain voltages [120].

$$\mathrm{DIBL} = -\frac{V_{\mathrm{Th}}^{\mathrm{high}} - V_{\mathrm{Th}}^{\mathrm{low}}}{V_{\mathrm{D}}^{\mathrm{high}} - V_{\mathrm{D}}^{\mathrm{low}}} \tag{28}$$

Table 11 Comparison for multimodal benchmark functions

Algorithm	Factors	(F8–F13) Multi-modal benchmark functions					
		F8	F9	F10	F11	F12	F13
Lightning search algorithm (LSA) [55]	Avg	−8001.3887	62.7618960	1.077446947	0.397887358	2.686199995	0.007241875
	St. deviation	669.159310	14.9153021	0.337979509	1.68224E−16	0.910802774	0.006753356
Battle Royale Optimization algorithm (BRO) [84]	Mean	−7035.2107	48.275350	0.350724	0.001373	0.369497	0.000004
	St. deviation	712.33269	14.094585	0.688702	0.010796	0.601450	0.000020
Opposition based enhanced grey wolf optimization algorithm (OEGWO) [85]	Avg	-3.36×10^{3}	8.48×10^{-1}	9.41×10^{-15}	7.50×10^{-13}	9.36×10^{-02}	1.24E+00
	St. deviation	3.53×10^{2}	4.65E+00	3.56×10^{-15}	4.11×10^{-12}	3.95×10^{-02}	2.09×10^{-1}
Photon search algorithm (PSA) [40]	Mean	11, 648.5512	7.3763	1.6766	0.5294	0.1716	1.5458
	St. deviation	1230.4314	9.1989	0.9929	0.6102	0.2706	3.3136
Hybrid Harris Hawks optimizer-pattern search algorithm (hHHO-PS) [67]	Avg	−12, 332	00	8.88×10^{-6}	00	2.94×10^{-15}	1.16×10^{-13}
	St. deviation	335.7988	0	0	0	3.52E−15	1.15E−13
Spotted hyena optimizer (SHO) [63]	Mean	$-1.16\text{E}\times10^{3}$	0.00E+00	2.48E+000	00	3.68×10^{-2}	9.29×10^{-1}
	St. deviation	$2.72\text{E}\times10^{2}$	0.00E+00	1.41E+000	00	1.15×10^{-2}	9.52×10^{-2}
Harris Hawks optimizer (HHO) [51]	Mean	−12, 561.38	0	8.88×10^{-16}	0	8.92×10^{-6}	0.000101
	St. deviation	40.82419	0	0	0	1.16×10^{-5}	0.000132
Enhanced crow search algorithm (ECSA) [86]	Mean	−2332.3867	0	8.88178E−16	0	0.11738407	0.444690657
	St. deviation	223.93995	0	0	0	0.2849633	0.199081675
Transient search optimization (TSO) [87]	Avg	−12, 569.5	00	8.88×10^{-16}	0	1.30×10^{-4}	7.55×10^{-4}
	St. deviation	1.81×10^{-2}	00	0	0	1.67×10^{-4}	1.74×10^{-3}
ICHIMP-SHO (proposed algorithm)	Mean	−5231.965502	7.95808E−14	9.52719E−14	0.001725278	0.088180059	1.911006715
	St. deviation	755.2916365	5.29885E−14	1.69917E−14	0.004532246	0.097309399	0.317196258

The value of DIBL is always positive which is ensured by the negative sign in front of the formula as threshold voltage measured at high drain voltage is always lower than that measured at low drain voltage. The unit for DIBL is mV/V and it should be as low as possible.

8.6 Analog/RF performance parameters

The ultra-low-power TFET devices must have good switching speeds to be compatible with modern high-speed processors. The most important high-frequency performance parameters which decide the efficient functioning of TFETs are transconductance (g_m), cut-off frequency (f_T), gain bandwidth product (GBP) and transit time (τ) [121].

8.7 Transconductance

The transconductance (g_m) of a TFET is defined as the rate of change of drain current to change its gate to source voltage when the drain to source voltage is kept constant. Mathematically it is given as,

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}} \tag{29}$$

It can be obtained graphically as the slope of transfer characteristic of TFET.

8.8 Cut-off frequency

Cut-off frequency (f_T) is one of the crucial performance parameters for analog/RF operations. It is defined as the frequency at which the small signal, short circuit current gain reduces to one [121]. It is given as

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \tag{30}$$

where C_{gs} is gate to source capacitance and C_{gd} is the gate to drain capacitance. The value cut-off frequency should be high for better performance.

8.9 Gain bandwidth product

GBP is another important RF performance parameter; it is a trade-off parameter between gain and bandwidth of the device. It is responsible for determining the selectivity of a circuit. GBP is generally used to determine the device performance at DC gain of 10 [122] and is mathematically given as

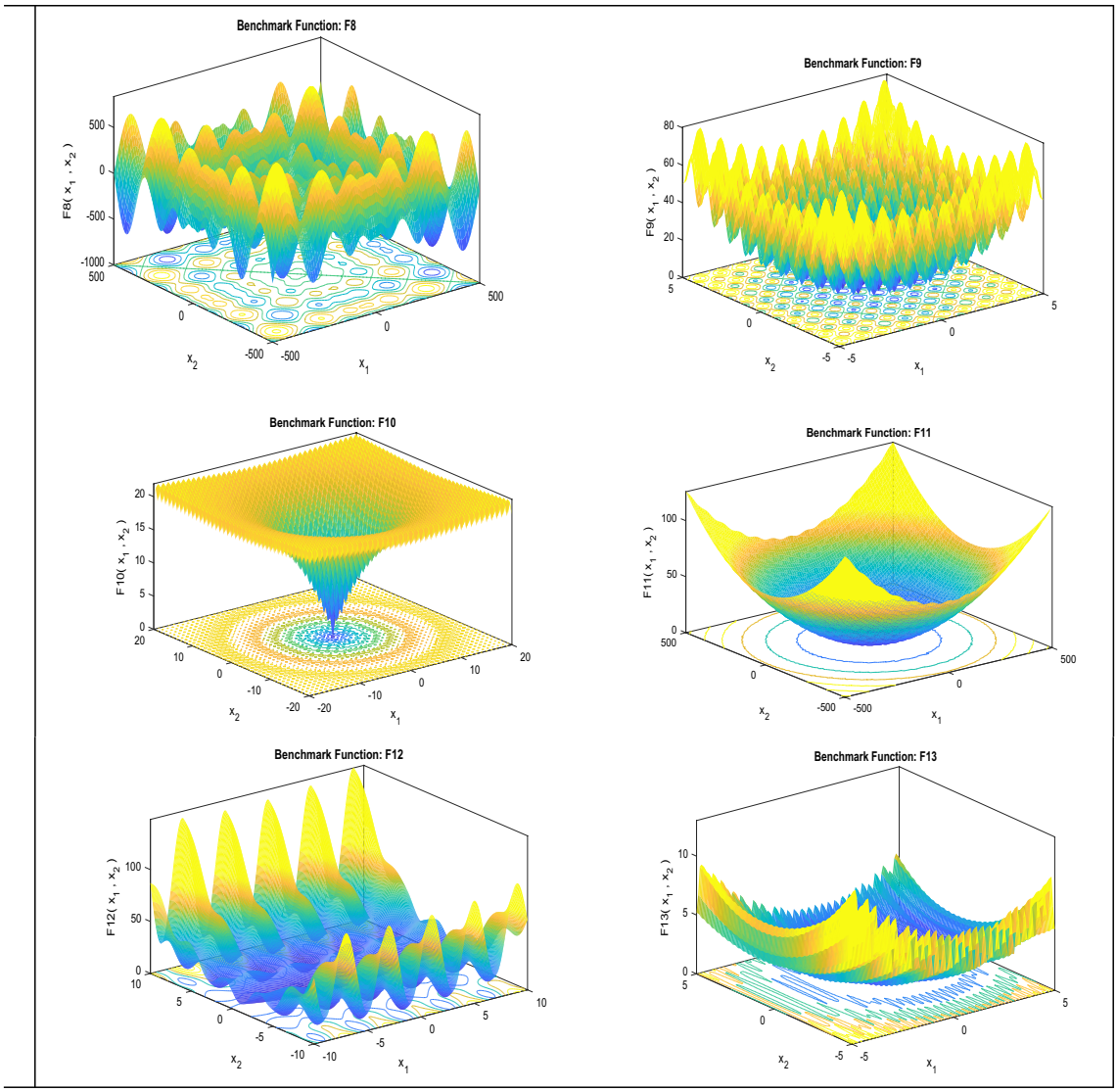


Fig. 7 3D view of multi-modal (MM) standard benchmark problem

$$\text{GBP} = \frac{g_{\text{m}}}{20\pi C_{\text{gd}}} \tag{31}$$

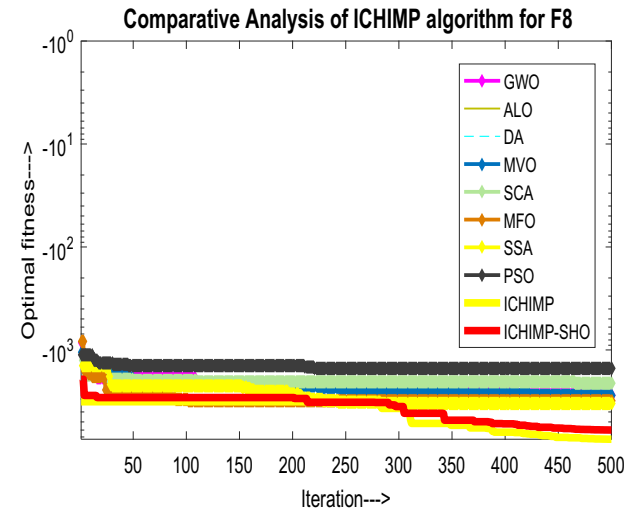
8.10 Transit time

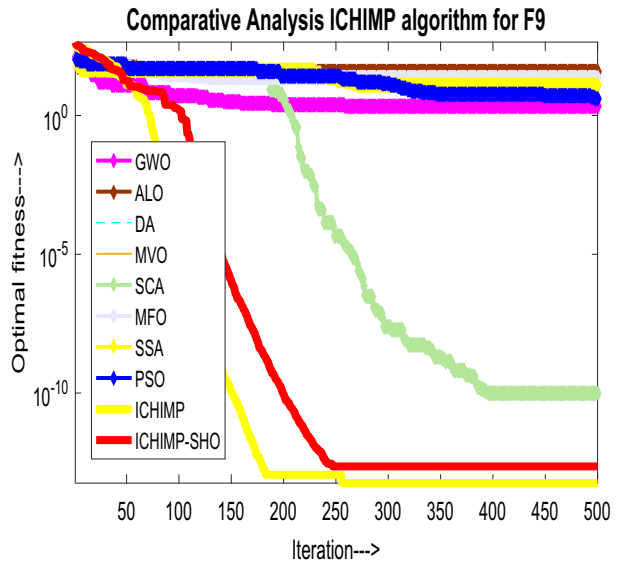
Another important parameter that determines the analog/RF performance of TFET devices is the transit time denoted by τ. Transit time specifies the time required for the charge carriers to travel from source of the device to the drain [121]. It is a measure of how fast the device functions. Mathematically it is proportional to the inverse of cut-off frequency, given as

$$\tau = \frac{1}{2\pi f_{\text{T}}} \tag{32}$$

9 Existing TFET architectures and dimensions

Researchers focused on various structural and geometrical modifications along with use of newer and advanced materials for the construction and modification of the basic tunnel FET structure. Some of these structures are classified and briefly explained here along with there dimensional features. Few of them focused on the use hetero dielectric structure for gate dielectric having a combination of low k and high k materials and use of low band gap material for source. Madan and Chaujar [123] suggested a TFET having gate to drain overlap, hetero gate dielectric and gate wrapped all around the channel structure called GDO HD GAA TFET (Fig. 14). The gate drain overlap suppresses the ambipolar current while hetero material for gate dielectric enhances





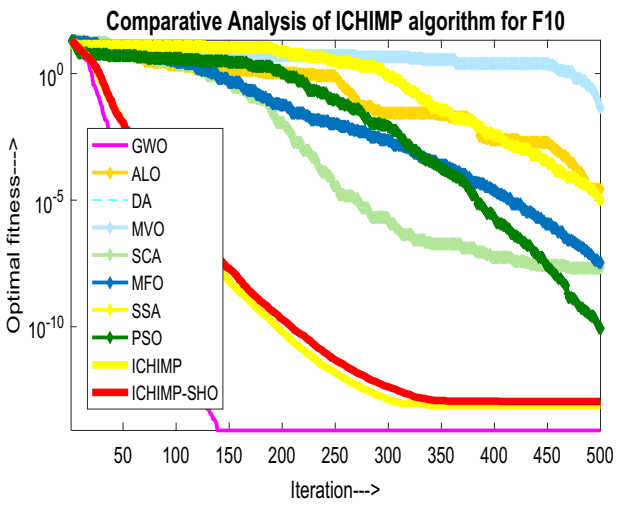
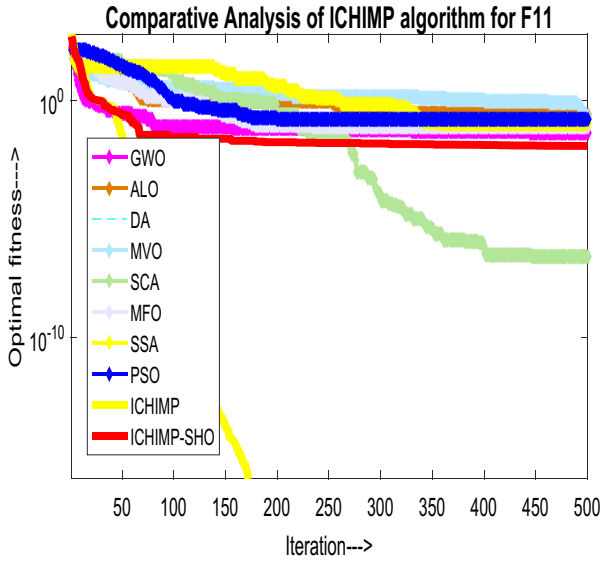
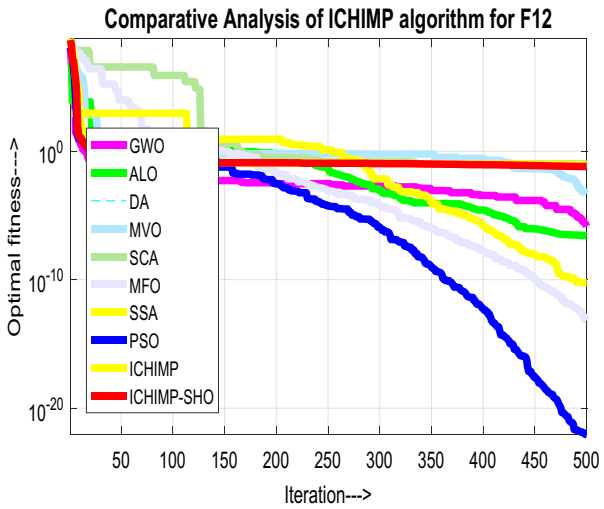


Fig. 8 Comparative curve of ICHIMP-SHO with GWO, DA, ALO, MVO, SSA and PSO for MM standard benchmark functions





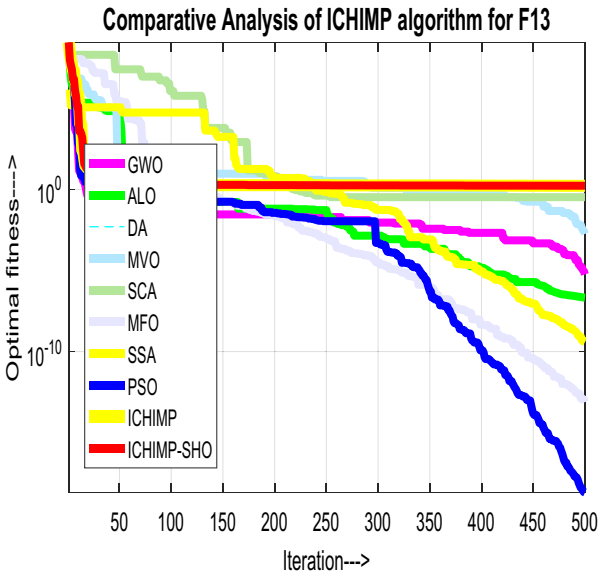


Fig. 8 (continued)

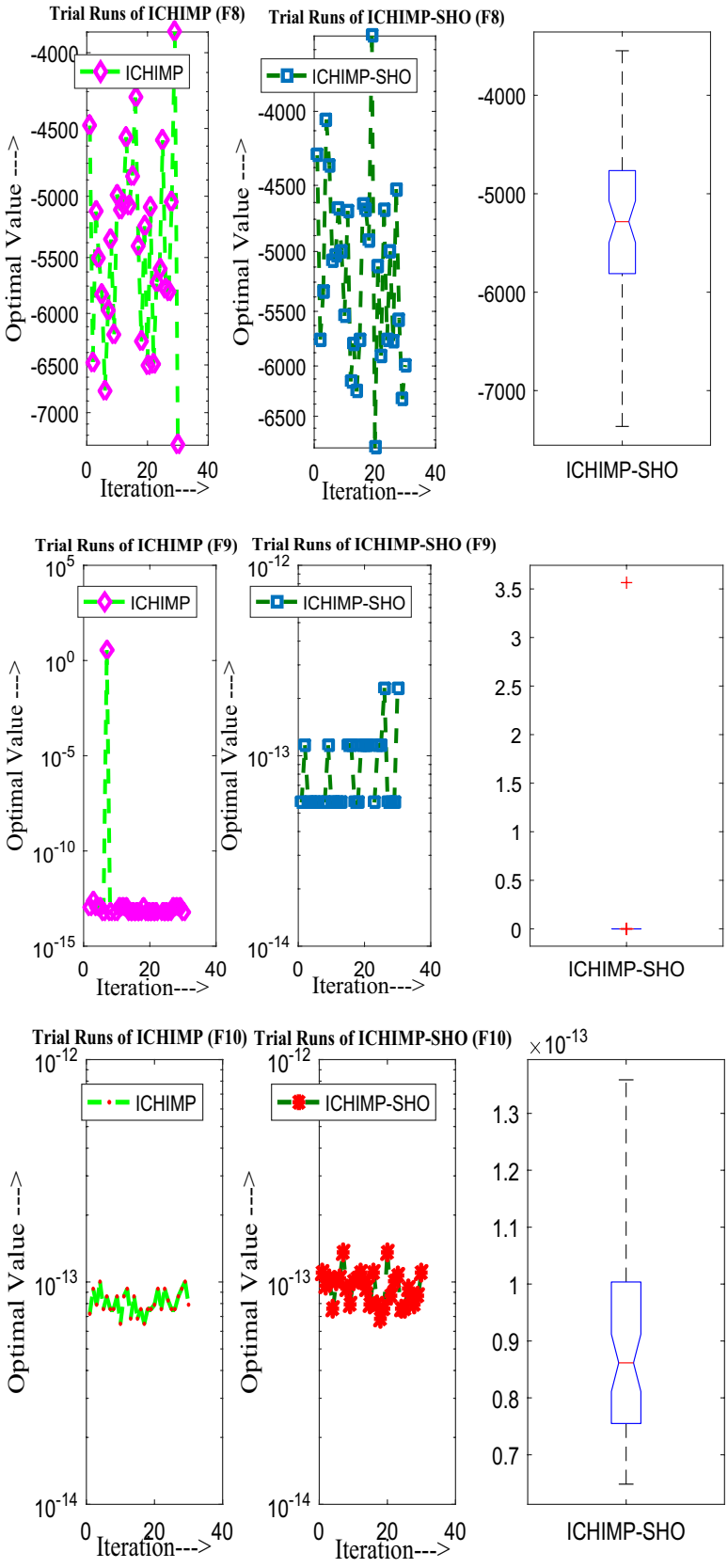
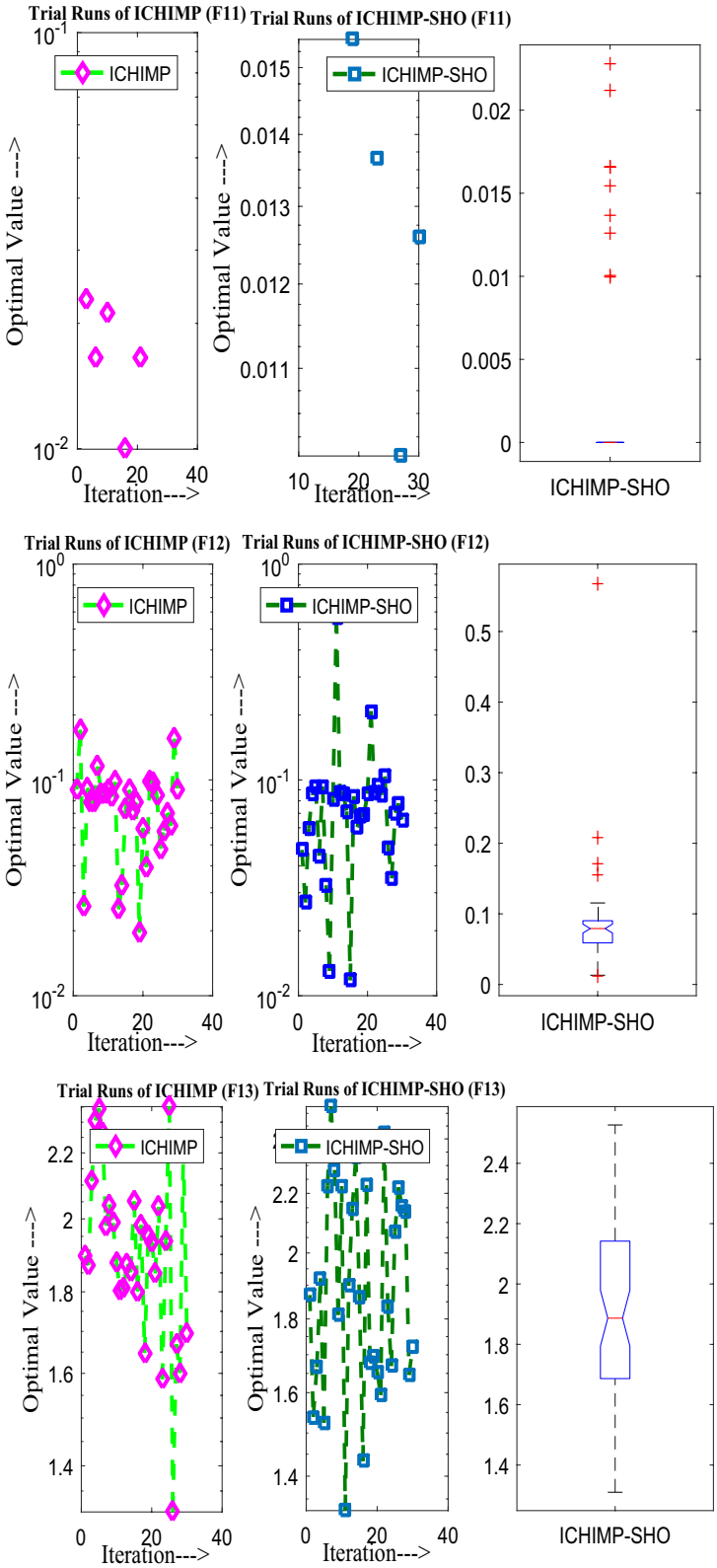


Fig. 9 Trail runs of ICHIMP and ICHIMP-SHO for MM standard benchmark functions

Fig. 9 (continued)



I_{ON}. Further, the gate all around structure improves the gate control over the tunnelling current. Dimensions: channel length, $L_g = 50$ nm, $R = 10$ nm, $T_{ox} = 2$ nm, gate metal $\Phi = 4.3$ eV, $\varepsilon_2 = 21$ (HfO_2, high k), $\varepsilon_1 = 3.9$ (SiO_2, low k), length of high-k dielectric $L_{high\text{-}k} = 10$ nm and source (p+), channel

Table 12 Test observations for fixed dimensions functions using IChimp-SHO algorithm

Function	Mean	STD	Best fitness	Worst fitness	Median	Wilcoxon rank sum test	*t* test	
						P value	*P* value	*h* value
F14	5.923306745	4.529146785	0.998003838	12.67050581	2.982105157	1.7344E−06	2.85762E−26	1
F15	0.003199196	0.006885586	0.000307505	0.020678817	0.000509082	1.7344E−06	0.016514745	1
F16	− 1.031628421	2.91482E−08	− 1.031628453	− 1.031628341	− 1.031628427	1.7344E−06	1.0841E−220	1
F17	0.397889119	3.73497E−06	0.397887373	0.397907788	0.397888221	1.7344E−06	1.4346E−147	1
F18	3.000056878	7.82165E−05	3.000000224	3.000253679	3.000022152	1.7344E−06	1.053E−134	1
F19	− 3.861720787	0.002004746	− 3.862779317	− 3.855118521	− 3.862617975	1.7344E−06	4.9726E−97	1
F20	− 3.266961533	0.070877244	− 3.321992205	− 3.114124068	− 3.32196637	1.7344E−06	5.07294E−50	1
F21	− 9.054114924	2.269865564	− 10.15311737	− 2.630423301	− 10.15104629	1.7344E−06	1.47747E−19	1
F22	− 9.791774335	1.890396917	− 10.4026378	− 2.765188383	− 10.40030086	1.7344E−06	1.05403E−22	1
F23	− 10.1738343	1.371487294	− 10.53611947	− 5.128445026	− 10.53438125	1.7344E−06	4.06341E−27	1

Table 13 Execution time for fixed dimensions benchmark problems using Imp-Chimp-SHO algorithm

Function	Best time	Average time	Worst time
F14	1.359375	1.510416667	1.734375
F15	0.25	0.288541667	0.5
F16	0.140625	0.209375	0.359375
F17	0.140625	0.222395833	0.40625
F18	0.140625	0.195833333	0.40625
F19	0.265625	0.2953125	0.515625
F20	0.375	0.428125	0.625
F21	0.375	0.4484375	0.703125
F22	0.4375	0.509375	0.640625
F23	0.546875	0.609375	0.78125

(p−), Drain (n+) doping are 1×10^{20} cm^{-3}, 1×10^{16} cm^{-3}, 1×10^{18} cm^{-3} respectively are used.

In their paper Wang et al. [119] proposed a carbon nano tube-based TFET having low doping and heterogeneous gate dielectric termed as LD-HTFET (Fig. 15) and compared its performance with CNT based TFET with high k material as gate dielectric (HK-TFET) and only heterogeneous gate dielectric based TFET (HTFET). The quantum kinetic model is used at the device level for the analysis of switching behaviour and HF figure of merits in presence of light doping and modulation of gate dielectric. The LD-HTFET is found to have better HF and switching figures. Circuit simulations with HSPICE suggested good improvements in terms of static noise margin, delay energy and power delay product. The device dimensions of the LD-HTFET include gate length of 20 nm, thickness of gate oxide of 2 nm, source/drain expansion length $L_{sd}=20$ nm, and gate oxide of $\varepsilon=3.9$ and 16 for low and high k respectively.

Patel et al. [121] proposed a nanowire TFET having heterogeneous gate dielectric and source made of low bandgap SiGe material called SiGe S NW TFET (Fig. 16) and evaluated its performance to common Si nanowire TFET for implementation of analog circuits like operational amplifiers. Due to construction source using SiGe having narrow bandgap and use of HfO_2 (having high value of k) as gate oxide towards the source-channel junction, there is 640 times increase in ON current and subthreshold swing of 6.54 mV/dec obtained as compared to 36.24 mV/dec for the conventional device. Improvement in ON current resulted in increased transconductance which resulted in better RF/analog performance. Change in diameter of the device impacts SS but variation in channel length is insignificant. Device dimensions are, length of drain/source/gate = 20 nm, diameter of nano wire = 20 nm, $t_{ox}=2$ nm, substrate doping $=1\times10^{17}$ cm^{-3}, drain doping $=1\times10^{18}$ cm^{-3} and source doping $=1\times10^{20}$ cm^{-3}.

Few researchers used muliple combination of gate metals having varring work functions. For example Raad et al. [124] proposed a hetero gate dielectric based dual-gate metal work function TFET (HGD DW TFET) which suppresses ambipolar behaviour and enhances RF figure of merits. Its structure (Fig. 17) has three gate metals having different work functions, $\Phi_1=\Phi_3=4.0$ eV and $\Phi_2=4.6$ eV. Low Φ on the drain side reduces ambipolarity and enhances ON current towards the source. SiO_2 having a lower value of k is used towards the drain end to reduce ambipolar leakage and enhance RF performance while high k (HfO_2) on the source side helps in enhancing drive current by reducing tunnelling width of the source to channel interface. The device dimensions used by them are, $L_D=L_S=100$ nm, $L_G=50$ nm which includes $t_h=2$ nm of high-density layer, $t_{ox}=2$ nm, $t_{Si}=10$ nm, length of Φ_1 and $\Phi_3=10$ nm and drain/source doping of 1×10^{20} cm^{-3}.

Bagga and Dasgupta [125] proposed Si nanowire-based triple metal gate all around TFET (TM GAA TFET) (Fig. 18). The gate wrapped around the structure with three

Table 14 Comparison for fixed dimension benchmark functions

Algorithm	Parameters	(F14–F23) Fixed dimensions benchmark functions									
		F14	F15	F16	F17	F18	F19	F20	F21	F22	F23
Lightning search algorithm (LSA) [55]	Mean	0.358172550	0.024148546	0.000534843	− 1.031628453	3.000000000	− 3.862782148	− 3.272060061	− 7.027319823	− 7.136702131	− 7.910438367
	St. deviation	0.743960008	0.047279168	0.000424113	0.000000000	3.34499E−15	0.000000000	0.059276470	3.156152099	3.514977671	3.596042666
Enhanced crow search algorithm (ECSA) [86]	Mean	1.000269	0.000327	− 1.03161	0.397993	3.00003	− 3.86061	− 3.32066	− 10.1532	− 10.44028	− 10.5359
	St. deviation	2.62E−03	1.24337E−05	2.20378E−05	1.16E−04	2.752E−05	4.53E−04	1.79E−03	8.75374E−05	1.611114E−04	4.62E−04
Transient search optimization (TSO) [87]	Mean	9.68E+000	9.01×10^{-4}	-1.06×10^{-1}	3.97×10^{-1}	3.00E+000	− 3.75E+000	− 3.01	− 10.1485	− 10.3958	10.5267
	St. deviation	3.29E+000	1.06×10–4	2.86×10^{-11}	2.46×10^{-1}	9.05E+000	$4.39\text{E}\times10^{-1}$	0.170990	$7.42\times10^{-1-3}$	1.43×10^{-2}	2.63×10^{-2}
Photon search algorithm (PSA) [40]	Mean	0.4802	0.0077	− 1.036	0.3979	3	− 3.8556	− 3.043	− 9.7302	− 9.8628	− 9.8189
	St. deviation	0.1158	0.0224	2.33×10^{-7}	1.41×10^{-7}	1.36×10^{-5}	0.0153	0.1940	1.1347	1.2894	1.8027
Hybrid Harris Hawks optimizer-pattern search algorithm (hHHO-PS) [67]	Mean	0.998004	0.000307	− 1.03163	0.397887	3	− 3.86278	− 3.322	− 10.1532	− 10.4029	− 10.5364
	St. deviation	1.57×10^{-16}	1.65×10^{-13}	1.11×10^{-16}	00	2.63×10^{-15}	2.26×10^{-15}	4.35×10^{-15}	7.47×10^{-12}	7.74×10^{-15}	7.69×10^{-15}
Spotted hyena optimizer (SHO) [63]	Mean	1.130	2.70×10^{-3}	− 1.0316	0.398	3.000	− 3.89	− 1.44E+000	− 2.08E+000	1.61×10^{1}	− 1.68E+000
	St. deviation	0.5659	5.43×10^{-3}	5.78×10^{-14}	1.26×10^{-14}	2.66×10^{-13}	1.13×10^{-11}	5.47×10^{-1}	3.80×10^{-1}	2.04×10^{-4}	2.64×10^{-1}

Table 14 (continued)

Algorithm	Parameters	(F14–F23) Fixed dimensions benchmark functions										
		F14	F15	F16	F17	F18	F19	F20	F21	F22	F23	
Harris Hawks Optimizer (HHO) [51]	Mean	1.361171	0.00035	−1.03163	0.397895	3.000001225	−3.8597664	−3.06481	−5.37397	−5.08346	−5.78398	
	St. deviation	0.95204	3.20×10^{-5}	1.86×10^{-9}	1.60×10^{-5}	4.94×10^{-6}	0.00519467	0.136148	1.227502	0.004672	1.712458	
ICHIMP-SHO (proposed algorithm)	Mean	5.923306745	0.003199196	−1.031628421	0.397889119	3.000056878	−3.861720787	−3.266961533	−9.054114924	−9.791774335	−10.1738343	
	St. deviation	4.529146785	0.006885586	2.91482E−08	3.73497E−06	7.82165E−05	0.002004746	0.070877244	2.269865564	1.890396917	1.371487294	

metals having distinct work functions helps create a barrier to suppress backward tunnelling current from drain and it also bends the energy band near-source which increases the driving current. The device is verified using Poisson's equation and Kane's model-based analytical model. In cylindrical coordinates, Poisson's equation may be written as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\varphi(r,z)}{\partial r}\right)+\frac{\partial^2\varphi(r,z)}{\partial z^2}=\frac{-qN_C}{\epsilon_{Si}}\ \text{for}\ (0\le z\le L, 0\le r\le R). \tag{33}$$

The device dimensions are, length of the channel $L=L_1+L_2+L_3=60$ nm where metal M_1 length $L_1=10$ nm, metal M_2 length $L_2=30$ nm, metal M_3 length $L_3=20$ nm, work functions $\Phi_{M1}=4.4$ eV, $\Phi_{M2}=4.8$ eV, $\Phi_{M3}=4.6$ eV, Gate Oxide thickness $t_{ox}=2$ nm and Si nano wire radius $R=10$ nm.

Many work is done on geometrical modification of the channel to make it stand vertical so that both line and point tunneling can be incorporated. Shih et al. [126] proposed a U-shaped gate heterojunction (InGaAs/GaAsSb) vertical tunnelling field effect transistor (U HJ VTFET) (Fig. 19). The structure shows BTBT normal to the Gate surface which improves the ON current. This device has a provision for independent and separate control of ON and OFF currents by insertion of a layer of spacer material at the interface of channel and drain. The Heterojunction of (InGaAs/GaAsSb) provides a very small bandgap of 0.02 eV. Performance-wise the device can achieve 520 µA/µm of drive current, an I_{ON}/I_{OFF} ratio of 10^7. The dimensions of the structure are $L_g=100$ nm, $L_d=50$ nm on both sides of gate, gate oxide (HfO_2) thickness of 2 nm, Gate metal work function 4.7 eV, Source (GaAsSb)-p + doping of 3×10^{19} cm^{-3} and drain (InGaAs)-n + doping of 2×10^{18} cm^{-3}. The device does not require any complex fabrication steps and is compatible with VLSI technology.

Kim et al. [127] proposed a TFET called VS-TFET having a vertical structure of the drain, channel and source stack with two gates on either side along with lightly doped Si to sandwich the stack from both sides (Fig. 20). The vertical channel in the device empowers it to have BTBT perpendicular to the gate field and great control over the tunnelling current. The device has a gradual doping profile for suppression of ambipolar conduction and NH_3 plasma treatment was done to have a better quality of gate dielectric. Very low SS of 17 mV/dec and high $I_{ON}/I_{OFF}=10^4$ is obtained in the device. Further it was suggested that the device can be modified for higher performance by constructing the tunnelling junction by narrow band gap materials like SiGe or Ge. The device dimensions include, source height = 100 nm with p-type doping $=5\times10^{19}$ cm^{-3}, channel height = 175 nm with p-type doping $=1\times10^{17}$ cm^{-3} and drain height = 50 nm with n-type doping $=1\times10^{20}$ cm^{-3}. Uddin Shaikh and Loan

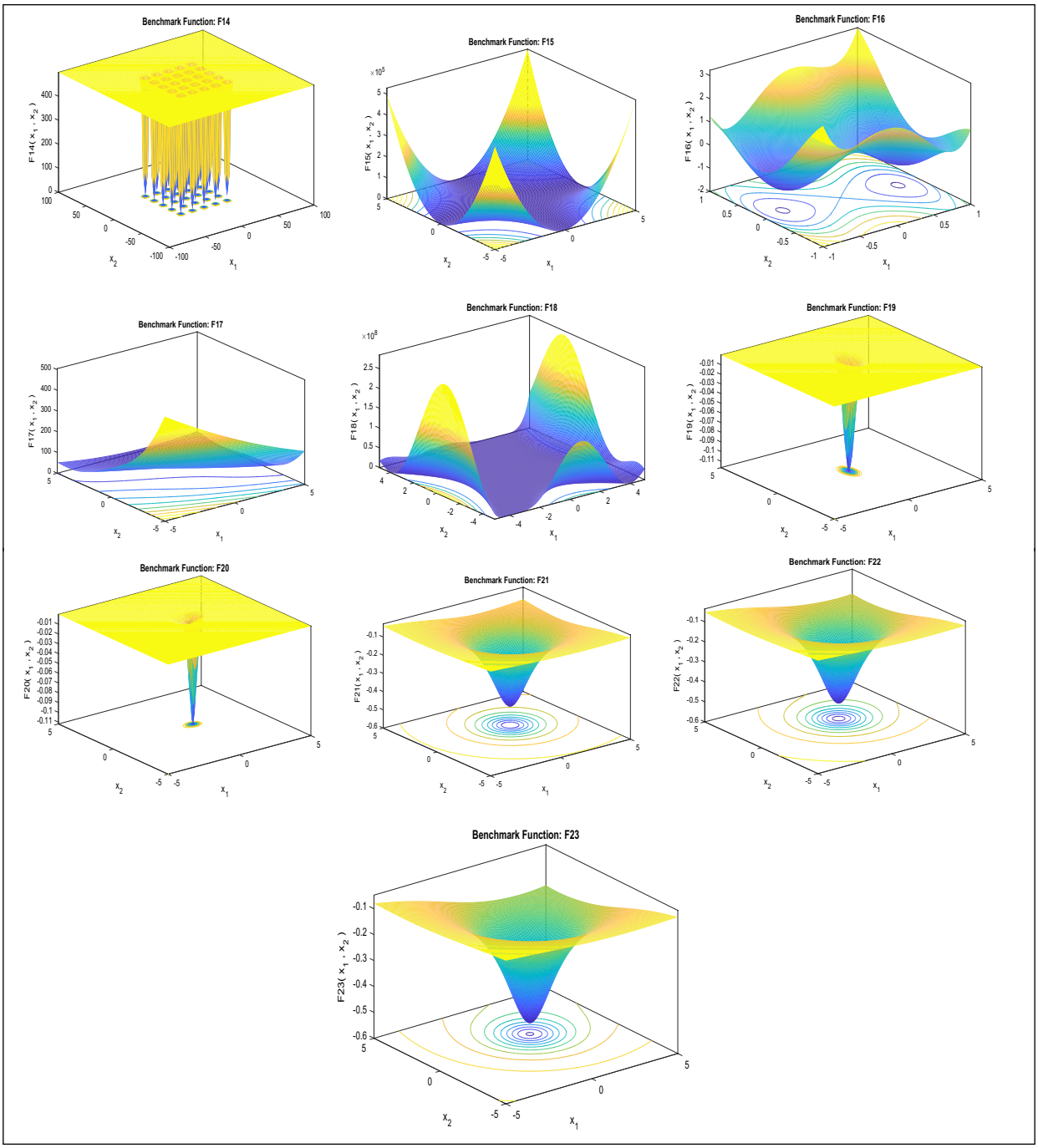
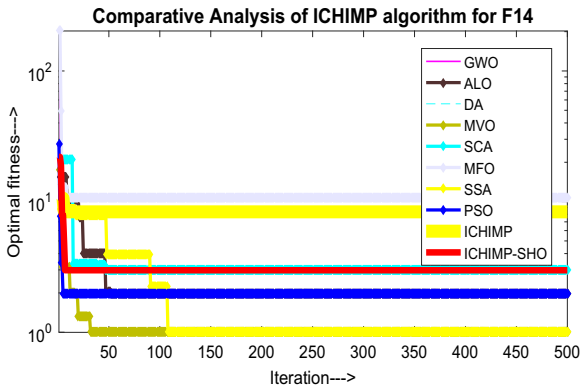
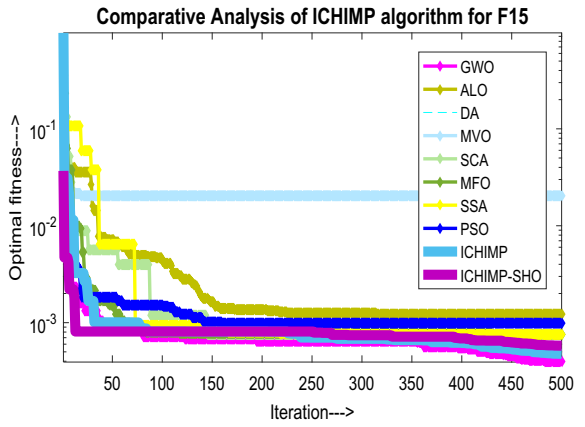
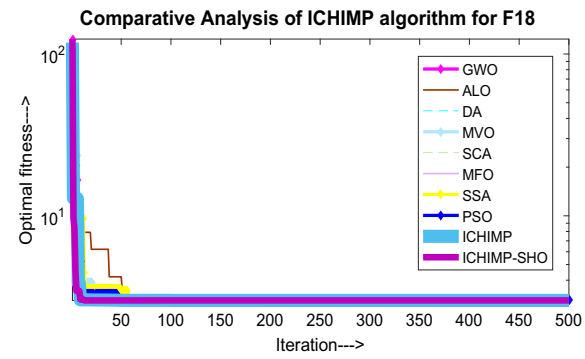


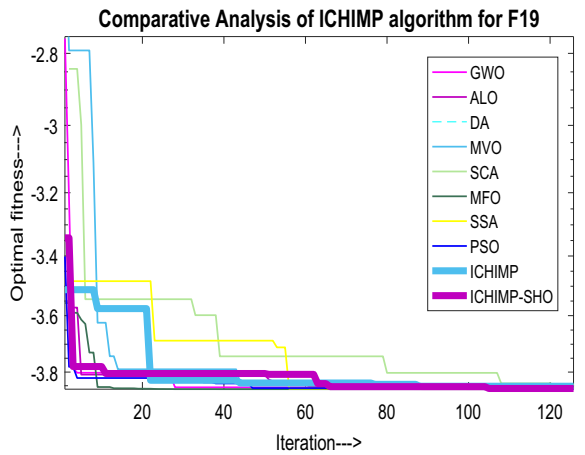
Fig. 10 3D view of fixed-dimension (FD) modal standard benchmark functions

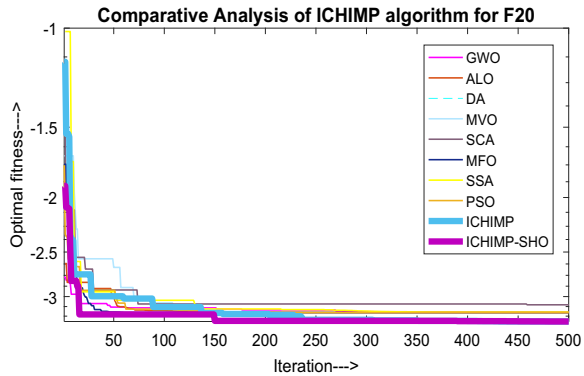
[128] proposed a drain-engineered TFET having four gates and a T shaped channel, called DE-QG-TFET as illustrated in Fig. 21. The device has a novel construction having two sources in the lateral direction and a vertically extended drain above the channel which is T shaped and is controlled by four gates. The unique construction highly suppresses ambipolar leakage compared to lateral double gate TFET. The device has double the ON current of a conventional DG TFET and ION/IOFF ratio five orders higher. Further the analog/RF figure of merits are also considerably improved. The device dimensions are, p type source doping of 1×10^{20} cm^{-1}, n type channel doping of 1×10^{17} cm^{-1}, n type drain doping of 5×10^{18} cm^{-1}, $t_{Si}=10$ nm, gate oxide SiO_2 thickness of 3 nm and gate metal work function of 4.5 eV.

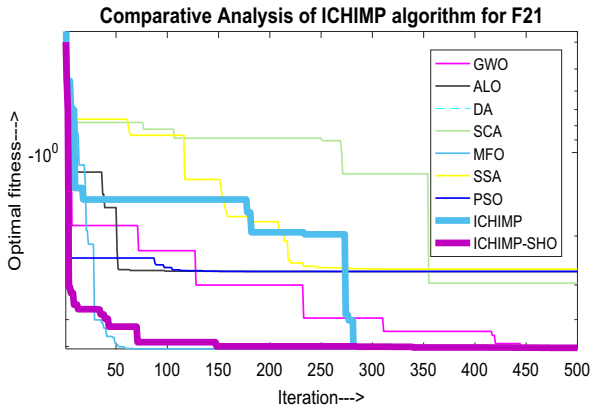


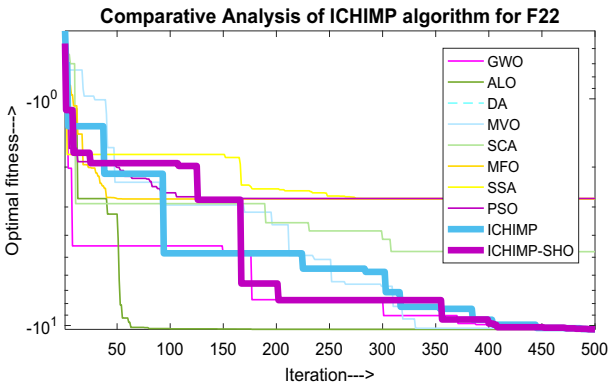












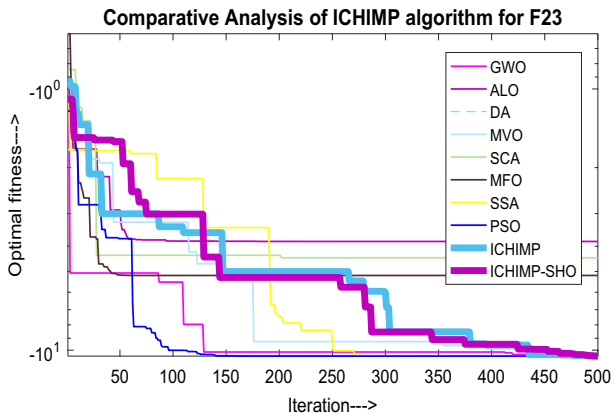
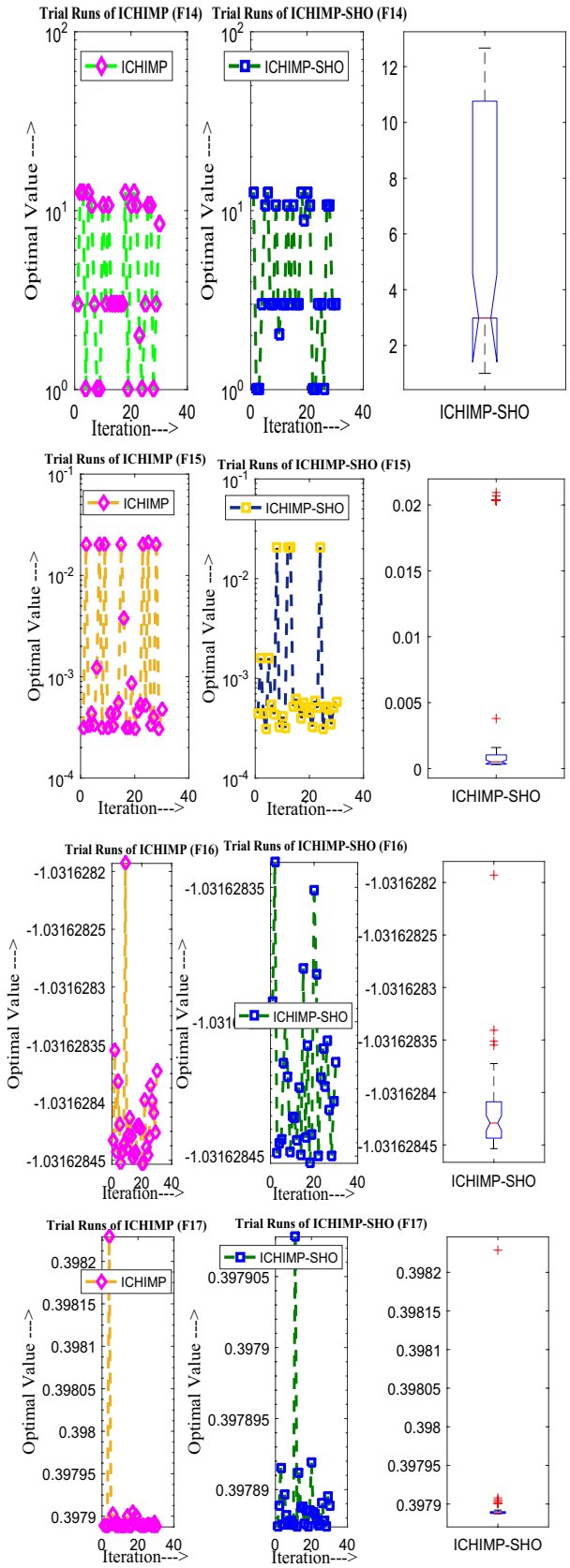


Fig. 11 Comparative curve of ICHIMP-SHO with GWO, DA, ALO, MVO, SSA and PSO for fixed standard

Fig. 11 (continued)



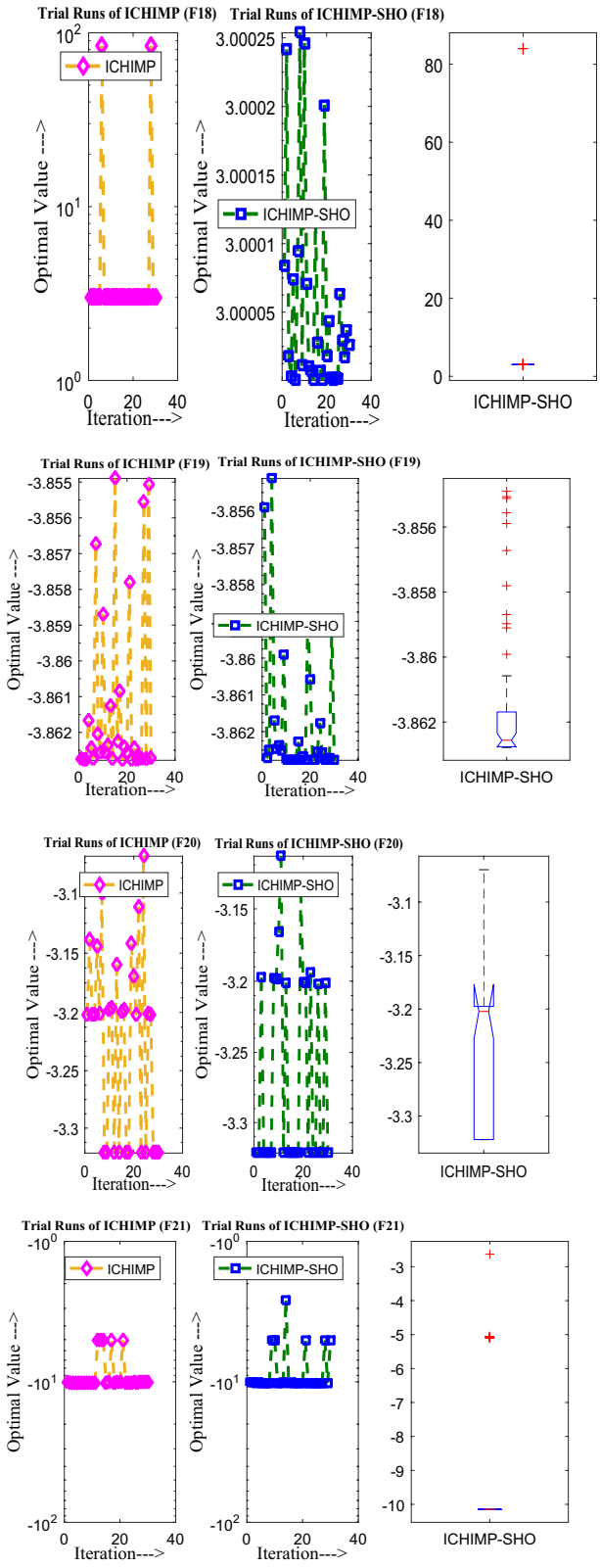


Fig. 12 Trail runs of ICHIMP and ICHIMP-SHO for fixed dimension standard benchmark functions

Fig. 12 (continued)

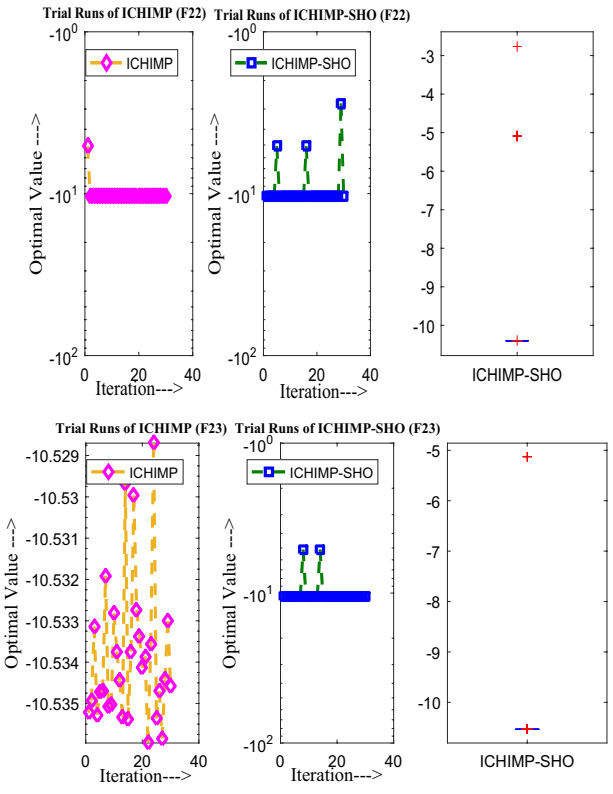


Fig. 12 (continued)

Kumar et al. [129] proposed a-Si nanotube-based TFET having two gates one running through the centre of the channel as a core and another wrapped around outside the channel as a shell (Fig. 22). The device with both inner core gate as well as outer shell based wrapped all-around gate gives better control over the channel and improves drive capacity. It is compared with conventional nanowire TFET for analog and RF performance and found to be much superior. Its vertical device geometry helps in enhancing the ON-state current to a great extent. The dimensions used are channel thickness = 50 nm, t_{ox} = 1 nm, radius = 5 nm, source doping = 1×10^{20} cm^{-3}, drain doping = 5×10^{18} cm^{-3}, channel doping = 1×10^{17} cm^{-3} and gate work function = 4.4 eV.

Research is also done to include the charge plasma based junction less technology to reduce various leakages and minimise fabrication complexity and cost. Nigam et al. [130] designed a TFET based on charge plasma technology having a control gate of dual metals, termed as DMCG-CPTFET (Fig. 23). The device is junction less and based on charge plasma-based electrical doping to reduce the fabrication complexity. The p + source is formed by the deposition of platinum (Φ = 5.93 eV) and the n + drain is formed by the deposition of hafnium (Φ = 3.9 eV) over Si. The gate is made of three metals with different work functions. Metal M_1 (Φ_1) called tunnelling gate on the source side, M_3 (Φ_3) called auxiliary gate on the drain side and M_2 (Φ_2) called control gate at the centre. $\varphi_1 = \varphi_3 < \varphi_2$ is taken for best performance. The tunnelling gate improves ON state performance while the auxiliary gate suppresses ambipolarity. The device dimensions are, length of gate L_g = 50 nm, thickness of Silicon layer t_{Si} = 10 nm, thickness of oxide layer t_{ox} = 1 nm, tunnelling gate length L_1 = 10 nm, control gate length L_2 = 25 nm and auxiliary gate length L_3 = 15 nm.

Yadav et al. [122] proposed doping less TFET having heterogeneous gate dielectric and work function engineering at both gate and drain called HGD DE DMG DL TFET (Fig. 24). The device is doping less based on the charge plasma technology which has large ease in fabrication. Here dual work function is used at two places; over drain it reduces ambipolarity and a gate terminal, works for the enhancement of ON-state current. Again, there is a hetero gate dielectric whose combined effect along with work function modulation both at gate as well as drain results in a reduction in subthreshold slope, threshold voltage and

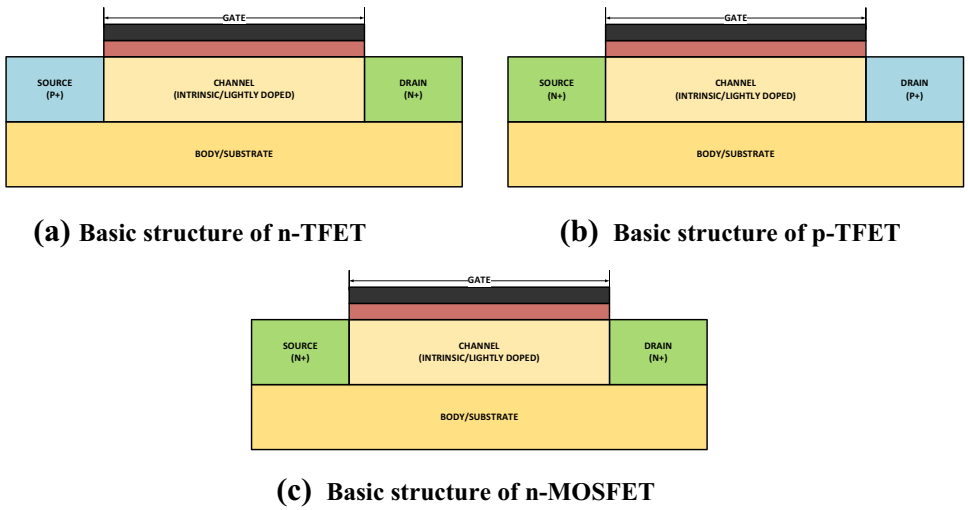


Fig. 13 **a** Basic structure of n-TFET. **b** Basic structure of p-TFET. **c** Basic structure of n-MOSFET

improved high-frequency responses. The device dimensions are the length of drain metal $L_D = 40$ nm with $\Phi = 3.9$ eV, length of the extended portion of drain metal $L_B = 10$ nm with $\Phi = 4.3$ eV, length gate metal $L_G = 40$ nm with $\Phi = 4.6$ eV, length of extended portion gate metal $L_C = 10$ nm with $\Phi = 4.0$ eV, length of source metal $L_S = 50$ nm with $\Phi = 5.93$ eV, the thickness of silicon body $t_{Si} = 10$ nm and thickness of oxide layer $t_{ox} = 1$ nm.

Yadav et al. [131] proposed a TFET having electrical doping, gate underlapping and heterogeneous body with low bandgap SiGe at source and Si at drain and channel. The device called HM-GUL-ED-TFET is shown in Fig. 25. The gate under-lap helps in suppressing the ambipolarity and gate leakage current (I_g). The $Si_{0.5}Ge$ material having narrow bandgap at the source helps in improving DC and RF figures of merit. Further the device uses charge plasma-based electrical doping which eases fabrication drastically. The device dimensions include length of electrical drain/source $L_{ED} = L_{ES} = 50$ nm with work function = 4.5 eV, $t_{Si} = 10$ nm, $t_{ox} = 1.5$ nm, control gate length $L_{CG} = 30$ nm, gate underlap $L_{GUL} = 20$ nm and substrate doping $= 1 \times 10^{15}$ cm^{-3}.

Devi and Bhowmick [132] proposed a junctionless TFET with a SiGe n + pocket doping near source end called JL-TFET (Fig. 26) which can be applied for the construction of efficient inverter circuits. The device has two metal gates, a fixed gate and a control gate having different work functions. It uses junction less technology, through which its N + -N + -N + structure is converted into PIN using suitable voltage variations at the two gates. A SiGe N + pocket is used near the source end which generates a path for tunnelling current transverse to the gate oxide in addition to the usual lateral path and drastically increases ON state current to about 5.7×10^{-4} A. By varying the fixed gate and control gate work functions to 5 and 4.5 eV respectively, close to 43.6 mV/dec of subthreshold swing value may be attained. Further, RF evaluation also shows superior performance concerning conventional JL-TFET. Dimensions of the device are, doping for source, channel and drain is 1×10^{17} cm^{-3}, gate oxide thickness $T_{ox} = 2$ nm, channel length $L_g = 35$ nm, Si thickness $T_{Si} = 30$ nm, pocket length 20 nm and thickness 10 nm.

Tripathi et al. [133] proposed a junction less TFET having a single gate and a SiGe based pocket near source called JLSGTFET (Fig. 27). The device utilizes junction-less technology for ease of fabrication. Low bandgap SiGe pocket between source and channel reduces the switching capacitance of the device. Ge mole fraction $x = 0.3$ is used, which improves various electrical parameters like transconductance, junction capacitance and leakage current.

The device attains I_{ON}/I_{OFF} ratio of 2×10^8, steep subthreshold slope of 52.3 mV/dec and DIBL = 2.1 mV/V at 300 K. Furthermore, the device parameters are investigated for a wide temperature range from 250 to 400 K and the variations are found to be very low, which makes it ideal for sub 20 nm, ultra-low power, digital applications. The device dimensions are, gate length $L_g = 15$ nm, SiGe pocket length of 5 nm, channel length of 15 nm, drain/source height of 20 nm and source/drain doping of 1×10^{20} cm^{-3}. Kumar and Raman [134] proposed a charge plasma-based TFET using cylindrical Si nanowire. It uses drain, source and

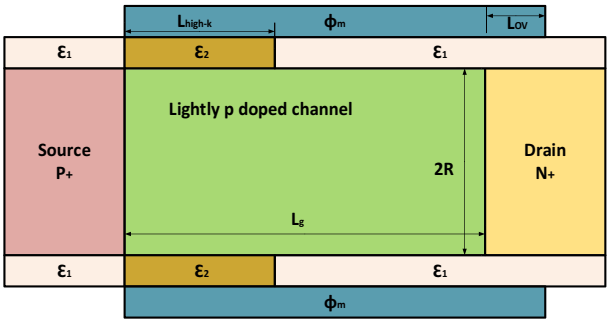


Fig. 14 Cross-sectional view of GDO HD GAA TFET

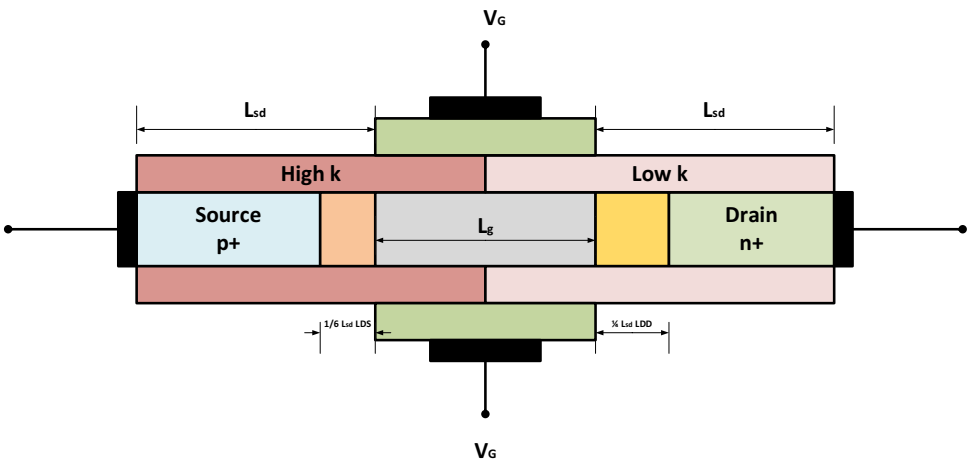


Fig. 15 Cross-sectional view of LD HTFET

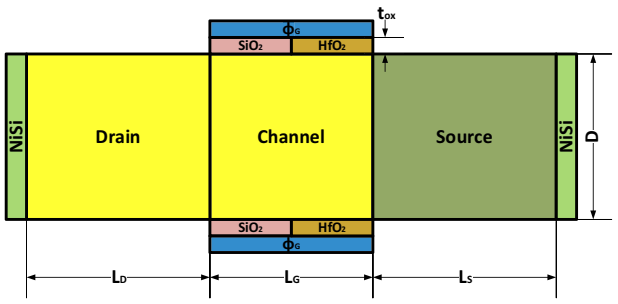


Fig. 16 Basic layout of heterogeneous gate dielectric, nanowire TFET with source made of SiGe

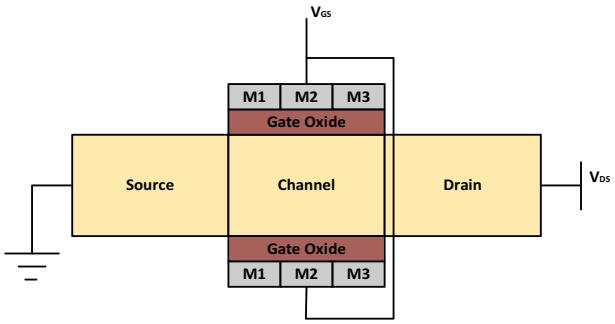


Fig. 18 Cross-sectional view of Si nanowire-based triple metal gate all around TFET (TM GAA TFET)

gate electrodes having specific work functions wrapped all around the intrinsic nanowire for inducing the vertical PIN structure. The 2D view of the proposed structure is shown in Fig. 28. The device is investigated for the effects of interface trap charges (ITC) at the channel dielectric interface and the associated noise behaviour is studied. It is found that the ITCs of all polarities degrade I_{ON}/I_{OFF} ratio however positive ITCs improve drive current as well as noise behaviour. The device dimensions are, length of source/drain 100 nm, channel length of 50 nm, radius of NW = 5 nm, $T_{OX} = 2$ nm, gate, source and drain work functions of 4. 5, 5. 93 and 3. 9 eV, respectively.

Buried Oxide (BOX) and Selective Buried Oxide (SELBOX) technology has been incorporated in few researches to enhance the performance of the TFETs. Bhattacharjee et al. [135] proposed a new TFET having a single gate and broken or splitted drain called SD-SG TFET as shown in Fig. 29. In the device drain doping engineering is used to create a splitted or parted drain in which one portion is highly doped and the other lightly, they are arranged in descending order of doping. The parted drain structure greatly reduces ambipolar conduction. Four devices with different relative positioning of the splitted drain (SD)

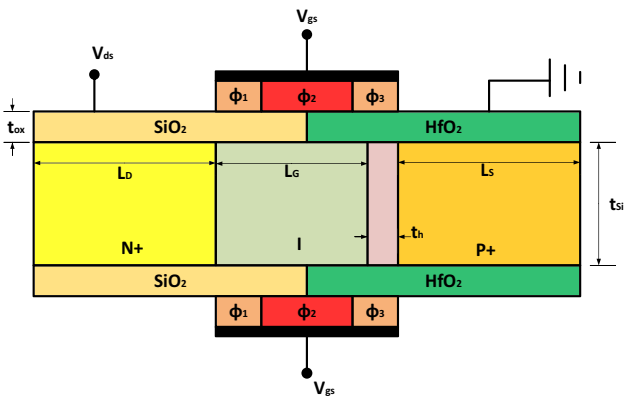


Fig. 17 Cross sectional view of HGD DW TFET

are analysed and evaluated for performance. One has the entire drain bisected into high and low doping called SD SG TFET and the others have either SD at the top called TSD SG, SD at the bottom called BSD SG or SD at the middle, called MSD SG TFET. The BSD-SG TFET showed a maximum I_{ON}/I_{OFF} ratio among all structures. All the structures showed better performance compared to conventional TFETs. The dimensions include source doping $N_S = 1 \times 10^{20}$ cm^{-3}, channel doping $N_{ch} = 1 \times 10^{17}$ cm^{-3}, drain doping $N_{D1} = 5 \times 10^{18}$ cm^{-3} and $N_{D2} = 1 \times 10^{17}$ cm^{-3}, drain length $X_d = 100$ nm, source width $Y_s = 60$ nm, channel width $W = 60$ nm, $T_{si} = 60$ nm and $T_{ox} = 1$ nm.

Mitra and Bhowmick [120] designed buried oxide (BOX) based TFET having the presence of gate on some portions of both source as well as channel called GOSC TFET (Fig. 30) and compared its performance with conventional FG SOI TFET and GOS SOI TFET when traps are there at all the Si to Oxide interfaces. The effects of trap charges present at the interface of gate oxide and Si and BOX & Si on subthreshold swing, drive current, ambipolarity, C_g and f_T is evaluated for all three devices. The traps at the interface of BOX to Si increases ambipolar conduction while traps at the interface of gate oxide to Si reduces ON-state current, the effect of the former is observed to be much more severe. It is found that GOS SOI TFET is most immune to the adverse effects of interface traps. For the GOS TFET performances are observed to be much better with SS of 61. 5 mV/V, V_T of 0. 6 V and I_{ON} of 37. 5 μm/μA. The device dimensions are, source/drain length = 30 nm, p + source (10^{21} cm^{-3}), p channel (10^{16} cm^{-3}), n + drain (5×10^{19} cm^{-3}), Gate work function = 4. 2 eV, $T_{ox} = 2$ nm, gate channel overlap $L = 10$ nm and $L_{UN} = 30$ nm.

Vanlalawpuia and Bhowmick [136] proposed a TFET with L shaped buried oxide layer (BOX) with Ge source region having a very thin δ-doped layer within it (Fig. 31). The use of low bandgap Ge material for source enhances the drive current and the use of δ-doped layer reduces OFF state leakage and ambipolarity. Further the source is positioned vertically below the gate channel stack which results

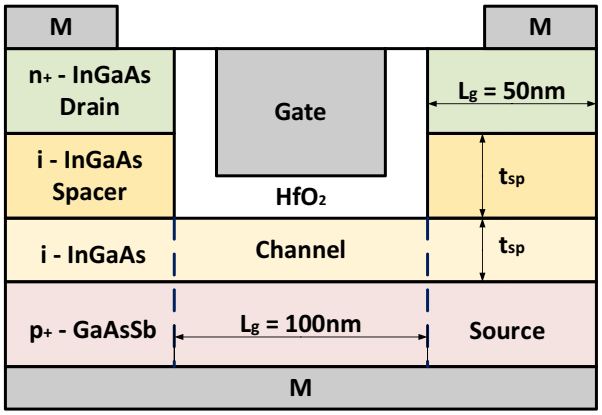


Fig. 19 U-shaped gate heterojunction vertical tunnelling field effect transistor (U HJ VTFET)

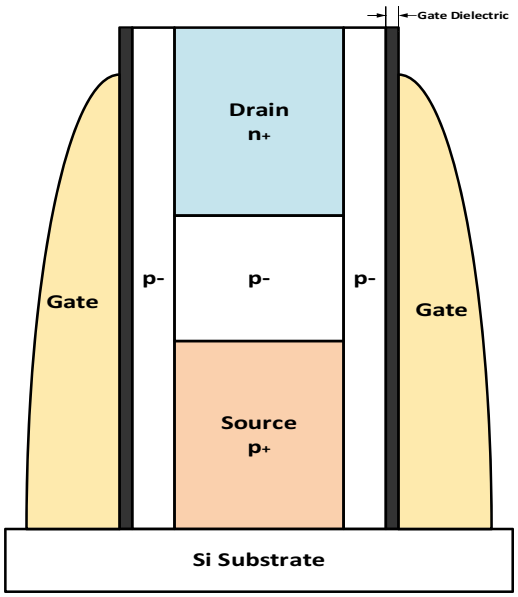


Fig. 20 Structure of the VS-TFET having double gate and normal channel with lightly doped Si on both sides

in vertical tunnelling current or BTBT perpendicular to the gate oxide, this results in very high ON current. The sizes and dimensions of each region are fixed after optimization using simulation software. The dimensions include the thickness of δ layer = 1 nm, L_{UC} = 15 nm, Ge source thickness of 16 nm, t_{OX} = 2 nm, source length of 15 nm, drain length of 10 nm and gate length of 30 nm. The source, channel, drain and δ layer doping are 1×10^{20} cm^{-3}, 1×10^{16} cm^{-3}, 5×10^{18} cm^{-3} and 5×10^{16} cm^{-3}, respectively.

Ahn et al. [137] proposed an InGaAs based planer TFET structure having Zn diffused source and W/ZrO_2/Al_2O_3 gate stack (Fig. 32). Narrow and direct bandgap, group III–V material InGaAs is used for the channel to enhance BTBT and hence the ON current. The mole fraction for In is optimised in such a way that a quantum well (QW) is formed which simultaneously suppresses OFF current while maintaining high I_{ON}. Zn is diffused in the source region to achieve an abrupt doping profile for high BTBT. ZrO_2/Al_2O_3 gate stack is used to have optimum gate control over the tunnelling current while maintaining low equivalent oxide thickness (EOT). The device dimensions are optimised for high performance in low power digital circuits.

Ghosh and Bhowmick [138] proposed a TFET device mounted on a selective buried oxide (SELBOX) and having a heterogeneous junction with the presence of a thin δp^+ layer of SiGe at the interface of source and channel (Fig. 33). The device is analysed with encouraging results for the impact of flicker noise due to the presence of Gaussian as well as uniform traps, which are a major concern for most TFET devices. The device uses selective BOX having a gap in place of fully depleted (FD) BOX because it reduces OFF current. It uses a low bandgap δ layer of SiGe which enhances BTBT and high k gate dielectric which improves I_{ON}. The mole fraction of the δ layer, its position as well as the position of the SELBOX gap are all optimised through simulations. The device dimensions include channel length of 30 nm, δ layer thickness of 3 nm, source/drain length of 35 nm, SELBOX thickness of 10 nm with gap length of 2 nm. The source, channel, drain and δp^+ layer doping of 1×10^{20} cm^{-3}, 1×10^{16} cm^{-3}, 5×10^{18} cm^{-3} and 1×10^{18} cm^{-3}, respectively.

Singh et al. [139] proposed a TFET on SELBOX with the partial ground plane (PGP) having a gate dielectric stack of HfO_2 over SiO_2 and low bandgap Ge as the source material, termed as GSHJ-PGP-STFET (Fig. 34). The device uses narrow bandgap Ge material for source to enhance BTB tunnelling. The HfO_2/SiO_2 stack provides for optimum gate control of the tunnelling phenomena and its combined effect with Ge source enhances ON-state current. The SELBOX structure with PGP suppresses OFF state leakage and maintains a good I_{ON}/I_{OFF} ratio. The device is found to be much superior to conventional SELBOX TFET and FD BOX TFET in terms of average SS, I_{ON} and I_{ON}/I_{OFF} ratio.

The device dimensions include channel length of 40 nm, source/drain length of 30 nm, SELBOX thickness of 10 nm with a gap width of 4 nm, high and low k gate oxide thicknesses of 2 and 1 nm, respectively. The doping concentrations of source, channel, drain, and PGP region are 10^{20}, 10^{16}, 5×10^{18} and 5×10^{18} cm^{-3}, respectively.

Research is also done to apply the properties of a TFET to make a biosensor. In this direction Verma et al. [140] proposed a TFET based label-free bio-molecule sensor which utilizes vertical dielectric modulation termed as V DMTFET (Fig. 35). The previously established lateral DMTFET (L-DMTFET) is compared with performance. A heavily doped n + pocket is introduced in the device for vertical

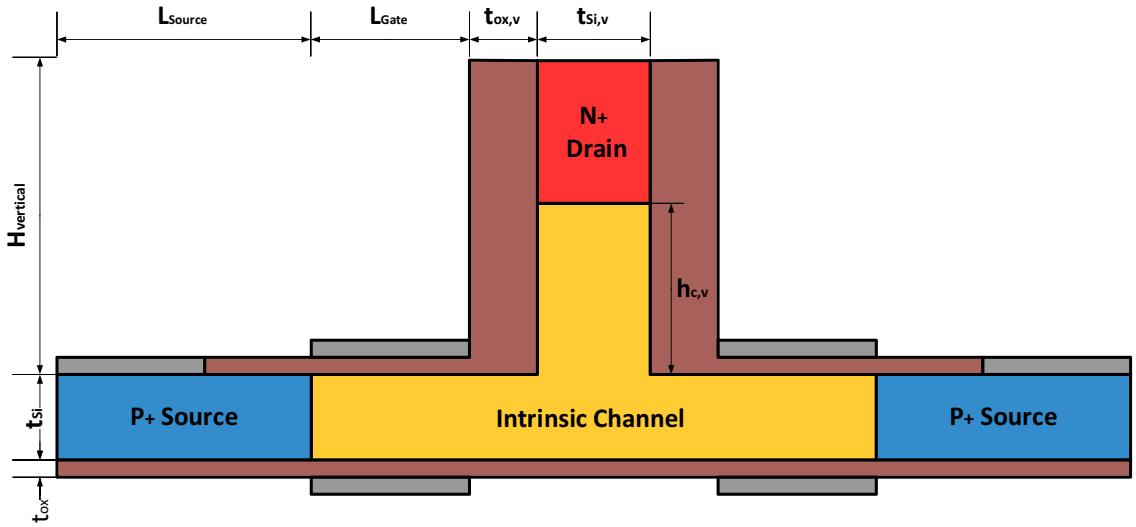


Fig. 21 Drain-engineered, T channel, four gates based TFET (DE-QG-TFET)

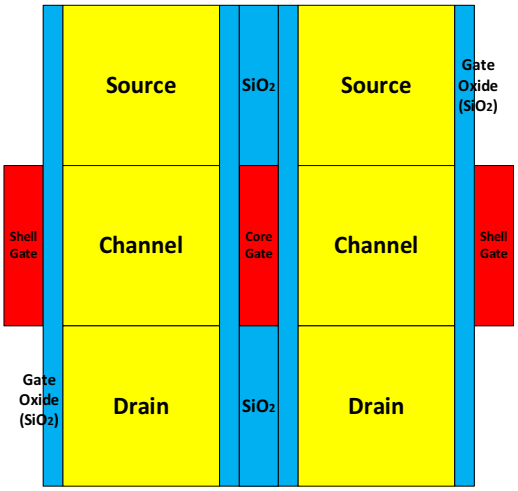


Fig. 22 Basic structure of core and shell gate-based Si nanotube TFET

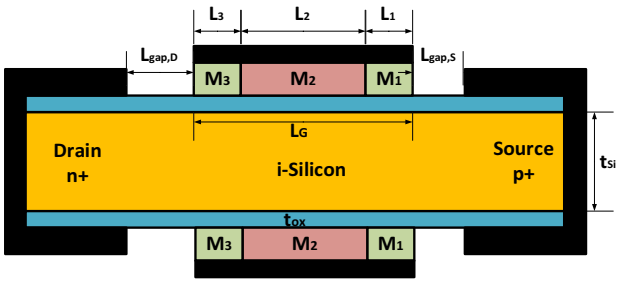


Fig. 23 Cross-sectional view of charge plasma based DMCG CPT-FET

tunnelling along with lateral tunnelling which increases the ON-state current greatly and reduces subthreshold swing. A gate to source overlap is also there for improving sensitivity. There are two nanocavities in the device the larger one $L_{c2}=15$ nm below the front gate and $L_{c1}=10$ nm below the back gate for sensing biomolecules. Filled cavities give higher sensitivities, gate metal M_1 ($\Phi_{M1}=4.3$ eV) is used near drain end and M_2 ($\Phi_{M2}=3.8$ eV) near source end to enhance the sensitivities. The device dimensions are, length of channel $L_{ch}=42$ nm, lengths of the source and drain $L_s=L_d=20$ nm, body thickness $t_{Si}=10$ nm, oxide $t_{ox}=6$ nm and cavity thickness $t_{cavity}=5$ nm. Doping of source, channel and drain is 5×10^{19}, 1×10^{12}, and 5×10^{18} cm^{-3} respectively and n + pocket doping is 5×10^{19} cm^{-3}.

10 Comparison of existing TFET architectures

A detailed parametric analysis along with applications of promising TFET configurations are presented in Table 15. The SD-SG TFET [135] shows the highest ON state current due to its drain doping engineering and splitted drain architecture. Its drain consists of a stack of highly doped region above a lightly doped region, which increases the tunnelling width of the drain channel interface and increases the drive current and reduces ambipolar leakage. Further when the relative position of the splitted drain is varied for channel maximum ON-current and I_{ON}/I_{OFF} ratio is found when it is at the bottom. The VS-TFET [127] promises to show the minimum sub-threshold slope of 17 mV/dec but its feature size is very large which will hamper the packing density. It

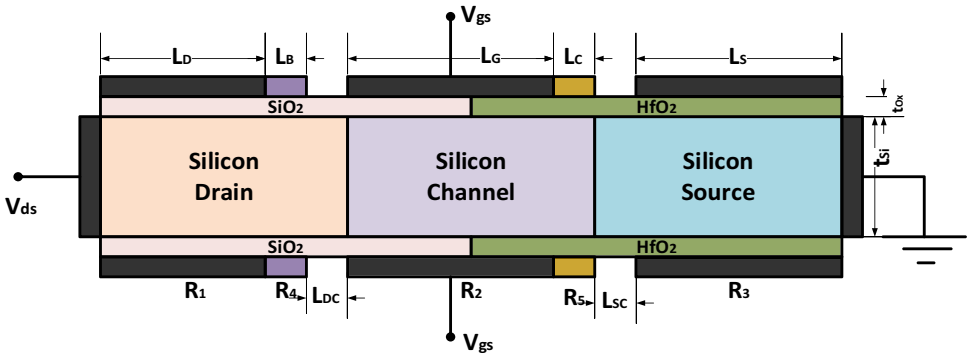


Fig. 24 Structure of gate-drain Φ engineered, doping less TFET with dual gate dielectric (HGD DE DMG DL) TFET

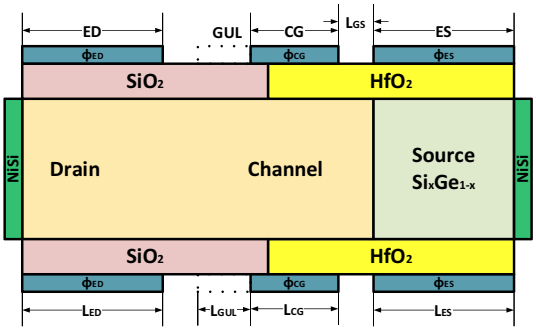


Fig. 25 Cross sectional view of HM GUL ED TFET

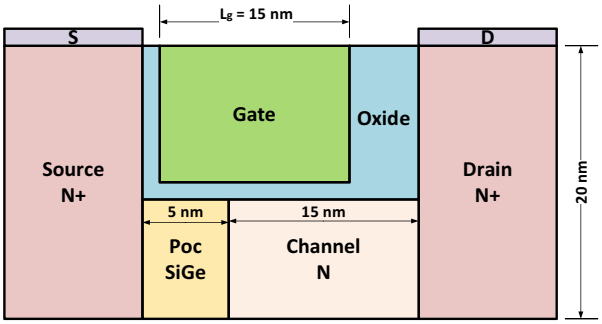


Fig. 27 Cross sectional view of the JLSGTFET with SiGe pocket near source

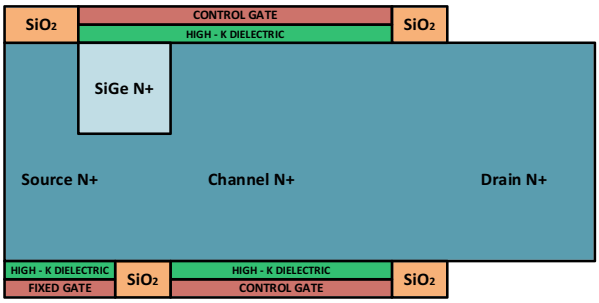


Fig. 26 Basic structure of SiGe n + pocket JL-TFET

has a vertical structure with channel above and on the sides of the source and a dual gate which controls both lateral and transverse tunnelling, which reduces the SS, but the structure has the drawback of least I_{ON}/I_{OFF} ratio. The HM-GUL-ED-TFET [131] has an SS of 19.13 mV/dec and I_{ON}/I_{OFF} ratio of 2.73×10^{11} at 30 nm technology node. It is found to be one of the promising candidates for ultra-low power portable devices for analog/RF applications. The device uses gate underlap towards drain side to suppress the ambipolar leakage, gate leakage and low bandgap material for source which enhances band to band tunnelling (BTBT) and hence ON current. Thus, as a combined effect the I_{ON}/I_{OFF} ratio is boasted, and SS made steeper. Further the device uses charge plasma-based electrical doping which reduces fabrication complexity and junction leakage. The V-DMTFET [140] shows good results as TFET based label-free biomolecule sensor which senses specific biomolecules based on the relative change in the dielectric constant of the sensing cavities due to the presence of target biomolecules (known dielectric constant). It shows SS of 47 mV/dec and good I_{ON}/I_{OFF} ratio. The JLSGTFET [133] has the lowest value of drain induced barrier lowering (DIBL) of only 2.1 mV/V and reasonable other performance parameters like SS, I_{ON} and I_{ON}/I_{OFF} at 15 nm technology node. It uses junction less technology with a p + $Si_{0.7}Ge_{0.3}$ pocket between the n+ source and n− channel which drastically improves the performance parameters.

A comparison of analog/RF performance parameters of some of the most efficient devices is represented in Table 16. The SiGe-S-NW-TFET [121] shows the highest cut-off frequency and GBP of 950 GHz and 549 GHz respectively. It uses Si nanowire technology with narrow bandgap SiGe material for source and hetero gate dielectric with high-k HfO_2 near source end for performance improvement. It also exhibits the lowest transit time of 0.9 ps. The GDO– HD–GAA-TFET [123] with gate-drain

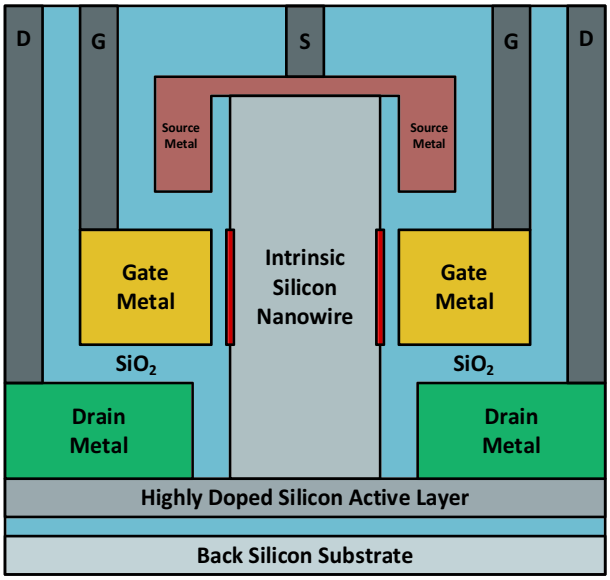


Fig. 28 2D schematic representation of Si nanowire doping less vertical TFET

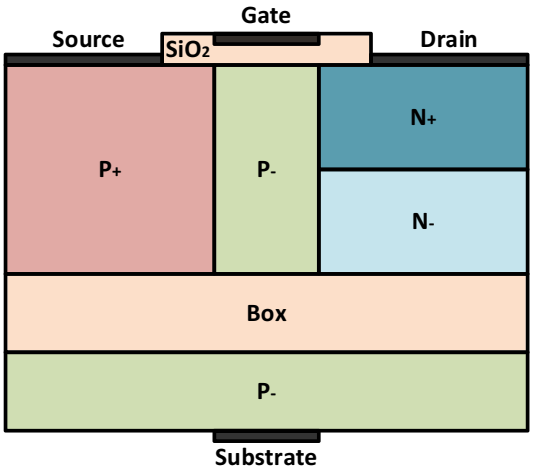


Fig. 29 The SD-SG TFET structure with the entire drain bisected into high and low doped parts

overlap, heterogenous gate dielectric and cylindrical gate all around structure has the highest value of transconductance of 0.53 mS.

The device offers high ON current and good gate control along with reduced ambipolarity, but it has low cut-off frequency and poor transit time response. The JL-TFET [132] using junction less technology along with low bandgap SiGe pocket near source exhibits moderate transconductance of 0.1mS and f_T of 100 GHz. Cut of the frequency of 130 GHz is obtained by D GAA CS NT TFET [129] with its cylindrical core–shell dual-gate all around structure, but its transconductance is not up to the mark, further its complex structure and fabrication complexity does not justify the performance improvement. The HM-GUL-ED-TFET [131] also shows good f_T and moderate gain-bandwidth product. It uses charge plasma-based electrical doping which eases fabrication and reduces leakage.

11 Conclusion

In the proposed research, the hybrid variants of chimp optimizer has been successfully developed, which are based on wholesome attitude roused by amazing thinking and hunting ability with sensual movement for finding optimal solution in global search region. The newly developed improved variant of Chimp optimizer has been successfully tested for various engineering design and standard benchmark optimization problems, which includes unimodal, multi-modal and fixed dimensions benchmark problems. After validating the efficiency of the proposed optimizers for standard benchmarks and engineering design problems, it has been experimentally observed that both the variants are competitive foe finding the solution within the global search space. Based on experimental results and comparative analysis with other methodologies, it has been recommended that the proposed hybrid variants can be universally accepted to solve any of the hard engineering design challenges in global search space. The chimp optimizer is found most suitable to optimize TFET structure in terms of dimension and performance parameters that can be a worthiest replacement candidate of MOSFET in ultra-low power, highly scaled down (high packing density) VLSI circuits. The paper also gives a comprehensive review of the

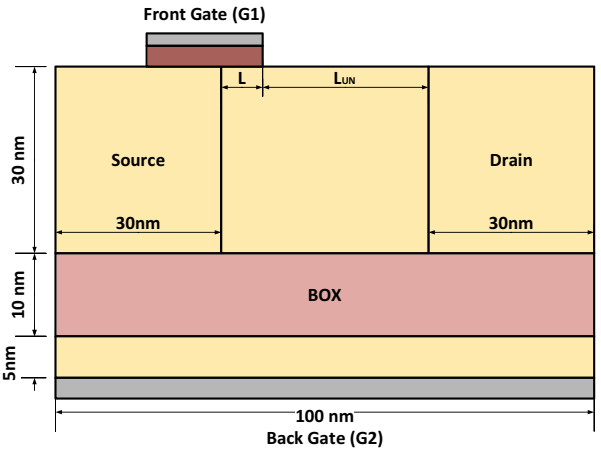


Fig. 30 Buried oxide based TFET with gate on both source and channel (GOSC TFET)

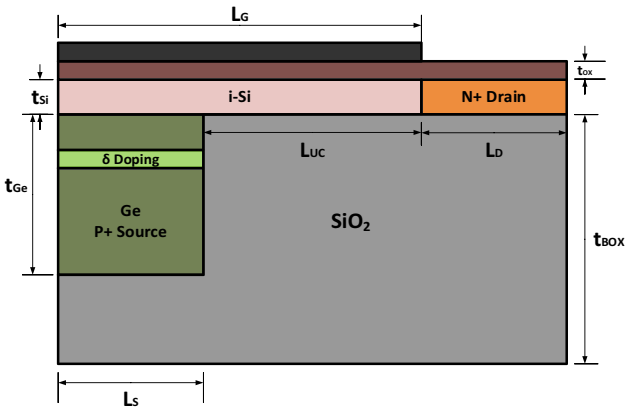


Fig. 31 Vertical TFET with Ge source having δ-doped layer and L shaped BOX

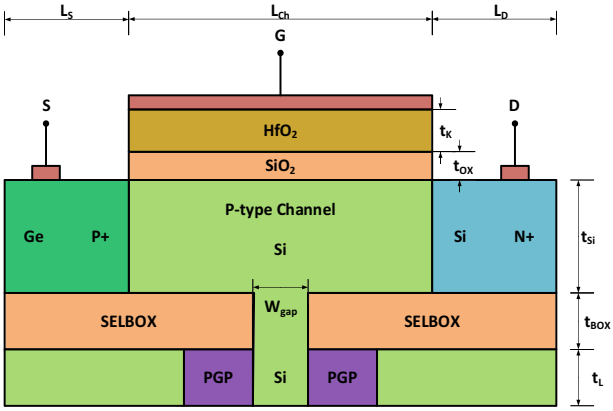


Fig. 34 Cross-sectional view of GSHJ-PGP-STFET [139]

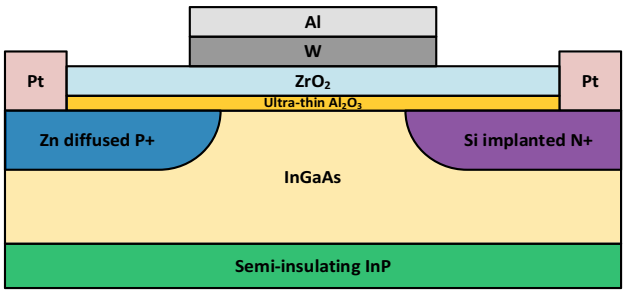


Fig. 32 InGaAs based planer TFET with Zn diffused source and W/ZrO_2/Al_2O_3 gate stack

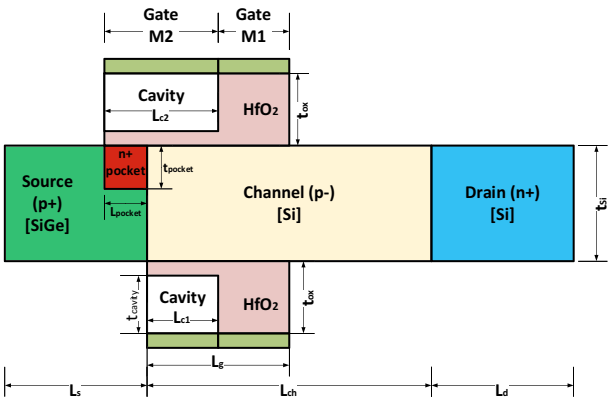


Fig. 35 Structure of vertical DMTFET based bio-molecule sensor

recent advances in TFET technology employing geometrical modifications, gate metal work function engineering, hetero source/channel/drain material with bandgap engineering, multigate, gate dielectric engineering, junction-less techniques etc. for improvement of performance parameters like steep SS, low ambipolarity, high drive current and I_{ON}/I_{OFF} ratio. It also analyses the devices based on different analog/RF performance parameters like transconductance, cut-off frequency, GBP, and transit time to suggest the most promising device configuration. Further, it investigates the devices from an application point of view like low power battery operated devices, digital, analog/RF circuits, and biomolecule sensors. The VS-TFET has least SS but low I_{ON}/I_{OFF} ratio and large feature size which restricts its applications. At 50 nm node, the SD SG TFET shows the highest ON current and I_{ON}/I_{OFF} ratio due to its splitted drain and relative positioning of drain,

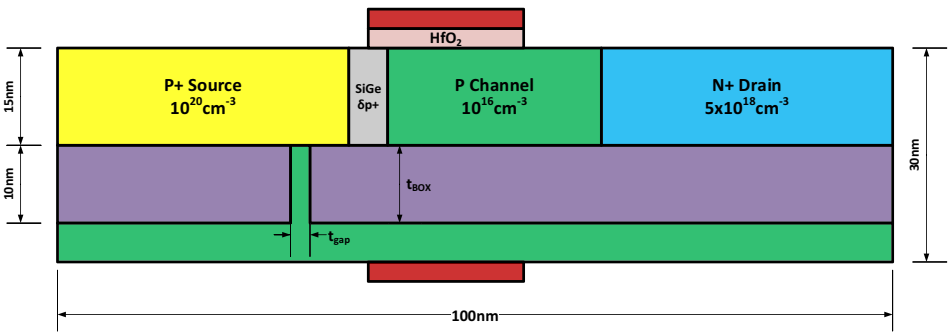


Fig. 33 SELBOX based TFET with p + SiGe layer at source channel interface

Table 15 Performance comparison of TFET architectures for DC parameters and applications

Device	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)	Channel length (nm)	Application
HGD DW TFET [124]	1.21×10^{-4}	1.23×10^{-16}	9.83×10^{11}	–	–	50	Analog/RF
U HJ VTFET [126]	5.2×10^{-4}	5.2×10^{-11}	1×10^{7}	–	–	100	Digital circuit
DMCG-CPTFET [130]	6×10^{-5}	1×10^{-17}	6×10^{12}	–	–	50	Analog/RF
V-DMTFET [140]	2.71×10^{-6}	2.71×10^{-14}	1×10^{8}	47	–	42	Biosensor
HGD DE DMG DL TFET [122]	1×10^{-6}	1×10^{-17}	1×10^{11}	–	–	50	Analog/digital circuits
HM-GUL-ED-TFET [131]	8.40×10^{-6}	3.07×10^{-17}	2.73×10^{11}	19.13	–	30	Analog/RF
D GAA CS NT TFET [129]	–	–	–	58.3	175.29	50	Analog/RF
JL-TFET [132]	5.71×10^{-4}	1.32×10^{-10}	4.32×10^{6}	43.6	–	35	Digital circuits
SD-SG TFET [135]	1×10^{-3}	1×10^{-17}	1×10^{14}	–	–	50	Analog/RF
SiGe-S-NW-TFET [121]	1.16×10^{-5}	8.63×10^{-17}	1.35×10^{11}	23.75	–	20	Analog circuit
VS-TFET [127]	–	–	1×10^{4}	17	–	175	Digital circuit
GOSC TFET [120]	3.75×10^{-5}	–	–	61.5	–	40	Digital circuit
JLSGTFET [133]	9.91×10^{-4}	2.80×10^{-13}	2×10^{8}	52.3	2.1	15	Analog/digital circuits

Table 16 Comparison of TFET architectures for analog/RF performance parameters

Device	Transconductance (gm) (mS)	Cut off frequency (f_T) (GHz)	Gain bandwidth product (GBP) (GHz)	Transit time (τ) (ps)
HGD DW TFET [124]	0.29	59.6	9.97	2.67
GDO-HD-GAA-TFET [123]	0.53	38	–	20
DMCG-CPTFET [130]	–	28	–	–
HGD DE DMG DL TFET [122]	0.0052	0.22	0.069	–
HM-GUL-ED-TFET [131]	0.0554	100.6	10.8	–
D GAA CS NT TFET [129]	0.0111	130	–	–
JL-TFET [132]	0.1	100	–	–
SiGe-S-NW-TFET [121]	0.045	950	549	0.9
DE-QG-TFET [128]	0.261	34	3.9	–
JLSGTFET [133]	0.016	–	–	–
GSHJ-PGP-STFET [139]	0.029	4.7	–	–

which enhances high BTBT and low leakage. The HM-GUL-ED-TFET has the best performance features at 30 nm node and boasts electrical doping for ease of manufacture. The JLSGTFET has the least DIBL and good overall performance at 15 nm. In RF analysis, the SiGe-S-NW-TFET exhibits the most superior ac performance with highest f_T and GBP of 950 and 549 GHz respectively and with a low transit time of only 0. 9 ps. The GDO-HD-GAA-TFET shows the highest value for g_m of 0.53 mS. So, a narrow band-gap vertical TFET with junction less properties for sub 20 nm technology is found to be the most promising TFET configuration for future low power analog/RF and some digital applications. Also, a V-DMTFET is found to be good as a biosensor with a low SS of 47 mV/dec at 42 nm feature size.

Glossary

GOSC TFET	Gate on source channel tunnel field effect transistor [120]
SiGe-S-NW-TFET	SiGe source nano wire tunnel field effect transistor [121]
HGD DE DMG DL TFET	Hetero gate dielectric drain engineered dual metal gate tunnel field effect transistor [122]
HGD DW TFET	Hetero gate dielectric dual gate-metal work function tunnel field effect transistor [124]
GDO– HD–GAA-TFET	Gate drain overlapped hetero gate dielectric gate all around tunnel field effect transistor [123]

U HJ VTFET	U-shaped gate hetero junction vertical tunnel field effect transistor [126]
DMCG-CPTFET	Dual metal control gate charge plasma tunnel field effect transistor [130]
V-DMTFET	Vertical dielectric modulated tunnel field effect transistor [140]
HM-GUL-ED-TFET	Hetero material gate underlapped electrically doped tunnel field effect transistor [131]
D GAA CS NT TFET	Dual gate all around core shell nano tube tunnel field effect transistor [129]
JL-TFET	Junction less tunnel field effect transistor [132]
SD-SG TFET	Splitted drain single gate tunnel field effect transistor [135]
VS-TFET	Vertical sandwiched channel tunnel field effect transistor [127]
DE-QG-TFET	Drain engineered quadruple gate tunnel field effect transistor [128]
JLSGTFET	Junction less single gate tunnel field effect transistor [133]
GSHJ-PGP-STFET	Ge source hetero junction partial ground plane base SELBOX (selective buried oxide) tunnel field effect transistor [139]

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Availability of data and material The associated data will be made available on request.

Declarations

Conflict of interest There is no conflict of interest at any level.

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