Optimized design of an all-optical XOR gate with high contrast ratio and ultra-compact dimensions

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Abstract

In this work, an optimized structure for an all-optical XOR gate with high contrast ratio and extremely compact dimension is proposed based on a photonic crystal platform. The above structure employs silicon rods in a hexagonal lattice configuration. The design works purely on linear interference effect between the incoming light signals without utilizing any non-linear materials. To study the propagation of light within the structure and to generate the bandgap diagram, the Finite Difference Time Domain technique and Plane Wave Expansion methods are utilized. After optimization of the various design parameters, a contrast ratio of 31.76 dB is attained by the proposed structure along with a response time of 0.46 ps and a footprint of 42.24 μm^2. The device can be operated in the C Band with optimum performance at 1550 nm, which is the telecommunication wavelength. The operating bit rate for the proposed structure is 2.17 Tbps. The all-optical XOR gate plays a crucial role as the building blocks of various sequential and combinational logic designs suitable for application in optical computing and telecommunication systems.

1 Introduction

Recent advance in technology calls for ultra-high-speed data transmission with low latencies to keep up with the user demands. Optical technology plays a pivotal role in dominating all areas of communication and computing due to its wide bandwidth, high speed, compactness and throughput [1]. Owing to the huge popularity of internet-based communications, the availability of bandwidth and high speed is already overwhelmed and leads to the electronic bottleneck problem. The increasing user demands require advanced technologies with ultra-high speeds and low latencies. The existing technologies cannot keep up with the increasing user demands, hence move towards all-optical communication which can provide high speeds with low latencies [2].

In a complete optical network, the various all-optical devices utilize optical logic gates as the fundamental building blocks [3]. Several combinational and sequential logic circuits for applications, such as switching, multiplexing, parity checking, encoding, filtering and so on, are constructed using logic gates [4, 5]. All these circuits can be implemented using optical logic gates without any electro-optic conversions [6–10]. Several methods have been utilized to implement these gates, such as using non-linear ring resonators [11], Semi-conductor Optical Amplifiers (SOA) [12], non-linear directional couplers [13], Highly Non-Linear Fibers (HNLF) [14], photonic crystals [15], plasmonic slot waveguides [16] and quantum-dot SOA (QD SOA) [17]. However, most of these designs lack chip-level integration capability due to bulky dimensions and flexibility issues [18]. SOA-based designs suffer from gain saturation and make use of high driving current resulting in low-speed operation. Non-linear fibers suffer from bulky design and sensitiveness to environmental factors despite providing better response times. PPLN (Periodically Poled Lithium Niobate)-based devices require accurate temperature control and high input powers for better operation [19]. Currently, photonic crystal platforms are gaining a lot of attention owing to their fascinating features like high integration capability with existing electro-optic as well as optical integrated circuits, flexibility in design, ultra-compact dimensions, wide operating bandwidth, high speed and low power consumption [20–22]. Photonic crystals possess a unique feature called bandgap which enable efficient manipulation of light in the required direction over a wide operating bandwidth [23]. Photonic crystal-based

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logic gates usually operate on the principles of self-collimation, Kerr non-linear effect or linear interference effect. Among these, designs based on non-linear effect require higher operating power and self-collimating effect has limitations in attaining compact dimensions [24]. Interference effect-based all-optical logic gates enable compact and power efficient designs with high compatibility for advanced optical integrated circuits.

The all-optical XOR (AO-XOR) gate or Exclusive OR gate is highly popular as it forms the primary element in the construction of all-optical logic circuits for several applications, such as optical computing, parity checking, all-optical error correction and detection, network coding, pseudorandom number generation, and so on. The AO-XOR gate forms the fundamental component for implementing complex logic circuits for these critical functionalities [25]. Several works on AO-XOR gates based on photonic crystals are already available in the literature.

A design based on a T junction and nano-resonators using two-dimensional (2D) photonic crystals possessed a footprint of 85.22 μm^2 along with a contrast ratio (CR) of 43.33 dB [26]. An AO-XOR was proposed using Y-branch waveguide with a CR of 33 dB and footprint of 160.08 μm^2 [27]. A simple design for AO-XOR gate in silicon on insulator with and operating wavelength of 1550 nm was proposed [28]. An implementation using silicon dielectric with square lattice with a footprint of 45.36 μm^2 attained a CR of 8.29 dB at 1550 nm [29]. A linear structure of footprint 60.2 μm^2 for AO-XOR operation was proposed with a CR of 14.7 dB and low response time [30]. A configurable structure working on interference effect with dimensions of 192 μm^2 was designed to achieve XOR functionality with an extinction ratio (ER) of 23 dB [31]. It can be observed that photonic crystal-based designs working on interference effect having compact dimensions and high CR can be seen as potential candidates for the future optical integrated circuits (OICs). Achieving high CR without the use of any additional phase control elements leads to a compact and energy efficient design.

In this paper, an optimized AO-XOR gate on a photonic crystal platform using silicon material working on interference principle is implemented. The already proposed structure of reconfigurable AO-XOR/NOT gate [32] is taken so as to optimize the various structural parameters to achieve the maximum CR and compact dimensions with low response times. The Finite Difference Time Domain (FDTD) technique-based simulations are utilized to study the light propagation within the structure whereas the bandgap structure is simulated utilizing Plane Wave Expansion (PWE) method. Section 2 describes the mathematical analysis and principle of operation followed by optimized structure of the AO-XOR gate in Sect. 3. Section 4 covers the simulation results and analysis for the optimized design. Section 5 concludes the work followed by references.

2 Mathematical analysis and principle of operation

Photonic crystals are periodic dielectric structures with low loss that can trap light and manipulate their propagation in the desired path using bandgap engineering. The photonic bandgaps (PBG) which arise due to periodic interactions within the crystal are the frequency bands which cannot propagate in the crystal. By properly inserting suitable defects, such as line, point and surface defects within the perfect crystal, light gets localized inside and various logic functionalities can be realized [33]. The macroscopic Maxwell's equations govern the distribution of magnetic and electric fields inside the photonic crystal. The solutions of Maxwell's equations may be treated as the product of a plane wave in periodic function as per the Bloch's theorem [34].

$$E(r) = \varphi(r).\exp(ik.r) \tag{1}$$

Here, φ (r) and k denote the periodic function and Bloch's wave number, respectively. Based on these assumptions, the time-independent relations for the wave equations are,

$$\frac{1}{\epsilon_r}\nabla \times \nabla \times \mathbf{E} = \left(\frac{\omega}{c}\right)^2 \mathbf{E} \tag{2}$$

$$\nabla \times (\frac{1}{\epsilon_r}\nabla \times \mathbf{H}) = \left(\frac{\omega}{c}\right)^2 \mathbf{H} \tag{3}$$

where, H, E, ω and ϵ_r represent the magnetic field, electric field, frequency and macroscopic dielectric function, respectively. These equations can be solved to determine the propagation modes within the proposed photonic crystal structure. The solution at one scale can be used to determine the solution at any other scale since the photonic crystals are scale invariant.

The beam interference effect can be utilized to determine the logic state of the gate output. The interference may be destructive or constructive depending on the phase of the arriving signals which can be controlled by changing the path length of waveguides. Constructive interference phenomena arise if the input waves have a phase difference which is an even multiple of π. This generates a higher optical intensity or a logic high output state. Destructive interference arises when the difference in phase becomes an odd multiple of π resulting in cancelation of signals leading to low output power or logic low state [35]. The proposed AO-XOR design consists of waveguides of different path lengths leading to phase difference between the input signals
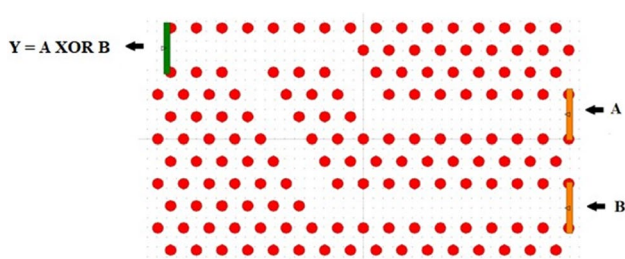
Fig. 1 Proposed structure of AO-XOR gate

Table 1 Truth table of XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

resulting in XOR operation without using any additional phase control mechanisms.

3 Design of modified AO-XOR gate

This work aims to boost the performance of the already designed AO-XOR gate [32] by proper optimization of the structural parameters. The lattice type, lattice constant, lattice dimensions and radius of rods are modified such that the CR is enhanced and the footprint of structure is decreased. The new optimized structure for the AO-XOR gate is illustrated in Fig. 1. Table 1 depicts the truth table for XOR gate. There is one output port (Y) and two input ports (A, B). The proposed AO-XOR gate is implemented on a Silicon-on-Insulator (SOI) photonic crystal platform that consists of a hexagonal lattice of Si rods embedded in air. It consists of 17×11 silicon rods having refractive index of 3.47. Each rod has a radius (r) of 0.21a and the

lattice constant (a) value is chosen as 523 nm. Hexagonal lattice is chosen as it tends to provide larger bandgaps as compared to square lattice.

The photonic bandgap diagram for the proposed structure is given in Fig. 2. The design parameters, such as lattice constant (a), radius of dielectric rods (r) and refractive index (n), determine the range of frequencies that fall in the PBG. The desired operating wavelength should fall within the PBG for the working of the all-optical logic gate. There are two large bandgaps existing in TE mode as inferred from the diagram. These correspond to the values 1622.5–1062.9 nm in the first band and from 809.7 to 633.9 nm in the second band. It can be seen that the required operating wavelength of 1550 nm, also called the telecommunication wavelength falls in the first gap.

The two input ports have considerable isolation between them so as to prevent intermixing of signals. Some amount of signal leakage is unavoidable when using such a geometry; however, the leakage should be kept as low as possible to avoid loss of signal power leading to inaccurate results and low CR values. At the same time, providing a larger gap between the adjacent waveguides could reduce signal loss but it tends to increase the device dimensions. Considering these trade-offs, the optimum gap between the adjacent waveguides is chosen as 2a for the proposed design.

The horizontal interaction length for the top input waveguide is 8a and that for the bottom waveguide is 10a. The vertical interaction length toward output waveguide is 4a for the top input waveguide and 8a for the bottom waveguide. As it can be seen, the distance covered by the optical wave to travel toward output port Y from input A is shorter compared to the distance between port Y and port B. Hence, when both the input ports have optical signals, these traverse different path lengths giving rise to a difference in phase that is an odd multiple of π, thus canceling them out. When only one input port has an optical signal, there is no interaction occurring and the same signal arrives at the output. The detailed design parameters are tabulated in Table 2. All these parameters are chosen after proper optimization as given in the next section.
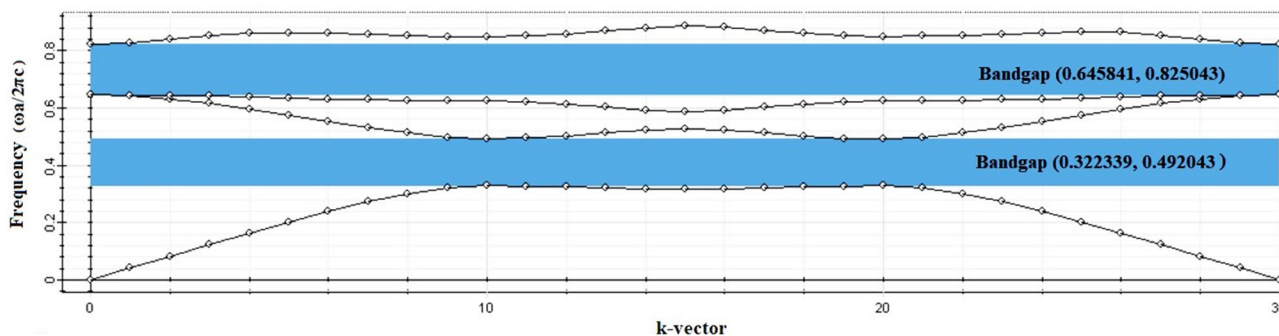

Fig. 2 Photonic bandgap structure for 17×11 Si rods in air

Table 2 Design parameters for modified AO-XOR gate

Lattice Type	Hexagonal
Lattice dimensions	17×11
Lattice constant (*a*)	523 nm
Dielectric material	Silicon (Si)
Refractive index of dielectric	3.47
Input power	1 mW
Wavelength	1550 nm
Radius of rods (r)	$0.21 \times a = 109.83$ nm
Footprint	42.24 μm^2

The above structure has several advantages as it is composed only of silicon material. The absence of non-linear materials leads to a less complex design with lower power consumption and the silicon-based structure increases the compatibility with existing CMOS logic system as well as with the hybrid electro-optic and future all-optical integrated circuits. The use of hexagonal lattice provides larger bandgaps and a wider bandwidth of operation. No additional control signals are used to achieve the XOR functionality. The design has ultra-compact dimensions which increase the flexibility and integration capability with other AO devices.

4 Simulation results and analysis

Simulation of the structure is performed by 2D FDTD technique utilizing Synopsys RSoft CAD software to analyze the propagation of light within the device and its various performance characteristics. The open-source software by Optiwave Systems called Opti-FDTD is utilized to generate the bandgap diagram using PWE method. To compute the optical power distribution, the absorbing boundary condition of Perfectly Matched Layers (PML) is applied. To obtain more accurate results to include dispersion effects eventually, the Lorentzian dispersion model was used along with the FDTD analysis using the above software. To check the working of the proposed gate, a Gaussian optical source generating a continuous light signal of wavelength 1550 nm is kept at each of the input ports. To measure the optical intensity arriving at the output, a line monitor is kept at output port Y. The input power P_{IN} at ports A and B is fixed

at 1 mW/μm^2. The spatial grid has to be small to generate a complete simulation. This is indicated by the wavelength of the material used. For stable operation, the space time grids should follow the given condition [36],

$$c\Delta t < \frac{1}{\sqrt{\frac{1}{\Delta x^2} + \frac{1}{\Delta z^2}}} \tag{4}$$

where, Δt denotes the step time, c denotes the free space velocity of light, and Δx, Δz represents the space steps along *x*- and *z*- axis, respectively.

Table 3 shows the digital as well as optical truth table for the optimized AO-XOR gate. Here, the measured output power is expressed as a fraction of the input power P_{IN}. To distinguish between logic 1 and logic 0 levels, the optical intensity levels of each state must be specified. In this work, power level below 0.005 P_{IN} denotes logic 0 state and power level above 0.1 P_{IN} denotes logic 1 state. The various performance metrics are computed to characterize the performance of the optimized design. The contrast ratio is a mathematical expression consisting of the output power levels for the two logic states [37]. i.e.,

$$CR\ (dB) = 10 \log_{10} \left(P_h / P_l \right) \tag{5}$$

where, P_h and P_l denote the lowest value of optical intensity in logic high state and the highest value of optical intensity in logic low state, respectively. The higher the value of CR, the easier it is to distinguish between the logic states and hence better the operation.

Another parameter that significantly affects the performance of the AO logic gate in an integrated circuit is return loss. It is calculated as the difference between the forward and reflected powers in dB. It is a measurement of the amount of light injected from the source compared to the amount of light reflected back toward the source and a high return loss value is preferred for better operation [38].

$$RL\ (dB) = 10 \log \left(P_{IN} / P_{REF} \right) \tag{6}$$

Using the above equation, Return Loss (dB) is calculated wherein P_{IN} denotes the input power and P_{REF} denotes the amount of light reflected back to the input port (s). Another parameter that determines the speed of the device is the bit rate [39]. The approximate operating bit rate of the device is

Table 3 Digital and optical truth table for optimized AO-XOR gate

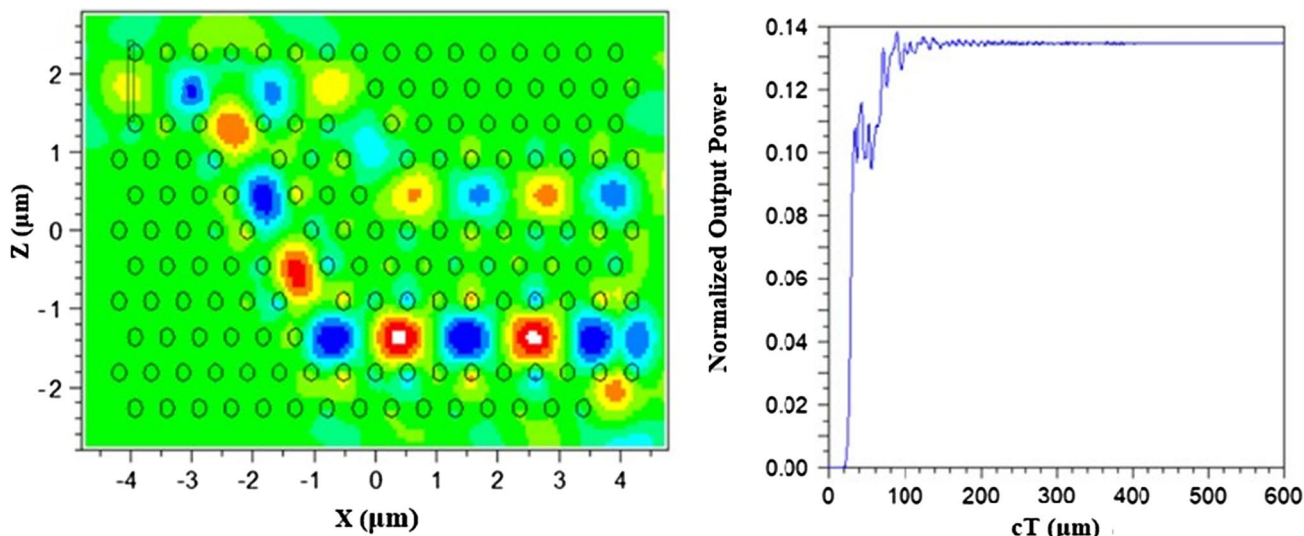| Input A		Input B		Output Y	
Logic state	Power level	Logic state	Power level	Logic state	Power level
0	0	0	0	0	0 P_{IN}
0	0	1	P_{IN}	1	0.139 P_{IN}
1	P_{IN}	0	0	1	0.135 P_{IN}
1	P_{IN}	1	P_{IN}	0	0.00009 P_{IN}

Fig. 3 **a** Optical field intensity. **b** Normalized output power for (A, B) = 01
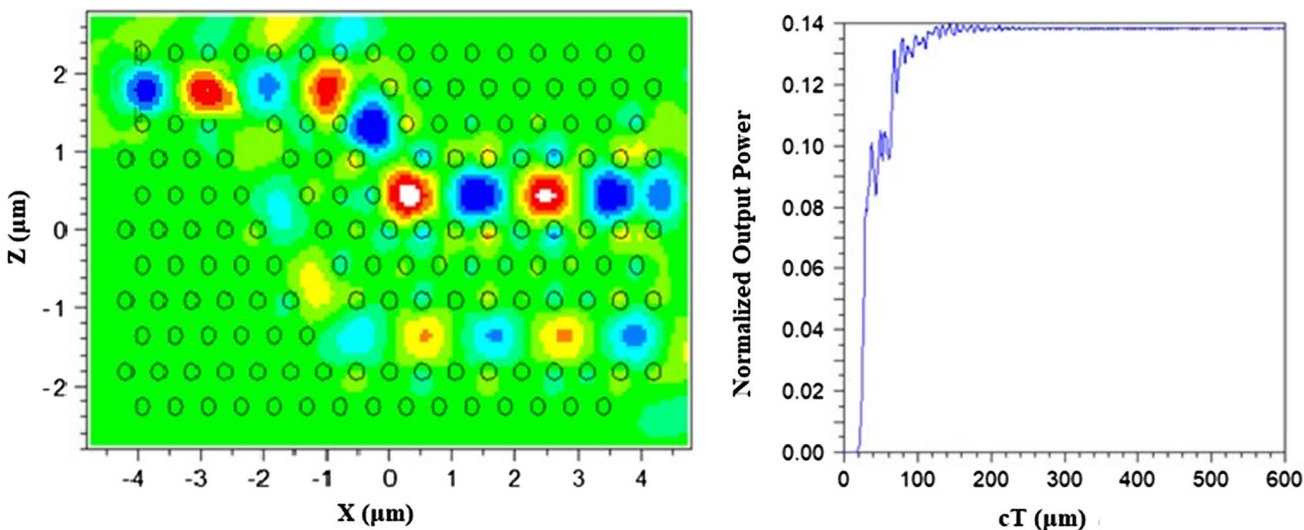

Fig. 4 **a** Optical field intensity. **b** Normalized output power for (A, B) = 10

given by the inverted value of response time. In addition, the dimensions of the device or the footprint are also of prime importance due to the need to integrate a large number of such devices onto a single chip. Lower response times and smaller dimensions are preferred for high-speed operation and easy integration with OICs.

The proposed structure has four different operating states owing to two different inputs. Depending on the interactions between the incoming light signals, the output port produces either a high-intensity signal or a low-intensity signal. In the first case, the two input ports have zero intensity or logic 0 state, i.e., A = B = 0. Then, no light propagates through the structure giving rise to zero intensity output or logic 0 state

Table 4 Normalized power and CR (dB) for different values of wavelength (nm)

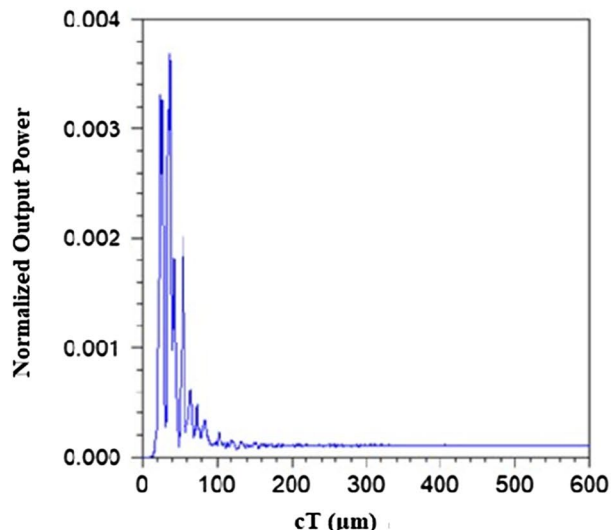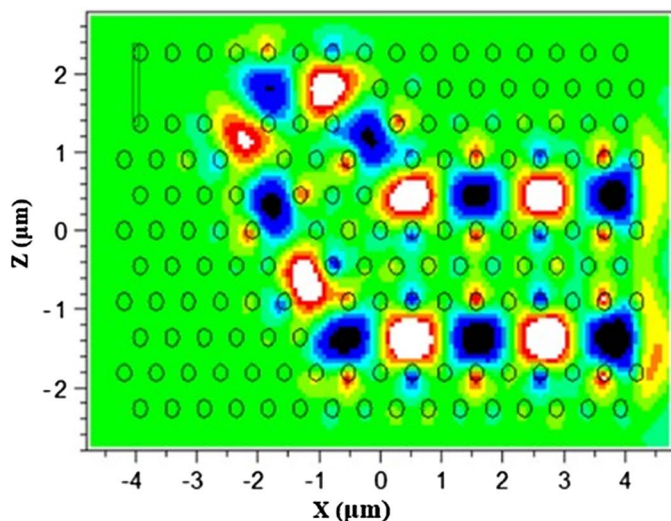| Wavelength (nm)	Normalized power P_O/P_{IN}				CR (dB)
	00	01	10	11	
1530	0	0.11	0.09	0.0015	17.78
1535	0	0.125	0.122	0.0019	18.08
1540	0	0.125	0.112	0.0025	16.5
1545	0	0.132	0.133	0.0008	22.17
1550	0	0.139	0.135	0.00009	31.76
1555	0	0.133	0.12	0.0004	24.77
1560	0	0.129	0.115	0.0009	21.06
1565	0	0.098	0.10	0.0011	19.49

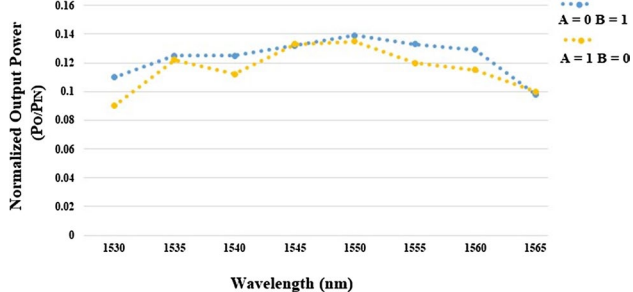**Fig. 5** **a** Optical field intensity. **b** Normalized output power for (A, B) = 11

Fig. 6 Plot of normalized output power versus input wavelength (nm) for A, B = (10), (01)
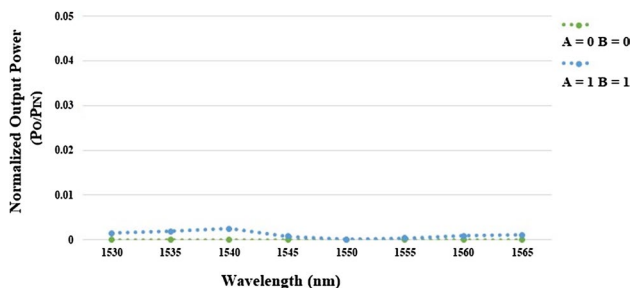

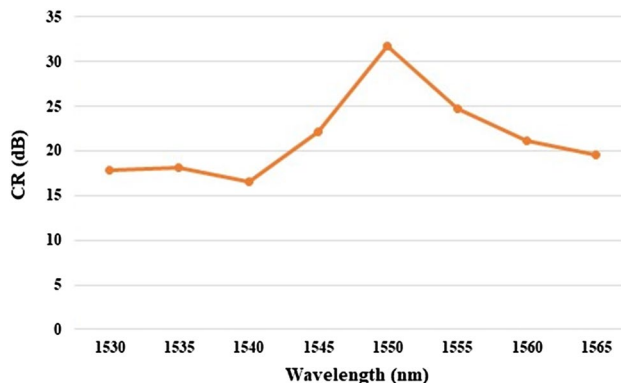**Fig. 7** Plot of normalized output power versus input wavelength (nm) for A, B = (00), (11)

Fig. 8 Variation of CR (dB) versus operating wavelength (nm)

at port Y. For the second case, the first input port has zero intensity and the second port has an input light signal of P_{IN} power i.e., A = 0, B = 1. Then, only one optical wave enters the structure and it propagates along the input waveguide toward the output Y giving rise to a logic 1 output. This is depicted in Fig. 3.

Table 5 CR (dB), response time (ps) and bit rate (Tbps) for different values of Si rod radius

Radius of Si rods (nm)	CR (dB)	Response time (ps)	Bit rate (Tbps)
$0.18 \times a$	6.75	0.89	1.12
$0.19 \times a$	8.94	0.68	1.47
$0.20 \times a$	16.02	0.65	1.54
$0.21 \times a$	31.76	0.46	2.17
$0.22 \times a$	17.69	0.52	1.92

Table 6 CR (dB), response time (ps) and bit rate (Tbps) for different values of lattice constant, a (nm)) with ± 5 nm variation

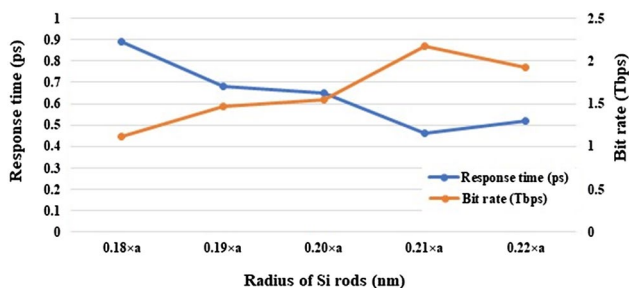| Lattice Constant (nm)	CR (dB)	Response time (ps)	Bit rate (Tbps)
520	25.18	0.68	1.47
521	25.7	0.5	2
522	25.3	0.49	2.04
523	31.76	0.46	2.17
524	24.35	0.6	1.66

Fig. 9 Variation of response time (ps) and bit rate (Tbps) versus radius of Si rods (nm)
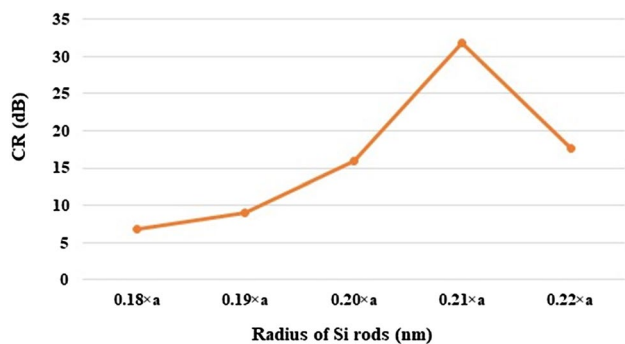

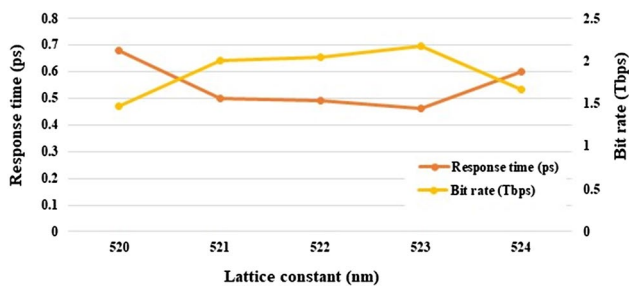**Fig. 10** Variation of CR (dB) versus radius of Si rods (nm)

Fig. 11 Variation of response time (ps) and bit rate (Tbps) lattice constant (nm)

For the third case, the first input port has a light signal, while the second port has zero intensity, i.e., A = 1, B = 0.

Table 7 CR (dB), response time (ps) and bit rate (Tbps) for different values of lattice constant, a (nm) with ± 5 nm variation

Lattice Constant (nm)	CR (dB)	Response time (ps)	Bit rate (Tbps)
513	21.58	0.72	1.39
518	24.57	0.69	1.44
523	31.76	0.46	2.17
528	24.01	0.68	1.47
533	22.55	0.71	1.41

Table 8 Return loss for various input combinations for AO-XOR gate

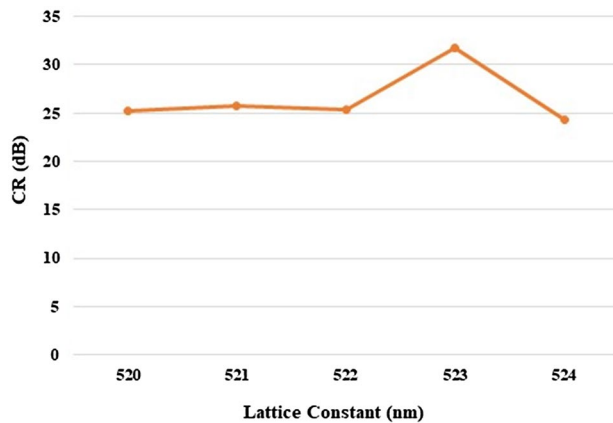| Input logic state	Return loss (dB)	
	Port A	Port B
Case 1: 00	–	–
Case 2: 01	–	3.5
Case 3: 10	4.9	–
Case 4: 11	3.6	4.08

Fig. 12 Variation of CR (dB) versus lattice constant (nm)

Then, only one signal travels through the structure without any interactions giving rise to logic high result. This is illustrated in Fig. 4. For the fourth case, two high-intensity waves propagate along the structure, i.e., A = B = 1. In this case, the two signals travel different path lengths and undergo a change in phase giving rise to a destructive interference effect. The signals get canceled out and very low intensity corresponding to logic 0 state reaches Y. This is depicted in Fig. 5.

For varying values of wavelengths from 1530 to 1565 nm, the normalized output powers for the four different input states are studied. This is tabulated in Table 4. For A, B = 10 and 01 cases, the output port Y has high-intensity light corresponding to logic 1 output. For A, B = 00 and 11, very low intensity or no light appears at port Y resulting in logic 0 state. Overall, the best performance is attained for 1550 nm wavelength as seen from Fig. 6 and 7. For all other values of wavelength, a lower value of CR was obtained with the least values attained for 1530 nm and 1540 nm. The plot of CR versus input wavelength is depicted in Fig. 8. A high CR value of 31.76 dB is attained by the device at 1550 nm.

The various structural parameters were chosen carefully after optimizing the design for achieving maximum CR with low response times. These metrics are directly affected by

Table 9 Performance comparison of the proposed work with existing works

Paper	Principle & technique	Contrast ratio (dB)	Response time (ps)	Footprint (µm²)	Operating wavelength (nm)	Bit rate (Tbps)
The proposed work	Interference effect & Hexagonal lattice 2D photonic crystals	31.76	0.46	42.24	1550	2.17
Anagha et al. [32]	Interference effect & Square lattice 2D photonic crystals	7.16	0.4	93.5	1550	2.5
Kordi et al. [30]	Interference effect & Square lattice 2D photonic crystals	15	0.14	60.2	1533–1556	**
Rao et al. [29]	Interference effect & Square lattice 2D photonic crystals	8.29	**	45.36	1550	**
Mohebzadeh-Bahabady et al. [26]	Interference effect & Hexagonal lattice 2D photonic crystals	19.25	0.466	252	1550	2.145
Preeti Rani et al. [40]	Interference effect & Hexagonal lattice 2D Photonic crystals	8.49	1.024	**	1550	0.976

**Not discussed

changes in radius of rods, operating wavelength, lattice constant and the material refractive index. The silicon rod radius is varied from 0.18a to 0.22a as shown in Table 5. The variation of response time and bit rate with Si rod radius is plotted in Fig. 9 and that of CR with Si rod radius in Fig. 10. The maximum CR value and the least response time is achieved for the radius value of 0.21a. Table 6 depicts the variation in lattice constant from 520 to 524 nm. The plot of response time and bit rate versus lattice constant is illustrated by Fig. 11. The highest bit rate of 2.17 Tbps and maximum CR is attained for lattice constant of 523 nm as seen from Fig. 12.

From a fabrication point of view, we have considered $a \pm 5$ nm variation of lattice constant for further analysis. These results are shown in Table 7. Again, it can be observed that the maximum value of CR (31.76 dB) and highest bit rate (2.17 Tbps) was attained for the lattice constant value of 523 nm. With varying values of lattice constant (± 5 nm), the CR and bit rate remained above 21 dB 1.3 Tbps, respectively. Even with such large variations, the proposed structure showed reasonably good performance especially in terms of the CR which is of utmost significance with regards to logic gates.

Table 8 shows the calculated values of return loss at each of the input ports A and B for the various logic states of the proposed AO-XOR gate. It can be inferred that a significant amount of back reflection occurs which has to be taken into consideration in future works to lower the loss of power especially when coupling with other devices in an OIC. However, in spite of this backscattering, a high CR is achieved owing to larger gap in power levels for logic 1 and logic 0 states. This is highly significant in distinguishing between the two logic states especially when working with low power levels.

From the above plots, operational characteristics of the newly designed AO-XOR structure is optimized to attain the maximum CR, the highest bit rate and the least response time. Thus, the final structure has the optimized design parameters of lattice constant 523 nm, radius $0.21 \times a$ and input wavelength 1550 nm.

The newly proposed design for AO-XOR gate has improved the already existing design and optimized the various structural parameters to attain a high CR of 31.76 dB without using any non-linear material or additional phase control elements along with a footprint of extremely low dimensions. The device is realized on wafer dimensions of 42.2 µm². A response time of 0.46 ps and a bit rate of 2.17 Tbps is attained by the structure. The entire device is composed of only silicon material which enables easy integration with hybrid electro-optic as well as with the upcoming OICs. Table 9 shows a comparison of the performance of the improved AO-XOR gate with existing works from the literature. It can be observed that achieving a CR above 30 dB for a structure based only on linear interference effect with extremely low dimensions and low response time (< 1 ps) can be considered as a huge step toward the practical realization of a complete optical network based on integrated all-optical devices.

5 Conclusion

In this work, an optimized design of AO-XOR gate based on beam interference effect in 2D photonic crystals is proposed. The design is achieved after proper optimization of the structure parameters to attain a maximum contrast ratio of 31.76 dB. The structure possesses very low dimensions of 42.2 µm² with an operating speed of 2.17 Tbps. The light

wave propagation within the structure is studied with the help of 2D FDTD technique. This work proves to be a potential candidate to build various combinational and sequential all-optical logic circuits for applications in the areas of optical computing and telecommunications.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

Ethics declarations This article does not contain any studies involving animals or human participants performed by any of the authors.

Consent to participate Not applicable.

Consent for publication Not applicable.

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