Applied Physics B (2019) 125:89
https://doi.org/10.1007/s00340-019-7202-3

Applied Physics B
Lasers and Optics

Guiding and controlling light at nanoscale in field effect transistor

Lalit Singh[1] · Surbhi Tidke[1] · Mukesh Kumar[1]

Received: 9 March 2019 / Accepted: 25 April 2019 / Published online: 4 May 2019
© Springer-Verlag GmbH Germany, part of Springer Nature 2019

Abstract
Metal–oxide–semiconductor field-effect transistor (MOSFET) and tunnel field-effect transistor (TFET) are proposed to guide and control the light at nanoscale utilizing the hybridization of plasmonic and optical modes. The hybrid plasmonic (HP) mode is confined in the dielectric sandwiched between the metal gate and semiconductor channel, which results from the coupling of surface plasmonic polariton mode at the metal–dielectric interface with the optical mode in the dielectric. Conventional conductivity modulations in the channel through gate and drain–source voltages are utilized to control the guided light. A long propagation length of 74 μm and a very small mode area of $\lambda^2/96$ are reported for field-effect transistor at an operating wavelength of 1550 nm which are useful to realize low loss and compact optoelectronic devices. The charge-carrier dynamics along with the plasma dispersion effect in the silicon channel, through voltages applied on the gate and source–drain, result in the optical phase modulation in MOSFET and TFET. Phase shift of π radian at a length of 1.2 mm and 0.21 mm is obtained in MOSFET and TFET, respectively. The proposed concept has the potential to enable multifunctionality of the mature field effect transistors.

1 Introduction

The rising silicon photonics holds a strong promise to revolutionize short-reach optical interconnects [1–3]. Wide deployment of broadband optical communications has become crucial especially for Internet data centers and high-performance computing systems [4, 5]. Integration of silicon-based complementary metal–oxide–semiconductor (CMOS) field-effect transistor (FET) and silicon integrated photonics, also known as silicon CMOS-integrated photonics, carries the potential to play a key role in enabling such deployment [6, 7]. The limitations of using copper in interconnects in electronic ICs have heralded the emergence of optical interconnects [8, 9]. The strong presence of silicon in electronic ICs favors the use of silicon to realize integrated photonic devices. During the last couple of decades, integrated silicon photonic devices have seen notable advances [10–15]. The realization of photonic devices at nanoscale for large-scale photonic integration remains a hot topic on which lot of research efforts are being made. Several mechanisms are proposed to reduce the photonic device size beyond the diffraction limit [15–17]. Sub-wavelength optics based on surface plasmon polaritons (SPP) allows controlling and guiding of light at nanoscale structures, mainly at the metal–dielectric interfaces [18, 19]. Because of the opposite polarities of permittivity of the two materials, i.e., noble metals (gold) and dielectric (silicon-oxide), the optical field can be squeezed into much smaller dimensions than the diffraction limitation of the light. High optical losses associated with SPP-based waveguides can be reduced with hybrid plasmonic (HP) by exploiting optical confinement deeper into the dielectric and away from the metal–dielectric interface [20–23]. HP waveguide can support HP mode to propagate longer with low loss and very small mode area, in the order of $\lambda^2/400$; hence, it can be a building block to realize photonics at nanoscale. A number of on-chip optical functions have been realized to guide the light in different materials and then to control the light for different applications, e.g., optical modulation. Guiding the light in silicon at nanoscale and then controlling it electrically are two fundamental requirements for the realization of

✉ Lalit Singh
phd1601102002@iiti.ac.in

Surbhi Tidke
surbhitidke@gmail.com

Mukesh Kumar
mukesh.kr@iiti.ac.in

[1] Optoelectronic Nanodevice Research Laboratory, Department of Electrical Engineering, IIT Indore, Indore 453552, India

compact silicon photonic platform, e.g., for silicon CMOS-integrated photonics [6, 7].

The MOSFET configuration has an advantage, over PIN diode with isolation trenches, of negligible dc power consumption along with localization of refractive index change under the gate electrode [24]. Metal–oxide–semiconductor-based silicon modulator based on free carrier effect offers bandwidth exceeding 1GHz with a V_π L product of 8 V cm [25]. The speed of silicon photonic modulators also depends on the free charge carrier concentration and the contact pad placements. The device speed can be increased by introducing a graded doping profile in the vertical direction in a way such that higher doping density exists near the gate oxide and lower doping concentrations in the rest of the waveguide [25]. Nanoscale photonic functionality using MOS-based structures is still missing; it can be exciting to use MOSFETs underlying electronic ICs as nanoscale optical waveguides with an electronic control for the realization of various photonic devices.

Here, we report nanoscale optical guidance and controlling of a MOSFET and in a tunnel TFET with mode field area of $\approx \lambda^2/100$. The 1550-nm wavelength light is made to confine in the gate oxide of few nanometer thickness sandwiched between the gate metal and the underlying silicon. The concept of hybrid plasmonic waveguide is used to guide the hybrid plasmonic mode in a 2–3 nm dielectric. The guided HP mode shows a propagation length of 72 µm for TFET and 48 µm for MOSFET. The mode areas are reported to be $\lambda^2/46$ and $\lambda^2/96$, respectively, for MOSFET and tunnel FET. The very electronic nature of FET is utilized to control the guided light at nanoscale. The design and analysis of the devices are performed with finite difference eigenmode (FDE) using LUMERICAL [26]. Conductivity modulations in FETs using applied voltages are shown to control the phase of the guided HP mode. An efficient optical phase modulation is reported in both the devices. On varying drain–source voltage phase shifts of radian at a length of 204 µm and 1235 µm are obtained for TFET and MOSFET, respectively. On varying gate voltage, the change in effective refractive index is in the order of 10^{-5}, which is smaller than that for a change in drain voltage resulting in 10^{-3} change in the effective refractive index. The proposed concept adds an extra degree of freedom in the application of FETs. The reported results are excellent examples for enabling multifunctionality in FETs.

2 Device description

The schematic of the proposed devices is shown in Fig. 1. A nanoscale optical waveguide as well as phase modulator is functional through the gate-oxide of Fig. 1a n-channel MOSFET and Fig. 1b n-channel tunnel FET. The hybrid plasmonic mode is guided in the gate oxide on the semiconductor channel as shown in 3D view of the proposed device. The inset of Fig. 1a shows the optical field confinement contour map. The charge carrier dynamics of the channel in both the cases is made to control the guided HP mode utilizing the conductivity modulations by varying the terminal voltages. The HP mode confined in the gate oxide is the result of the coupling of SPP with the optical mode (leaky) in the underlying semiconductor (channel). The hybridization of leaky optical mode from the high index layer silicon is coupled with SPP from the interface of the dielectric and metal. The square norm of the mode amplitude of the hybrid mode is a crucial parameter which is defined as $|b|^2 = \frac{n_{hyb}-n_d}{2n_{hyb}-n_d-n_{spp}}$, where nhyb, nd and nspp are the real refractive index of the hybrid, dielectric (optical) and plasmonic mode. The mode character study on a similar design is done in [20, 22]; if the mode character is greater than 0.5, the hybrid mode is more inclined toward a leaky optical field; and if it is less, then the

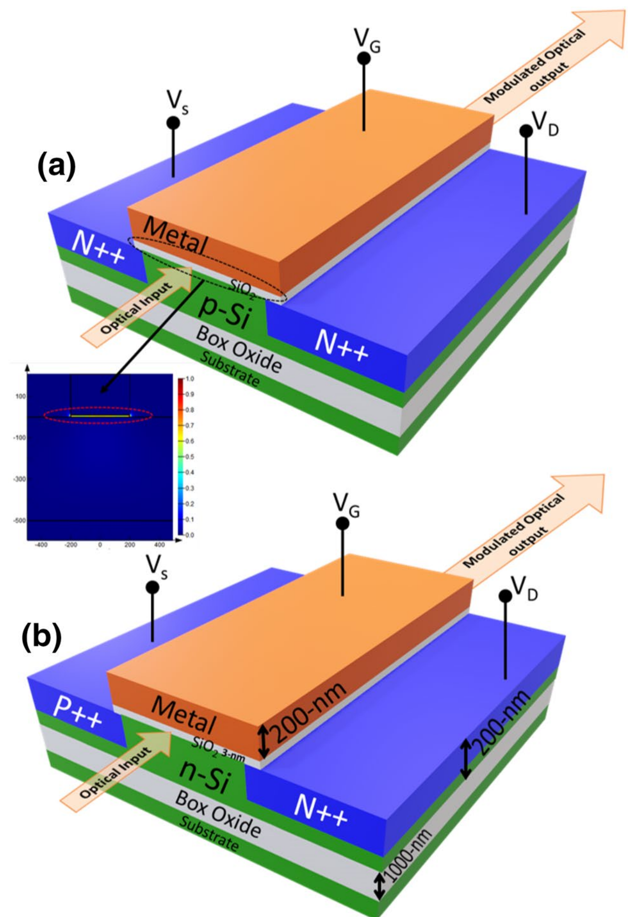

Fig. 1 Schematic of nanophotonic waveguide cum phase modulator based on hybrid plasmonic concept using **a** MOSFET (inset shows the optical field confinement in gate oxide) and **b** tunnel FET, both on silicon-on-insulator with a 120-nm channel length

field is more plasmonic mode. The coupled (HP) mode supports long propagation while maintaining a mode area small enough to cause nanoscale confinement. The electric field associated with the excited plasmonic wave decays exponentially along both the sides of the interface. Gold is used as the top gate metal for the proposed device, with relative permittivity of = − 115.13 + i 11.259 [27]. The field enhancement exists at the top and bottom surfaces of the low index SiO_2 layer. The bottom surface, i.e., Si–SiO_2 interface, has field enhancement due to a strong discontinuity of the normal component of the electric field. This phenomenon takes places only when the thickness of the SiO_2 becomes less than the penetration depth of the evanescent wave resulting into the overlapping of the optical mode and the surface plasmonic mode on each other. The coupling of two modes has potential to propagate at a longer distance of several tens of microns, realizing a promising platform for ultradense photonic integration. Two major factors contributing to the performance of conventional MOSFET for optical behavior are: (1) carrier-induced channel formation and (2) voltage-controlled displacement of channel charge carriers from source to drain. In TFET, source and drain are of opposite doping types and the substrate has a doping type similar to that of the drain influencing injection and depletion of carrier charge concentration on the applied voltage. The light matter interaction due to the graded doping profile and the charge carrier concentration density help in electro-optic phase modulation [21].

The dimensions of high index layer silicon are chosen such that only leaky optical mode can travel through it. The lateral and vertical dimension of the high index layer is taken from [24]. The insulator thickness affects the properties of the waveguide mode. The optimized designs of both the devices exhibit electronic characteristics in line with conventional FETs. The silicon layer thickness is 200 nm (optimized to achieve hybrid mode confined in SiO_2). Figure 2a, b shows the transfer and output characteristics of the MOSFET transistors, respectively, formed on p-type Si. Figure 2c, d shows the input and output characteristics of the TFET transistor. The analysis for MOSFET and TFET includes trap-assisted (SRH) and band-to-band tunneling models, respectively. All the characteristics are in compliance with the basic requirements of a transistor.

3 Optoelectronic characteristics

The drift-diffusion transport solver of Lumerical DEVICE software is used to analyze the electrical characteristics of the proposed device by defining the component geometry and Gaussian doping profile [26]. Simulation of the charge distribution in response to an applied voltage is performed. Lumbricals optical solver, MODE solutions, is used to

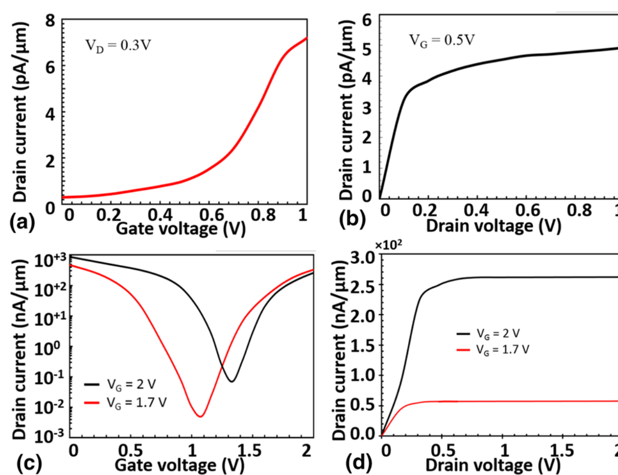

Fig. 2 Simulated characteristics of n-type MOSFET. **a** Transfer characteristics for a fixed drain of 0.3 voltage. **b** Output characteristics for a fixed gate voltage. Simulated characteristics of nTFET. **c** $I_D V_G$ characteristics for different drain voltages. **d** $I_D V_D$ characteristics for a drain voltage of 2 V and 1.7 V

perform FDE simulations of the guided-wave structures and extract the phase response as a function of the applied voltage with respect to change in effective refractive index. A fixed source wavelength of 1500 nm is used for simulation. The refractive index used at 1550 nm of wavelength for SiO_2 and Si is 1.44 and 3.48, respectively, and the dielectric constant for gate metal gold is = − 115.13 + i 11.259 [27]. PML is designed to absorb the outgoing waves from the active computation domain without reflecting them back to the active region of the device. The perfectly matched layer boundaries and metal boundaries are located at more than three times the dimensions of the device being simulated along the x-axis and z-axis. The electrical characteristics for the phase modulation are analyzed using the drift-diffusion transport method by studying the distribution of the charge component in response to an applied voltage. The modulation occurs in a transverse device where the current flow is perpendicular to the direction of light propagation. MOSFET utilizes a single injection carrier (hole or electron) altering the refractive index. Equation (1), (2) shows the change in refractive index because of the changes in electron–hole densities [28].

$$\Delta n_e = -\ 8.8 \times 10^{-22}\ \Delta N_e, \quad (1)$$

$$\Delta n_h = -\ 8.5 \times 10^{-18}\ (\Delta N_h\ )^{0.8}, \quad (2)$$

where ΔN_e and ΔN_h represent the electron and hole charge densities, respectively. The equations reveal that the effective refractive index change due to holes is three times larger than that of electrons for the same carrier concentration. In n-type MOSFET, applying positive voltage at the gate terminal tends to repel holes near the oxide that are pushed

downward, leaving behind negative ions. This forms uniform channel thickness and length called the inversion layer. The impact of charge density on effective refractive index was observed at a fixed positive gate voltage, and on applying negative voltage to the drain, the potential difference of the gate-to-drain region becomes less positive compared to the potential difference to that of the gate-to-source region as shown in Fig. 3a. The presence of less positivity of the voltage among the two potential difference regions above the channel results in lesser number of holes being repelled. As a result, more holes are present in a region that is less positive. As drain to gate voltage becomes more positive the greater number of holes get repelled which results in larger change in n_{eff} as shown in Fig. 3b. On applying negative to positive voltage at the drain terminal, the thickness of the depletion region starts increasing, pushing a greater number of holes from the gate-to-drain region, resulting in linear increase in effective refractive index because of the push–pull effect of drain voltage. Figure 3c further shows the inversion layer with stationary immobile ions. Current flows when the channel starts forming. When $V_G > V_{TH}$, injection of carriers into the channel takes place. The propagation length is defined as the distance for the SPP intensity to decay by a factor of 1/e. This condition is satisfied at a length for the guided HP mode given by L_{prop} (μm) $= \lambda/4\pi(n_{eff(imag)})$ [28]. The device modulation speed is dependent on many factors. The speed of the optical phase modulation of the proposed device is limited by the charge carrier injection in the channel and the transistor internal high-frequency capacitance. Further, the increases in doping concentration in drain/source region affect the modulation speed of the device. The choice and the placement of physical contact pads also play a role in lowering the speed of the phase modulation of the device. Figure 4 shows a slope of 0.01 for propagation length at $V_G = 1$ V because of the injected carriers. When $V_G = 0$ V, there is no formation of channel as well as no carrier injection with zero slope. The propagation length for fixed gate voltage, varying drain voltage is L_p ($V_G = 0$ V) = 47.74 μm at $V_D = -3$ V and L_p ($V_G = 1$ V) = 47.70 μm at drain voltage of − 3 V. Figure 4 shows a slope of 0.01 for propagation length at $V_G = 1$ V because of the injected carriers. When $V_G = 0$ V, there is no formation of channel as well as no carrier injection with zero slope. The propagation length for fixed gate voltage, varying drain voltage is L_p ($V_G = 0$ V) = 47.74 μm at $V_D = -3$ V and L_p ($V_G = 1$ V) = 47.70 μm at $V_D = -3$ V. The n-channel tunnel FET device structure has resemblance to a MOSFET forming the inversion or accumulation layer on applying gate voltage, and the substrate region works similar to the PIN diode [29].

The p+ doped region is named as source and the n+ doped region is name as drain. The substrate is lightly n-doped as the intrinsic region. The drain voltage is the onset of tunneling barrier saturation obtained at constant gate voltage. Optically in NTFET, forward bias affects change in the refractive index compared to the reverse bias. Figure 3d shows the injection of holes and electrons into the intrinsic region. The major contribution of the optical losses comes from the absorption of charge carriers and/or from the plasmonic ohmic losses. The larger the charge carriers, the larger will be the optical absorption. The other

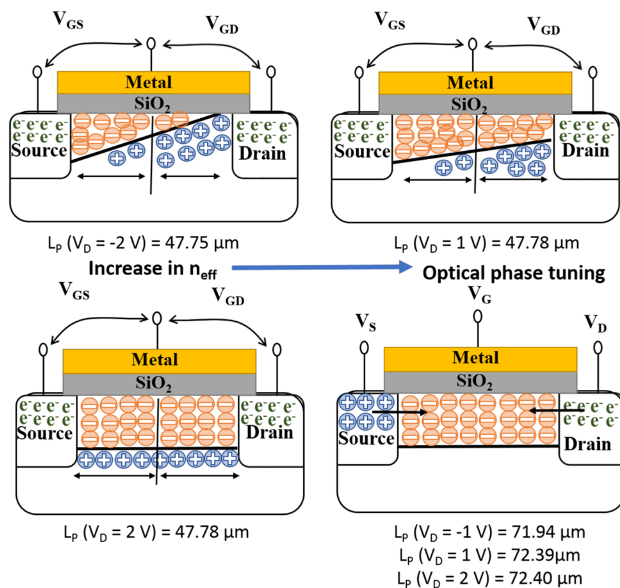

Fig. 3 Opto-electronic n-type MOSFET mechanism at $V_G = 1$ V and $V_S = 0$ V, showing **a**, **b** increase in effective refractive index resulting in optical phase tuning, **c** formation of inversion layer resulting in negligible change in effective refractive index. **d** N-TFET carrier injection from source as well as from drain into the intrinsic region. The light propagation length with respect to applied drain voltages is mentioned below the respective mechanism

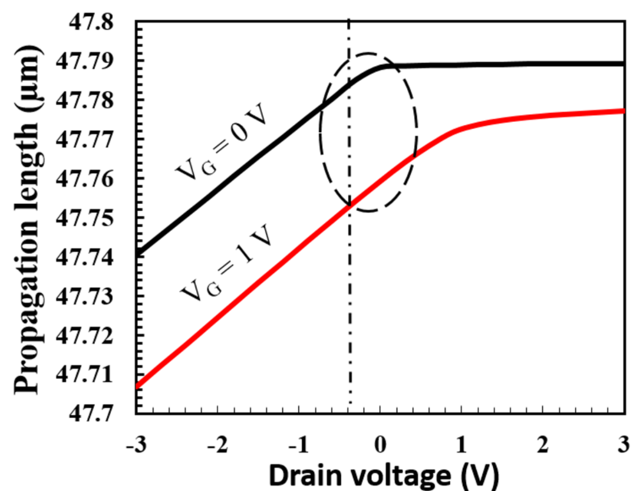

Fig. 4 Effect on propagation length of hybrid plasmonic mode by varying drain voltage at a fixed gate voltage for a conventional proposed MOSFET

sources of optical losses may be related to the in and out coupling of the device. In the proposed device, the optical field intensity is mainly concentrated in the gate oxide layer of 3 nm where the major losses are incorporated due to the plasmonic ohmic losses. The effect of change in drain voltage on the imaginary part of effective refractive index is shown in Fig. 5 (dotted line). The change in the refractive index results in a phase shift $\Delta\phi$ in the hybrid plasmonic mode given by:

$$\Delta\phi = \frac{2\pi L}{\lambda}\Delta n_{\text{eff}}, \tag{3}$$

where L_π is the active length of the phase shifter for π phase shift, Δn_{eff} is the change in effective index of the waveguide on application of external electrical field, and λ is the wavelength of light in free space. Figure 5a shows change in the optical phase shift of MOSFET on applying drain voltage from − 3 to 3 V for a waveguide length of 1.235 mm. A linear slope is observed from − 3 to 1 V and thereafter the slope decreases, because as the voltage on drain varies from − 3 to 1 V, the effective refractive index increases linearly.

After a voltage of 1–3 V, the change in effective refractive index is almost negligible, resembling a strong inversion region. Similarly, Fig. 5b shows the optical phase shift in tunnel FET on applying voltage from − 1 to 1 V for a waveguide length of 0.204 mm. A sudden change in phase shift is observed from − 1 to − 0.6 V, i.e., tremendous change at a very short voltage range. In this condition, the tunnel FET works in forward bias. Hence, a very large number of holes are injected into the intrinsic region. After a voltage of zero volt, the tunnel FET works in reverse bias, leading to negligible change in charge carrier concentration, resulting in negligible change in effective refractive index.

Considering the MOSFET device structure, Δn_{eff} of 10^{-4} is observed implying an active length of 1.235 mm. In Fig. 6a, the length for phase shift starts decreasing from − 3 to 1 V due to more negative potential difference of the gate-to-drain region. For a wavelength of 1.55 µm, L_π is 1.937 mm at $V_D = -3$ V and 1.43 mm at $V_D = 1$ V. From 1 V onward, the length reduces gradually to 1.2 mm at 3 V. As per Eq. (2), in hybrid plasmonic n-channel tunnel FET device, the n_{eff} of 10^{-3} is predicted for 1×10^{16} injection level. This implies an active length of 0.21 mm at a fixed gate voltage of 1V for a drain sweep from positive to negative.

In Fig. 6b L_π is inversely proportional to the applied drain voltage. The light guiding region is influenced by dual carrier injection effecting change in the refractive index. For example, with applied voltage of −1 V, the length is 0.4 mm, while at 1 V, the required length is 0.210 mm. Hybrid plasmonic waveguide phase modulation is greater in a device

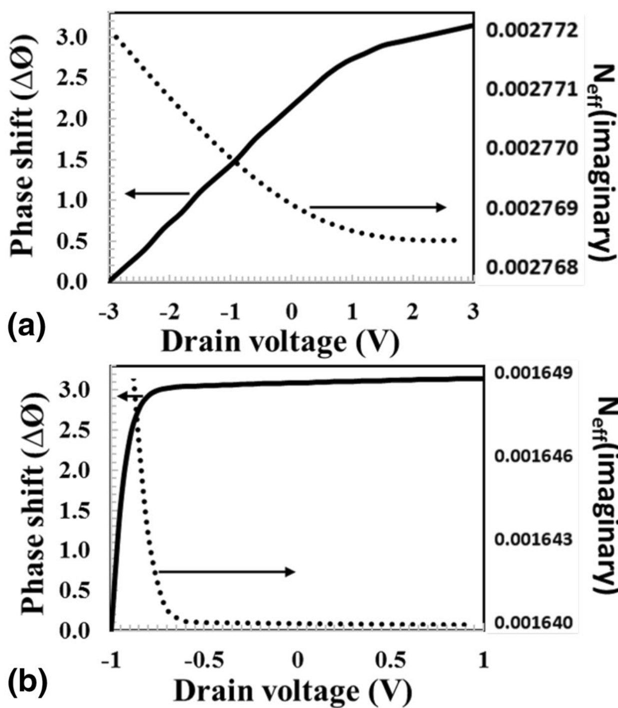

Fig. 5 Optical phase shift (solid line) in relation with change in effective refractive index on varying drain voltage at fixed $V_G = 1$ V in **a** n-type MOSFET, **b** NTFET. The dotted line shows the change in the imaginary part of the effective refractive index of the hybrid mode

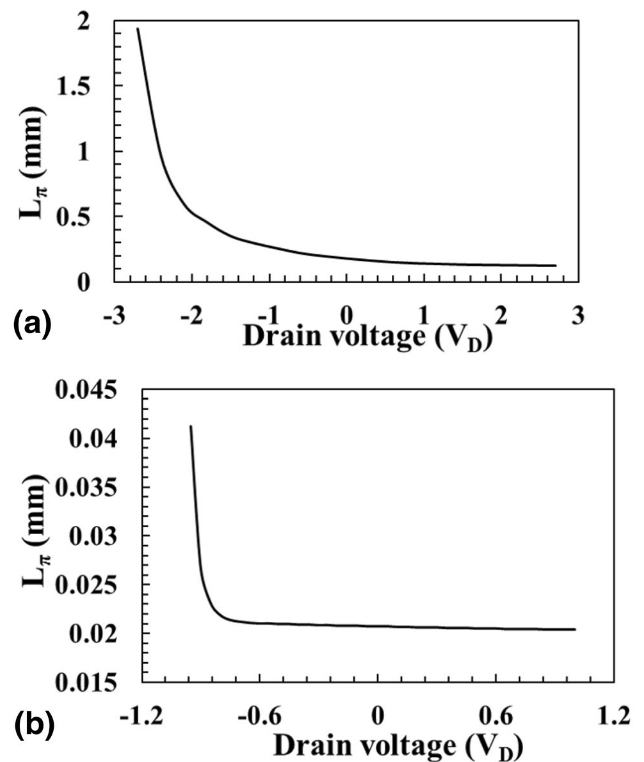

Fig. 6 Effect on L_π with change in voltage **a** from − 3 to 3 V of the proposed n-type MOSFET, **b** −1 to 1 V of the proposed NTFET for guided hybrid plasmonic mode at an optical wavelength of 1550 nm

structure similar to that of tunnel FET than in n-type MOSFET. Conventional MOSFET utilizes only one type of carrier injection (electron or hole), whereas the advantage of conventional TFET over MOSFET implies injection of both, electron and hole, increasing Δn_{eff}.

To improve the device performance to meet the requirement of application and to compete with other devices, some optimizations is further needed. Increasing the doping concentration of the source and drains can increase the device performance in terms of modulation efficiency, but with increased optical losses. The device dimension can further be optimized to achieve efficient optical coupling. For example, increasing the gate oxide thickness may lower the optical losses, but at the cost of high energy consumption to achieve pi phase shift of the optical signal. The optimization of lateral dimensions should improve the amount of charge carrier injection, which in turn may show larger change in the real part of the effective refractive index of the proposed device. These optimizations will be a subject of our near future work.

4 Conclusion

The MOSFET and tunnel FET are proposed in the form of nanophotonic devices. A nanoscale optical waveguide utilizing hybrid plasmonic concept and electrical control of guided mode are realized in FETs. An efficient optical phase modulation in the HP mode is reported in the proposed devices. The electrical and optical characteristics of the field effect transistor are studied in relation with the working mechanism of the device, perturbing the effective refractive index. Conductivity modulations in FETs are used to electrically control the optical properties due to free carrier plasma dispersion effect. The minimum length for phase shift achieved by a voltage swing of −3 V to 3 V for n-channel MOSFET is 1.235 mm, and that in n-channel tunnel FET is 0.21 mm on a voltage swing of −1 V to 1 V for the propagated hybrid plasmonic mode. The MOSFET and TFET utilize single injection carrier type and dual injection carriers, respectively, affecting the refractive index. In the n-channel tunnel FET, the observed refractive index change is 0.003 at a very small voltage range from −1 to − 0.6 V. The proposed concept can open up new areas for applications of FETs. The reported results create a novel way to use FETs in integrated photonics, thereby providing an extra degree of freedom in their applications.

Acknowledgements This work was supported in part by the Science and Engineering Research Board, India (SERB), YSS/2014/0000089, and in part by the Defence Research and Development Organization, India (DRDO) (ERIP/ER/1303134/M/01/1616).

References

1. H. Subbaraman, X. Xu, A. Hosseini, X. Zhang, Y. Zhang, D. Kwong, R.T. Chen, Recent advances in silicon-based passive and active optical interconnects. Opt. Express **23**(3), 2487–2511 (2015)
2. R. Soref, The past, present, and future of silicon photonics. IEEE J. Select. Top. Quantum Electron. **12**(6), 1678–1687 (2006)
3. T. Barwicz, H. Byun, F. Gan, C. Holzwarth, M. Popovic, P. Rakich, M. Watts, E. Ippen, F. Kärtner, H. Smith et al., Silicon photonics for compact, energy-efficient interconnects. J. Opt. Netw. **6**(1), 63–73 (2007)
4. M.A. Taubenblatt, Optical interconnects for high-performance computing. J. Lightwave Technol. **30**(4), 448–457 (2012)
5. S.J. Koester, C.L. Schow, L. Schares, G. Dehlinger, J.D. Schaub, F.E. Doany, R.A. John, Ge-on-SOI-detector/Si-CMOS-amplifier receivers for high-performance optical-communication applications. J. Lightwave Technol. **25**(1), 46–57 (2007)
6. J.S. Levy, A. Gondarenko, M.A. Foster, A.C. Turner-Foster, A.L. Gaeta, M. Lipson, Cmos-compatible multiple-wavelength oscillator for on-chip optical interconnects. Nat. Photon. **4**(1), 37 (2010)
7. C. Gunn, Cmos photonics for high-speed interconnects. IEEE Micro **26**(2), 58–66 (2006)
8. R. Kirchain, L. Kimerling, A roadmap for nanophotonics. Nat. Photon. **1**(6), 303 (2007)
9. G.T. Reed, G. Mashanovich, F.Y. Gardes, D. Thomson, Silicon optical modulators. Nat. Photon. **4**(8), 518 (2010)
10. J. Michel, J. Liu, L.C. Kimerling, High-performance Ge-on-Si photodetectors. Nat. Photon. **4**(8), 527 (2010)
11. A.W. Fang, B.R. Koch, R. Jones, E. Lively, D. Liang, Y.-H. Kuo, J.E. Bowers, A distributed bragg reflector silicon evanescent laser. IEEE Photon. Technol. Lett. **20**(20), 1667–1669 (2008)
12. A.H. Atabaki, S. Moazeni, F. Pavanello, H. Gevorgyan, J. Notaros, L. Alloatti, M.T. Wade, C. Sun, S.A. Kruger, H. Meng et al., Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip. Nature **556**(7701), 349 (2018)
13. S. Rajput, V. Kaushik, S. Jain, M. Kumar, Slow light enhanced phase-shifter based on low-loss silicon-ITO hollow waveguide. IEEE Photon. J. **11**, 1–8 (2019)
14. S. Jain, S. Rajput, V. Kaushik, M. Kumar, High speed optical modulator based on silicon slotted-rib waveguide. Opt. Commun. **434**, 49–53 (2019)
15. K. Liu, S. Sun, A. Majumdar, V.J. Sorger, Fundamental scaling laws in nanophotonics. Sci. Rep. **6**, 37419 (2016)
16. Z. Ma, M.H. Tahersima, S. Khan, V.J. Sorger, Two-dimensional material-based mode confinement engineering in electro-optic modulators. IEEE J. Select. Top. Quantum Electron. **23**(1), 81–88 (2017)
17. J. Dionne, H. Lezec, H.A. Atwater, Highly confined photon transport in subwavelength metallic slot waveguides. Nano Lett. **6**(9), 1928–1932 (2006)
18. E. Ozbay, Plasmonics: merging photonics and electronics at nanoscale dimensions. Science **311**(5758), 189–193 (2006)
19. J.A. Schuller, E.S. Barnard, W. Cai, Y.C. Jun, J.S. White, M.L. Brongersma, Plasmonics for extreme light concentration and manipulation. Nat. Mater. **9**(3), 193 (2010)
20. R.F. Oulton, V.J. Sorger, D. Genov, D. Pile, X. Zhang, A hybrid plasmonic waveguide for subwavelength confinement and long-range propagation. Nat. Photon. **2**(8), 496 (2008)
21. M. Alam, J.S. Aitchison, M. Mojahedi, Theoretical analysis of hybrid plasmonic waveguide. IEEE J. Select. Top. Quantum Electron. **19**(3), 4602008 (2013)
22. L. Singh, T. Sharma, M. Kumar, Controlled hybridization of plasmonic and optical modes for low-loss nano-scale optical

confinement with ultralow dispersion. IEEE J. Quantum Electron. **54**(2), 1–5 (2018)
23. T. Sharma, L. Singh, M. Kumar, Nanophotonic ultrashort coupler based on hybrid plasmonic waveguide with lateral subwavelength grating. IEEE Trans. Nanotechnol. **15**(6), 931–935 (2016)
24. C.A. Barrios, V.R. de Almeida, M. Lipson, Low-power-consumption short-length and high-modulation-depth silicon electrooptic modulator. J. Lightwave Technol. **21**(4), 1089 (2003)
25. A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, M. Paniccia, A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor. Nature **427**(6975), 615 (2004)
26. M. Lumerical, Solutions (2016). https://www.lumerical.com/products/device/
27. P.B. Johnson, R.-W. Christy, Optical constants of the noble metals. Phys. Rev. B **6**(12), 4370 (1972)
28. Y. Kou, F. Ye, X. Chen, Low-loss hybrid plasmonic waveguide for compact and high-efficient photonic integration. Opt. Express **19**(12), 11746–11752 (2011)
29. S.R. Giguere, L. Friedman, R.A. Soref, J.P. Lorenzo, Simulation studies of silicon electro-optic waveguide devices. J. Appl. Phys. **68**(10), 4964–4970 (1990)

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.