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An optical resilient packet ring node with SOA-based loadable and erasable storage buffer

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ABSTRACT We demonstrate a novel semiconductor optical amplifier (SOA)-based optical buffer with loadable and erasable functions and apply it in an optical resilient packet ring node. The two SOAs in our storage buffer configuration not only provide a nonlinear phase shift to implement the buffer function, but also compensate the transmission attenuation during long-time storage. The extinction ratio of this optical buffer is demonstrated to be more than 15 dB with a 2.5-Gbps packet, which indicates that power leakage from the buffer is small. The 2.5-Gbps all-optical packet switching experiment results are demonstrated with acceptable packet degradation after storage of 145 μs.

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1 Introduction

One of the key components for an optical packet switching (OPS) system is a controllable variable optical buffer, which provides a solution to avoid the switching resource contention. An optical buffer is a device with input and output data streams in the optical domain without O/E/O conversion. The performance of an optical buffer directly determines the network structure and the switching efficiency.

Currently, most of the reported optical buffers can be generally grouped into two categories: fiber-loop type and slow-light type. The slow-light optical buffer is realized by slowing down the group velocity of light propagating in a certain medium. This type of buffer appears very promising; however, there is a trade-off between bandwidth and storage time [1], and the input/output signal is sometimes difficult to couple with optical fibers. As for the fiber-loop type, one key issue is how to import/export a signal into/out of the fiber loop regarded as a loading/reading operation. Besides, another key issue is the deterioration of stored signal quality owing to the amplified spontaneous emission (ASE) accumulation, which is generated by an optical amplifier installed within the fiber loop to extend the storage time. Many configurations have been proposed to solve the problems posed in a fiber-loop optical buffer. A 10-Gbps multiwavelength fiber loop buffer was reported relying on tunable filters and semiconductor optical amplifiers (SOAs)-based wavelength converters, and the recirculating times are determined by the wavelength assignment to the optical signal [2]. Also, several nonlinear recirculating optical buffers have been demonstrated with a 10-Gbps terahertz optical asymmetric demultiplexer (TOAD) [3] or a 40-Gbps ultra-fast nonlinear interferometer (UNI) structure [4]. To extend the storage time, the application of another TOAD in the fiber loop will ameliorate ASE accumulation by regenerating packets in every round trip [3].

Recently we proposed a controllable, dual-loop optical buffer (DLOB) configuration [5]. In this paper we will extend the reported configuration and further demonstrate the 'erase' function for this buffer. The underlying principle is based on generating a nonlinear phase shift with SOAs to implement loadable and erasable functions. Compared with other works, there are some merits of our DLOB, such as short fiber loop, compact configuration, and low power requirement of the optical control signal. In particular, we will apply this novel optical buffer to a 2.5-Gbps optical resilient packet ring (RPR) node design. The current RPR network is based on electronic buffers in which data packets are stored and switched out through O/E/O conversion, which significantly limits its traffic throughput [6]. We demonstrate that the optical RPR network, in which the electronic buffer is replaced by an all-optical buffer, will significantly simplify node structure and enhance traffic capacity owing to elimination of the O/E/O conversion process. To the best of our knowledge, it is the first time that an optical buffer has been applied to a RPR network.

2 Principle of DLOB

The configuration of our DLOB with 'erase' function is shown in Fig. 1. The four side ports (port 1 to port 4, port 3 to port 6) of a 3×3 collinear coupler are connected accordingly to form a horizontal '8' figure. Two polarization controllers (PCs) are used to bias the loops. Four wavelength demultiplexers (WDMs) and the two SOAs are employed to generate a nonlinear phase difference (NPD) between signals propagating in clockwise (CW) and counter-clockwise (CCW) directions in each loop, with the assistance of a control

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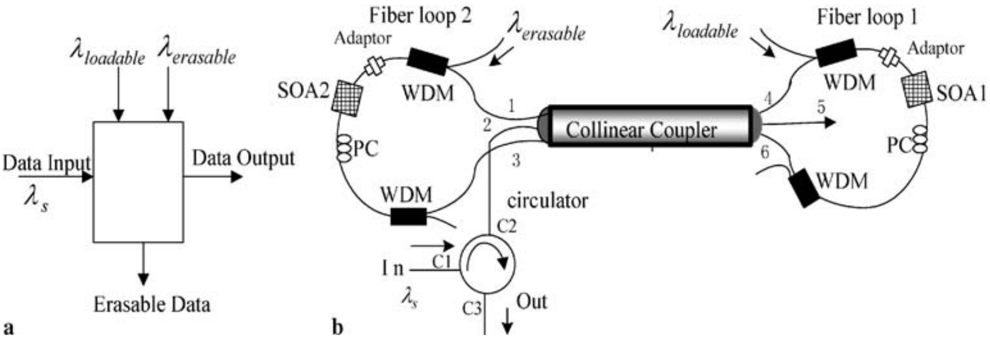

FIGURE 1 Schematic diagrams of a DLOB with loadable and erasable functions. (**a**) Ports of the proposed DLOB. (**b**) Schematics of the buffer with a horizontal figure-8 configuration

light. A packet signal, launched in port C1 of the circulator, is split into two portions with equal power traveling in CW and CCW directions in loop 1. The CW and CCW signals meet again at ports 4 and 6 after one full circulation in the loop 1. They interfere and combine to port C3 of the circulator under the condition that those two signals are biased to have the same state of polarization. If we introduce an optical 'load' signal synchronized with the CW signal into SOA1, and the NPD between CW and CCW signals reaches π, the signals will transfer into loop 2. No signal will appear at port C3 of the circulator, which implies that the input signal has been loaded in the DLOB. After the signal circulates several times in the horizontal figure-8, we inject another optical 'read' signal to SOA1 to generate another π NPD between signals propagating in two directions of the fiber loop 1; the stored signal will leave the figure-8 fiber loop completely and appear at port C3 of the circulator.

When erasing is required for the data packet circulating in the fiber loop, we can inject another optical signal with different wavelength, named the 'erase' signal, into the fiber loop 2. When the optical 'erase' signal propagates with the CW signal into SOA2 synchronously, and the NPD between CW and CCW signals reaches 2π in the fiber loop 2, the signal will appear at port 5 of the 3×3 coupler, named as the erase port. Since no signal will be reflected into the fiber loop 1 theoretically, there will be no data in the optical buffer, and the buffer is ready for the next packet storage.

The NPD $\Delta\varphi$ and gain ratio $m = g_{\mathrm{cw}}/g_{\mathrm{ccw}}$ for the two different directions of the SOA are coupled by the line width enhancement factor α of the SOA [7]:

$$\Delta\varphi = -\frac{\alpha}{2}\ln\left(\frac{g_{\mathrm{cw}}}{g_{\mathrm{ccw}}}\right) = -\frac{\alpha}{2}\ln(m). \tag{1}$$

Here $g_{\mathrm{cw}}(t)$ and $g_{\mathrm{ccw}}(t)$ are the SOA amplitude gains in the two different propagating directions. Considering the ideal condition of a 3×3 collinear coupler [5], we derived the extinction ratio (ER) for loading, reading, and erasing applications as

$$\mathrm{ER} = 10 \times \log\left(\frac{P_{\mathrm{packet}}}{P'_{\mathrm{packet}}}\right) = 10 \times \log\left(\frac{1+\mathrm{e}^{2\pi/\alpha}}{1-\mathrm{e}^{2\pi/\alpha}}\right), \tag{2}$$

where P_{packet} and P'_{packet} are the packet power with and without the control signal, respectively. According to (2), it is obvious that the ER value is related to the line width enhancement factor α of the SOA, which is often used to calculate nonlinear phase shifts from the gain variations. For all the applications, the extinction ratio can be at least 15 dB when α is larger than 15.

The two SOAs in the fiber loop not only compensate the power attenuation during propagation in the fiber loop, but also generate a nonlinear phase shift to realize 'load' and 'erase' functions. According to a measurement by Schares et al. [8], the nonlinear phase shift increases with the bias current, control pulse energy, and SOA length, and decreases with the repetition rate. Even for a 40-Gbps signal, a phase shift of over π can be achieved in a 1.5-mm-long bulk InGaAsP–InP SOA; therefore, the operation bit rate of our optical buffer can be scaled to 40 Gbps with a long-cavity SOA. The storage time for this optical buffer can be adjusted at integer multiples of the fiber loop delay. Since the fiber loop delay is stable and can be calculated by the node control unit (NCU), it is easy to generate correct control signals for packet scheduling.

3 Optical RPR node design

Once an optical packet enters the OPS node, only the optical header undergoes O/E conversion for determining the packet's routing information. We propose to implement a three-node optical RPR network, with a DLOB incorporated in each node, as shown by Fig. 2. Because of the ring topology, we assume that the packets arrive in a synchronized fashion. The optical power of an optical packet arriving at the node is split into two asymmetrical portions. The signal with smaller power will be used to implement head recognition to determine whether this data packet belongs to the current node. Simultaneously, the other signal with most of the optical power is delayed by a 500-m single-mode fiber and waits for the switching operation from the NCU. Although significant progress has been made in the all-optical signal processing area, including Boolean logic gates, clock-recovery circuits, and header separation and recognition [9], the enrollment of electronics for the NCU is necessary due to the complex structure of present all-optical processing techniques. After serial to parallel conversion, the received signal is converted to the correct input level for an Altera field programmable gate array (FPGA) with parallel 155-Mb/s processing capacity to implement header reorganization and complex control functions.

If the objective address in the packet head is equal to the address of the current node, the NCU will give a downstream signal to drop the buffered packet; otherwise, the NCU will forward the packet to the output port of the node. There might be a conflict between an upstream packet and a forwarded

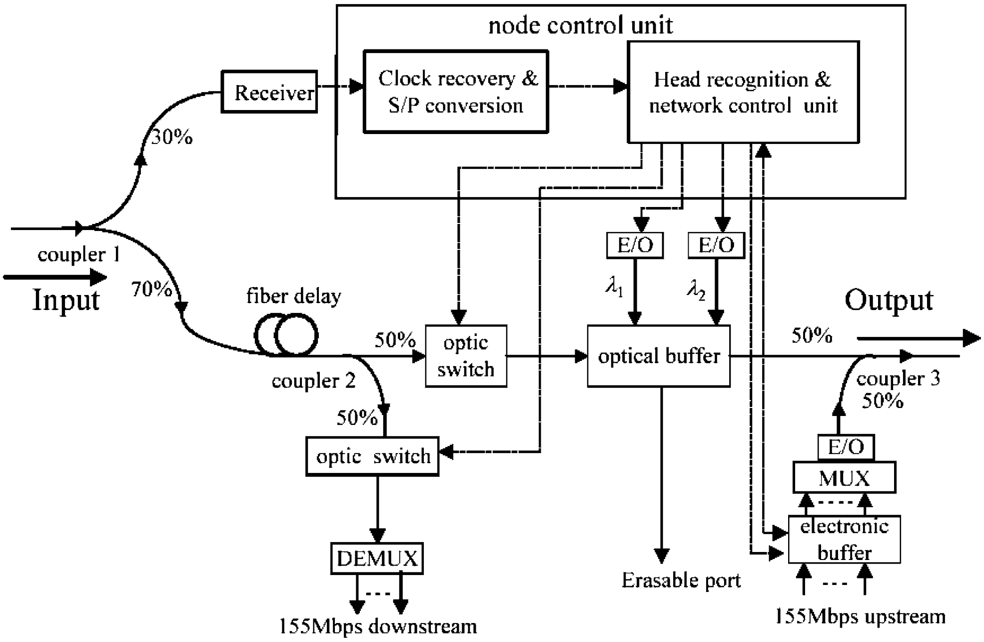

FIGURE 2 Demonstration of an optical resilient packet ring node structure with the DLOB. Traffic from the ring network is coupled to the node input port. $\lambda_1 = 1556.56$ nm and $\lambda_2 = 1553.36$ nm are selected as the loadable and erasable wavelengths. The *solid line* and *dashed line* show the optical connection and electrical connection in the node, respectively

packet. Here we assume that the upstream packet has the lower priority to enter the ring, while the forwarded packets have the higher priority to pass the node. Thus, if such packet contention takes place, the upstream packet will be buffered by an electronic buffer. However, to ensure the integrity of the upstream packet, the NCU will give out a 'load' signal for storing the forwarded packet into the DLOB before it reaches the output port, if the output port is detected to be occupied by one upstream packet. Once the transmission of this ongoing upstream packet is complete, later upstream packets will be buffered by the electronic buffer. Simultaneously, the forwarded packet in the optical buffer will be transmitted to the node output port. The 'erase' function of the optical buffer is useful for providing service priority, network configuration and loop-back diagnostics applications.

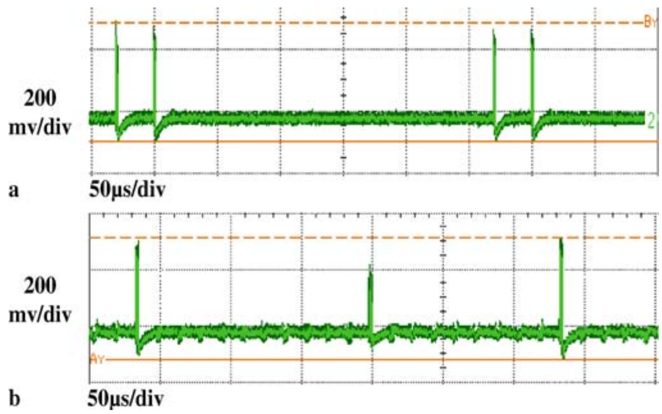

FIGURE 3 (**a**) Two-packet profile before arriving at the node input port. (**b**) Two-packet profile observed at the node output port. The first packet passes the node directly and the second is buffered for 145 µs

4 Experiment

In our particular experiment, the bit rate of the packet is 2.5 Gbps. The cycle of the data packet is 5 µs, and the guard time is 2.8 µs for each packet. The header is 15 bytes including a synchronization bit, source address bits, objective address bits, and service-class bits. The payload is generated with $2^7 - 1$ pseudo random binary pulse sequence (PRBS) data. Two SOAs, with bulk InGaAsP–InP structure from Inphenix, are biased at 160-mA current, and the total delay of one circulation in the horizontal '8' figure is 15 µs. Three distributed feedback (DFB) laser modules with maximum output power of 10 dB m at different wavelengths are used as the loadable ($\lambda_1 = 1556.56$ nm), erasable ($\lambda_2 = 1553.36$ nm), and packet signal ($\lambda_s = 1559.89$ nm) light sources, respectively. These wavelengths are chosen for peak SOA gain, and otherwise they are not special. Two $LiNbO_3$ modulators driven by control signals from the NCU are chosen as optical switches in Fig. 2.

Primarily we demonstrate the 2.5-Gbps packet buffering in the optical RPR node. The NCU generates different control signals for two packets based on schedule strategy (Fig. 3a). The first packet passes through the node directly, whereas the second is purposely buffered for 145 µs and then forwarded to the output port (Fig. 3b). We compare the packet waveform with the eye-diagram in Fig. 4a–c, and observe that although the peak power of the buffered packet is 4.1 dB lower than that of the original packet, no shape deformation of these two packets occurs. The gain decreases because of gain saturation, which results from the high-power control signal. Hence, the buffered signal receives less gain compared with the case where the signal packet passes through directly. Due to the ASE noise accumulation, the packet signal after storage becomes noisy. We collect the timing-jitter value from a Tektronix CSA8000 oscilloscope directly; the root mean square (RMS) value of the timing jitter is around 5–8 ps.

We then fix the power of the packet signal and the control signal as −2.8 dB m and 4.8 dB m, respectively, and monitor the ER value by adjusting the SOA bias current. The ER value for each operation can achieve 18.9 dB at the sig-

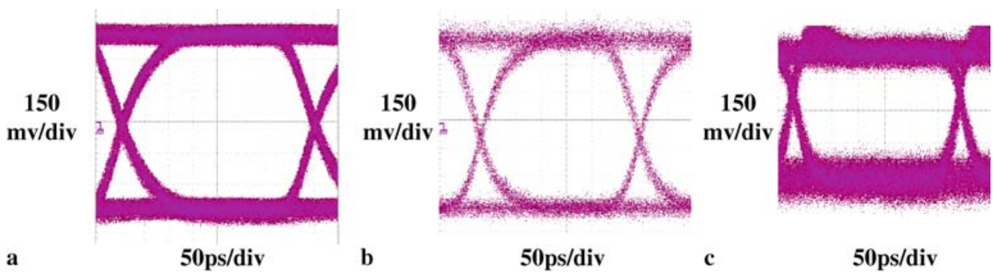

FIGURE 4 Comparison of the eye-diagrams of the 2.5-Gb/s packet signal. (**a**) Signal eye-diagram of the input packet before entering the node input port. (**b**) Signal eye-diagram of the first packet passing the node directly. (**c**) Signal eye-diagram of the second packet passing the node after 145-µs storage

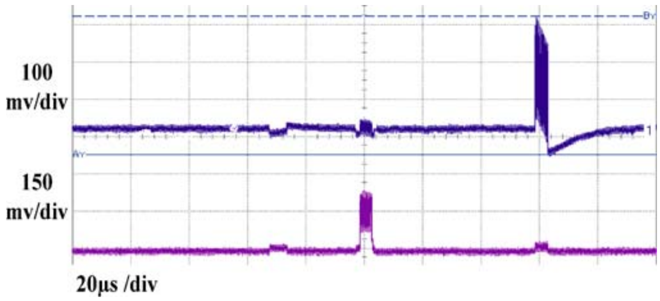

FIGURE 5 Demonstration of the erasable function

nal output port when the SOA bias current is 160 mA. We believe the NPD π can only be obtained in this bias current for this type of SOA, and the ER value will drop dramatically under a different bias current. We also change the switching logic in the NCU to verify the 'erase' function in the optical buffer. Two packets enter the DLOB. The first packet is forwarded to the node output port after a storage time of 40 µs and the second is erased after 30-µs storage according to the different switching signals from NCU. The top waveform in Fig. 5 is observed at the node output port and the bottom waveform in Fig. 5 is measured at the erasable port. The crosstalk is suppressed to less than 18 dB between those two ports; therefore, we can conclude that an 'erase' function in the optical RPR node is successfully demonstrated. Finally, we measure the eye-diagram of a downstream packet with a 1-GHz Agilent oscilloscope after demultiplexing from 2.5 Gbps to 155 Mbps. We have shown one of the worst 155-Mbps signals from 16 channels in Fig. 6. However, it shows that the downstream packet remained of very high quality under the control of proper switching signals.

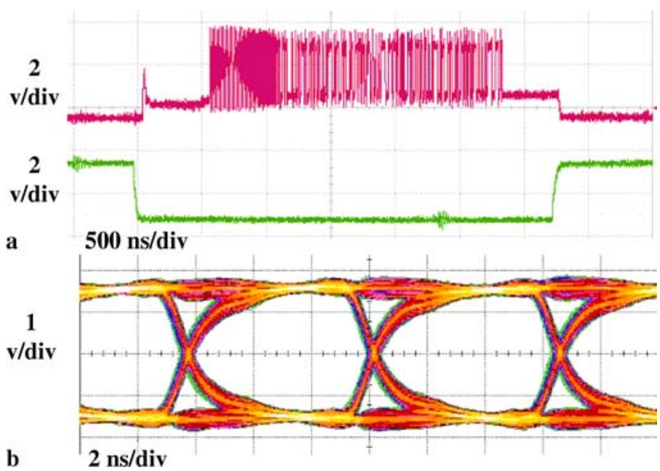

FIGURE 6 Waveform and eye-diagram of 155-Mb/s downstream packet signal after demultiplexing. (**a**) The *top waveform* is a 155-Mb/s downstream packet and the *bottom waveform* is the control signal generated from the node control unit. (**b**) The eye-diagram of a 155-Mb/s downstream packet signal

5 Conclusion

We proposed an optical RPR node design with a novel SOA-based optical buffer with loadable and erasable functions. Two SOAs are used as a nonlinear element as well as a power compensator in the configuration. The ER of loadable and erasable operations for this kind of buffer is measured to be more than 15 dB, which means that the crosstalk of the DLOB is small. Though the optical power of the buffered packet is 4.1 dB lower than that of the original packet due to SOA gain saturation, the packet pattern is maintained quite well. In addition, we have successfully demonstrated a 2.5-Gbps switching operation with the proposed DLOB. By choosing a long-cavity SOA and a high control signal power, our proposed node structure can be updated to a 40-Gbps operation theoretically.

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