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Optimising dislocation-engineered silicon light-emitting diodes

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ABSTRACT This article presents a study of the possibilities of optimising the electroluminescence (EL) efficiency of dislocation-engineered silicon light-emitting diodes (DELEDs). The diodes were produced by implantation of boron in n-type (100)Si wafers, at a constant ion energy and fluence, of 30 keV and 1×10^{15} ions/cm^2, respectively. The density and the areal coverage by dislocation loops were varied by applying different annealing times in a rapid thermal processing, from 30 s to 60 min. It is shown that the EL efficiency is directly correlated to the number and areal coverage by the loops. The highest population of loops, $\sim 5 \times 10^9$ /cm^2, and an areal coverage of around 50% were achieved for 1–5 min annealing. This loop distribution results in optimal DELEDs, having the highest EL response and the largest increase of EL intensity with operating temperature (80–300 K). The results of this work confirm a previously introduced model of charge-carrier spatial confinement by a local stress induced by the edge of the dislocation loops, preventing carrier diffusion to non-radiative recombination centres and enhancing radiative transitions at the silicon band edge.

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1 Introduction

Light-emitting devices produced from silicon or silicon-based materials are a goal as an ultimate solution of optical interconnects, for further progress in ultra-large-scale integrated (ULSI) silicon technology. The main problem in achieving this goal is the indirect band gap nature of silicon, resulting in inefficient light emission. A number of approaches to overcome this problem were reported, such as light emission from porous silicon [1], silicon/silicon dioxide superlattices [2, 3], erbium precipitates in silicon [4], silicon/germanium [5] and iron disilicide precipitates in silicon [6]. However, a basic disadvantage in these devices is either thermal quenching leading to a low emission at room temperature, or incompatibility with standard ULSI routines; none of them so far being applied commercially.

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Efficient light-emitting diodes operating at room temperature can be produced by dislocation engineering in silicon [7], using standard ULSI procedures involving ion implantation of boron and a subsequent thermal processing. The role of boron implantation is to induce the formation of dislocation loops, as well as to provide p-type doping in the n-type silicon substrate. Interstitial dislocation loops induce a local strain that increases the silicon band gap at their outer edge by up to 0.75 eV, thus enabling spatial confinement of the injected carriers and suppressing their diffusion to non-radiative recombination centres in favour of radiative transitions [7, 8]. As opposed to conventional silicon where luminescence thermally quenches, electroluminescence (EL) of dislocation-engineered light-emitting diodes (DELEDs) increases with temperature. Furthermore, the estimated room-temperature quantum efficiency of these devices is comparable to commercial III-V semiconductor LEDs [7, 9].

Ion-implantation-induced formation and evolution of crystal defects and dislocation loops in silicon as a function of irradiation and annealing parameters were studied extensively [10–17]. These studies have shown that dislocation loops are extrinsic in nature, having {111}Si habit planes, and consisting of perfect and faulted Frank loops with Burgers vectors $a/2\langle 110\rangle$ and $a/3\langle 111\rangle$, respectively. In a previous publication [18] we have demonstrated a possibility of controlling the depth distribution and the mean size of dislocation loops in (100)Si, by varying the boron ion energy over 10–80 keV. In this work we have applied constant irradiation parameters, 30-keV boron implants of 1×10^{15} ions/cm^2, in (100)Si wafers, and studied the influence of the annealing time on the growth and evolution of dislocation loops and on EL efficiency of DELEDs fabricated from this material. It was found that the EL efficiency can be directly correlated to the loop density and areal coverage.

2 Experimental procedures

Silicon DELEDs were fabricated from phosphorus-doped n-type (100)Si wafers (2–7 Ω cm) implanted with boron. Implantation of B^+ ions was performed at a constant energy of 30 keV and a constant fluence of 1×10^{15} ions/cm^2. The wafers were inclined by 7° off normal incidence, and implanted with an ion beam current of $\sim 1\ \mu$A/cm^2, at ambient temperature. The projected 30-keV boron range in Si

is R_p = 110 nm, and straggle ΔR_p = 39 nm, according to TRIM [19]. After implantation the wafers were processed by rapid thermal annealing (RTA) in a nitrogen ambient, at 950 °C, from 30 s to 60 min.

Structural characterisation of Si samples, prepared for plan-view and cross-sectional imaging, was done by transmission electron microscopy (TEM), using Philips EM 400 T and CM 200 microscopes. For plan-view imaging we used an off-axis four-beam imaging condition near [001]Si, which allows simultaneous observation of both perfect and faulted dislocation loops, having different Burgers vectors, as described previously [18]. Cross-sectional imaging was done near the [110]Si zone axis. We also used channelling Rutherford backscattering spectroscopy (RBS), with a 1.5-MeV He^+ ion beam, to study the damage distribution in Si.

The diodes were formed by depositing an Al contact on the front p-side and an AuSb contact on the back side of the n-Si substrate, and a selective etching to isolate the p-n junction. A window was left open on the back side of the diodes to measure the electroluminescence. The surface area of the diodes is 8×10^{-3} cm^2. Their schematic presentation and a more detailed description of the fabrication procedure is given elsewhere [7, 8, 20]. EL measurements were performed under forward bias, with the current density of 2 A/cm^2, detecting the light emission by a liquid-nitrogen-cooled germanium p-i-n detector, in a conventional 0.5-m spectrometer. Temperature dependence of EL was measured in the range 80–300 K, the samples being mounted in a continuous-flow liquid-nitrogen cryostat. Prior to EL experiments we have measured the current–voltage characteristics of the diodes.

3 Results

3.1 *Structural characterisation*

The results of TEM analysis show that dislocation loops develop after annealing for 30 s. However, they increase in number and size after annealing for 1–5 min, and after annealing for 10–60 min their density and size gradually reduce. In all cases we observe both perfect and faulted loops, in {111}Si habit planes. To determine the type of loops and their habit planes we have used different sample tilts and trace analysis, as described in detail earlier [18].

Figure 1 shows bright-field plan-view TEM images of samples annealed for 30 s and 1, 5 and 40 min, taken for four-beam alignment near the [001]Si zone axis. After 30-s annealing we observe dislocation loops ranging from ∼ 25 nm to ∼ 400 nm. The smaller loops are either faulted or perfect, and the irregularly shaped large ones are all perfect dislocation loops. Examples of faulted and perfect loops are indicated by markers. Annealing for 1 min yields a higher density of both types of loops, their size being close to those formed after 30-s annealing. A prolonged annealing for 5 min induces a substantially higher number of large perfect loops, up to ∼ 500 nm, coexisting with smaller loops of ∼ 25 to ∼ 150 nm. With further increase of the annealing time, perfect loops reduce in size, and also the total number of both types of loops reduces. However, we also observe that faulted loops increase in size. The image taken from the sample annealed for 40 min shows perfect loops of up to ∼ 190 nm and faulted loops of up to ∼ 200 nm.

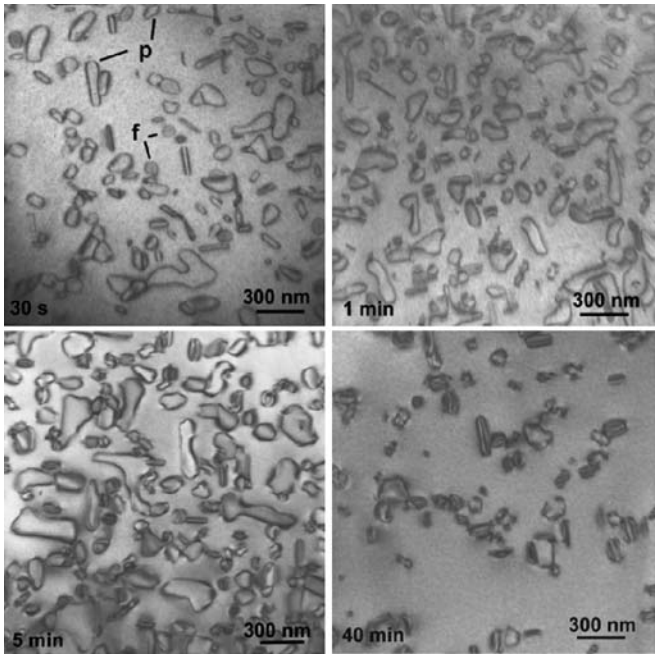

FIGURE 1 Plan-view bright-field TEM images of Si samples annealed for different times, taken near [001]Si. Examples of perfect loops are marked as p and faulted as f

Figure 2 shows bright-field cross-sectional TEM images of samples annealed for 30 s and 10 and 40 min, taken near [110]Si. In the sample annealed for 30 s the loops are distributed from the surface to approximately the end of the boron range (∼ 200 nm). For 10-min annealing the loops are more uniform in size, and confined around the projected boron range (110 nm). In the sample annealed for 40 min there are loops located around the projected ion range, but also some of them diffuse to the surface.

In Fig. 3 we have plotted the density of dislocation loops (a), the estimated areal coverage by the loops (b), and the estimated total circumference of the loops (c), as a function of annealing temperature for the samples analysed by TEM. It is seen that the maximum number of loops is reached after annealing for 1 min. The maximum areal coverage, of ∼ 55%, is reached after 5-min annealing. However, when comparing the circumference of the loops, the total circumferance of all the loops after 1-min annealing is much closer to that achieved after 5-min annealing, and drops considerably after annealing for 10 min. For these statistics we have analysed a total area of $4 \times 4\,\mu$m^2, containing above 1000 loops for the highest population. To determine the areal coverage and circumference we assumed a circular shape of the loops, lying in {111}Si planes. These planes are inclined by 35.3° to the [001]Si zone axis. Hence, circular loops appear as having an oval shape, elongated along ⟨110⟩ directions, their longer dimension corresponding to the actual diameter. The largest irregularly shaped perfect loops were divided into smaller parts, considered to consist of coalesced circular loops, taking into account only the total outer circumference. In plan-view images we see occasional trace lines, originating from the loops cut off at the surface, which were not considered in the statistics. An estimated error in these calculations is up to ∼ 20% for denser populations,

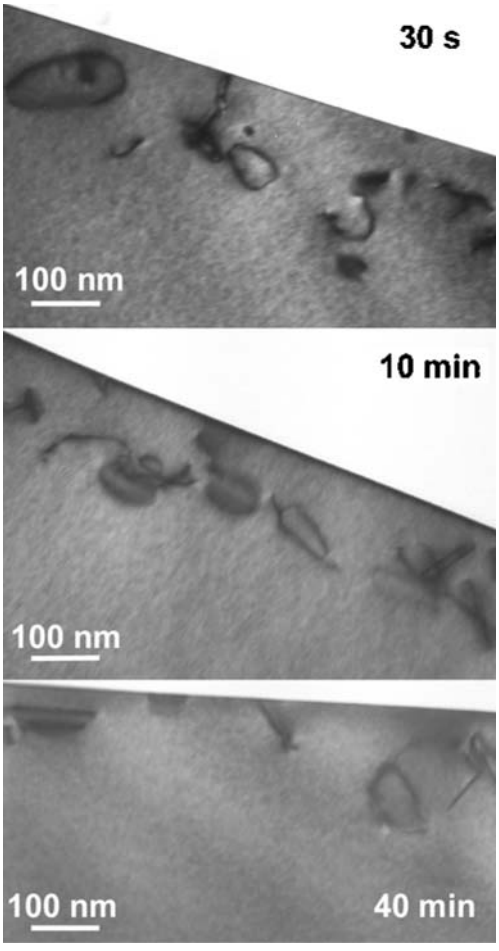

FIGURE 2 Cross-sectional bright-field TEM images, taken along [110]Si, of samples annealed for different times

though the plotted graphs give an indication of the general trend.

RBS channelling spectra, taken from non-implanted, as-implanted and samples annealed for 30 s and 1 and 40 min, are given in Fig. 4. In (a) and (b), the spectra were taken along the [110]Si channel, in order to achieve a higher depth resolution. The samples were tilted by $\sim 45°$ off normal incidence. In (a) we can see the distribution of crystal damage in the as-implanted sample, the increased backscattering yield arising mainly from Si interstitials. It is seen that the applied boron fluence is below the amorphisation threshold, the height of the damage peak being far below the random level. The spectra shown in (b) illustrate the damage distribution after annealing. After 30 s the damage is reduced, although there is still a considerable backscattering yield immediately below the surface Si peak, suggesting the presence of interstitials not trapped by the loops. After 1-min annealing the yield below the surface peak drops close to the virgin level, but it increases towards the deeper region of the sample. Here we have marked a small peak on the spectrum, which indicates the inner edge of the formed layer of dislocation loops. A more detailed description of a similar analysis, showing the depth and thickness of the layer consisting of dislocation loops, was given previously [18]. The spectra shown in (c) were taken at normal incidence, along the [100]Si channel. They show

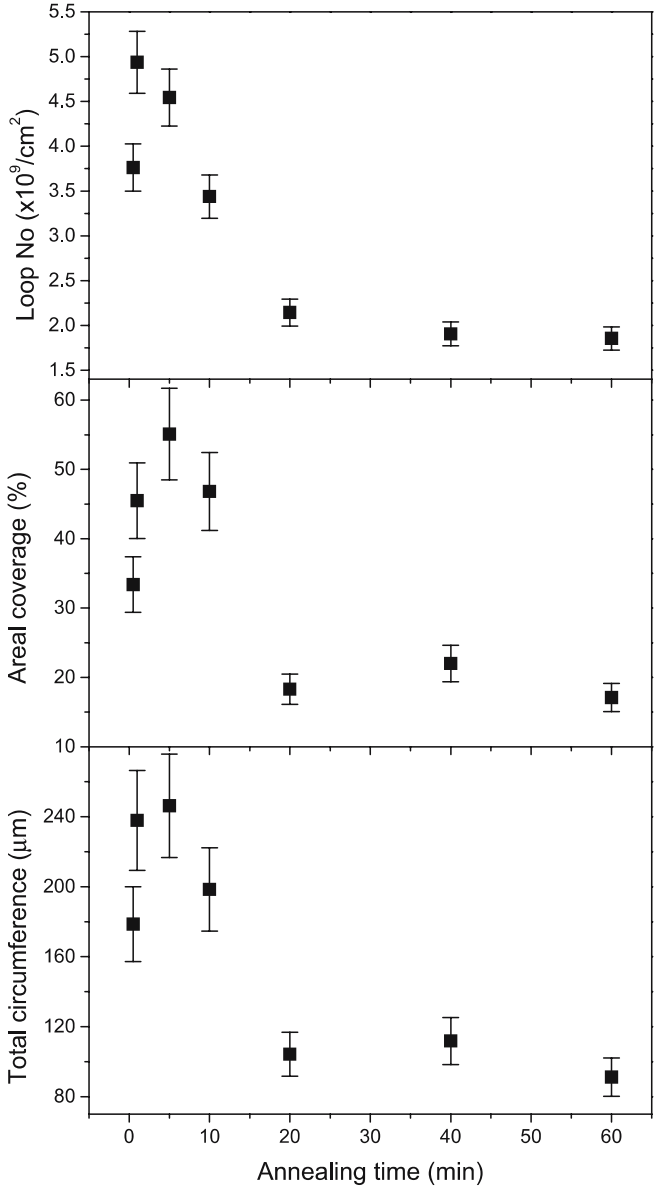

FIGURE 3 The number of dislocation loops (**a**), the areal coverage by the loops (**b**), and the total circumference of the loops (**c**); from an analysed area of 4×4 μm^2, as a function of annealing time

a lower degree of crystal damage for longer annealing. These results are consistent with TEM analysis, where we have seen a lower density and smaller dislocation loops. RBS analysis also shows the presence of native oxide at the surface, increasing with annealing time and inducing a higher Si surface peak in the spectra. This oxide layer was removed by HF etching, prior to depositing the front Al contacts on DELEDs.

3.2 *Electroluminescence analysis*

Room-temperature electroluminescence spectra show a distinct peak at 1.1 μm, corresponding to the phonon-assisted silicon band-edge emission. No other luminescence features are observed. In particular, the D-line emission often associated with dislocated silicon is absent. D-line luminescence is associated with threading dislocations that are

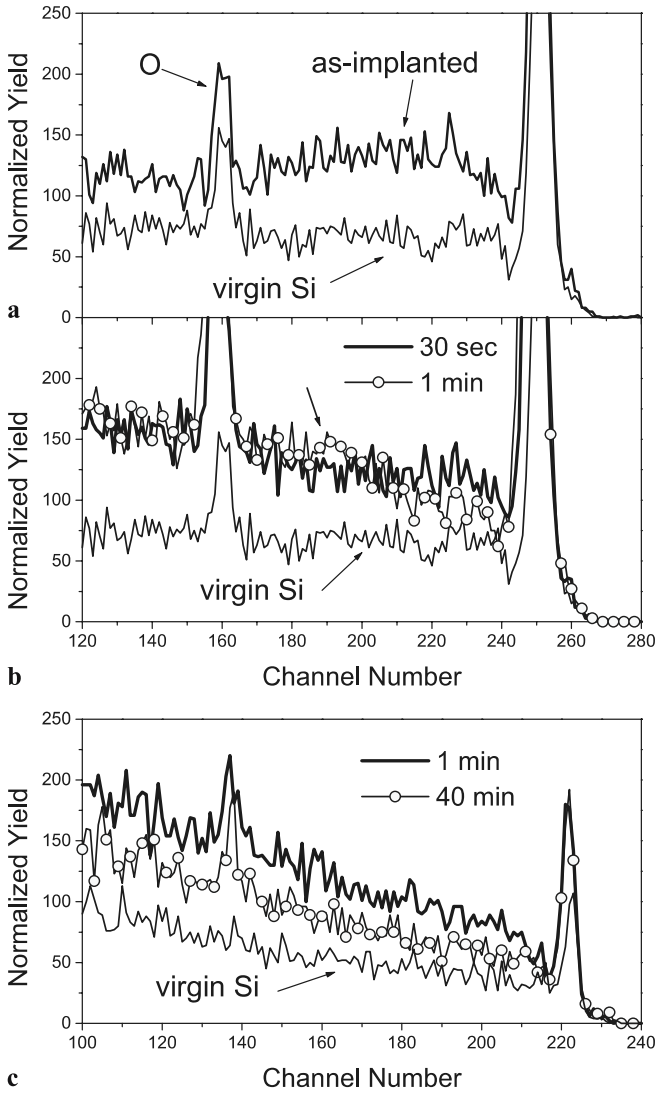

FIGURE 4 RBS analysis of as-implanted and annealed Si samples: (**a**) and (**b**) channelling spectra along [110]Si; (**c**) channelling spectra along [100]Si

not present in our samples, rather than the loops which act here as a strain-induced diffusion barrier which localises the carriers in the defect-free silicon layer adjacent to the depletion-region edge where recombination occurs. However, the EL efficiency varies with the annealing processing of the Si wafers, and the measurement temperature (80–300 K). Current–voltage measurements show that the turn-on voltage is below 1 V, the characteristics of similar diodes being presented elsewhere [7, 8, 21]. The estimated position of the p-side of the depletion region is at a depth of $\sim$ 350 nm, meaning that the loops are located within the p-type region of the junction.

Figure 5 shows the room-temperature EL spectra of DELEDs fabricated from Si wafers annealed for 30 s and 1, 5, 40 and 60 min. They illustrate the influence of dislocation loop density on EL efficiency. The strongest EL response comes from the samples annealed for 1 and 5 min. The room-temperature integrated EL intensity as a function of annealing temperature is plotted in Fig. 6. It is seen that the EL efficiency follows the trend presented for the dislocation loop

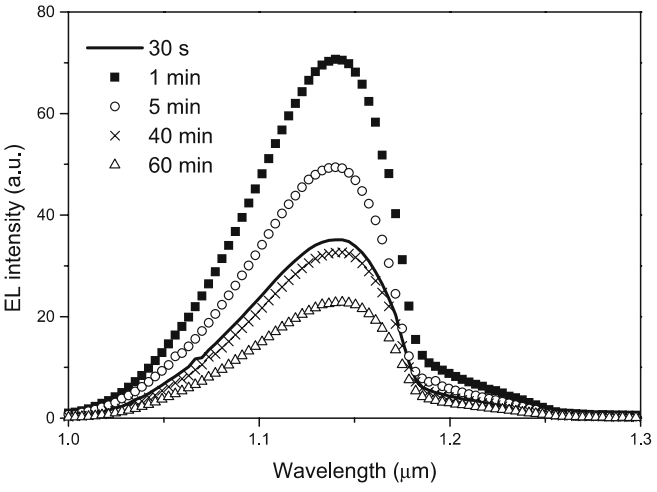

FIGURE 5 Room-temperature electroluminescence response of DELEDs produced from Si wafers annealed for different times

density (Fig. 3). The maximum EL intensity was achieved from the sample annealed for 3 min. This annealing time is within the range where we reach the highest population of dislocation loops and an optimal areal coverage of around 50%. Photoluminescence (PL) measurements have been carried out on all the samples and show a trend with annealing identical to the EL measurements. It is worth noting that the current voltage (I–V) characteristics of the devices are identical over the full range of annealing temperatures used [21], indicating no significant change in the carrier-injection conditions with annealing. This is because the I–V characteristics of a diode are determined only by the p-n junction height. Here the strain field of the dislocation loops has decayed to close to zero at the junction depth ($\geq$ 350 nm) and so the junction height and injection are independent of the presence or absence of the dislocation loops. Diffusion of boron during prolonged annealing may influence the junction depth, though the peak p-doping is maintained in the range of 10^{19} /cm^3. Furthermore, recently we have demonstrated that inducing the dislocation loops within the p-region of the junction is crucial for efficient EL of the diodes [22].

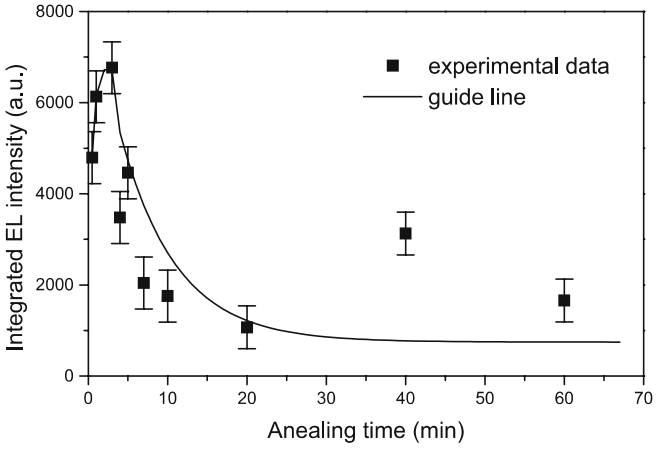

FIGURE 6 Room-temperature integrated EL intensity of silicon DELEDs as a function of annealing time. The *solid line* is a guide for the eyes

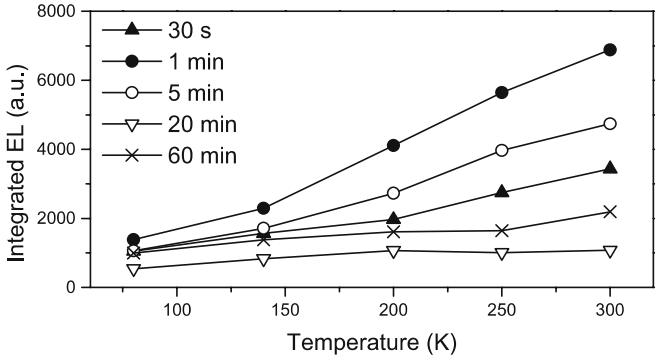

FIGURE 7 Integrated 1.1-μm peak EL intensity of silicon DELEDs as a function of measurement temperature

In Fig. 7 we have plotted the integrated 1.1-μm peak EL intensity as a function of the measurement temperature of DELEDs, fabricated from Si wafers annealed for different times. The plots show that the highest EL intensity, in the whole temperature interval, is achieved from the sample annealed for 1 min. The next highest EL intensity comes from the sample annealed for 5 min. It can also be seen that the biggest increase of EL with measurement temperature comes from the samples annealed for 1 and 5 min, having the highest density or the largest areal coverage by dislocation loops.

4 Discussion

Studies of ion-implantation-induced dislocation loops in Si [10–18] suggest that they are extrinsic in nature, formed from Si interstitials generated in collision cascades. By a categorisation introduced by Jones et al. [12], our case belongs to type I damage, when the Si substrate is not amorphised, but the implanted fluence is above a critical value of $\sim 2 \times 10^{14}$ ions/cm^2. Introduction of foreign atomic species induces an increased local density in the host material. Simulations of the crystal damage, using the TRIM code, indicate that interstitials are generated deeper in the substrate and vacancies closer to the surface [17]. The majority of induced interstitials and vacancies recombine upon post-irradiation annealing, but there are excess Si interstitials due to the introduced doping species, which preferably occupy substitutional sites in the lattice. The excess Si interstitials nucleate in the form of {113} rod-type defects, and faulted and perfect dislocation loops in {111}Si planes, depending on the annealing time and temperature. For longer annealing times and higher temperatures, the presence of extrinsic defects reduces, the excess interstitials either being incorporated in the main crystal matrix, or diffusing to the surface. Studies of the Si surface proximity on evolution of dislocation loops upon annealing suggest that it acts as a sink for Si interstitials [15].

In our experiments, 30-keV boron ions can be considered as shallow implants, the loops being located around the projected ion range of 110 nm, and spreading to the Si surface. Post-implantation processing by RTA at 950 °C induces the highest loop density and areal coverage after 1–5 min. Also, the most efficient EL is achieved from DELEDs produced from Si wafers annealed within this time interval. According to the mechanisms suggested for the formation of dislocation loops, these conditions are reached when practically all excess Si interstitials are trapped by the loops. For a shorter annealing (30 s) there are excess interstitials not bounded by the loops, which can act as point-defect centres for non-radiative recombinations. For a prolonged annealing, dislocation loops first coalesce in the form of larger loops (5 min), and then ($\geq$ 10 min) gradually decrease in size and density. Being relatively close to the surface, it can be assumed that the loops are dissolved partly by incorporation of Si interstitials in the basic crystal matrix, and their simultaneous diffusion to the surface.

EL measurements indicate that the most efficient spatial confinement of charge carriers is achieved by smaller and denser dislocation loops. Previous studies gave an estimate of the local stress induced by interstitial loops, calculated using the standard elastic theory of dislocations and the known values of Poisson's ratio and Young's modulus for silicon [7]. The induced stress increases the band gap in the vicinity of the outer loop edge by up to ~ 0.75 eV. This applies to both faulted and perfect dislocation loops, the latter not having stacking faults, but introducing an extra layer in the Si crystal matrix. The model is presented schematically in [8, 23], proposing that the carrier confinement occurs between the strain barrier resulting from the edges of the loops and the depletion-region edge. The present work confirms this theory, showing that dense smaller loops, giving a larger total length of the edge circumference, are dominant for efficient EL. This is illustrated, for example, by comparing the samples annealed for 1 and 10 min. The sample annealed for 1 min has a higher density of dislocation loops, while the areal coverage is slightly higher in the sample annealed for 10 min, but the total circumference of the loops is again higher in the sample annealed for 1 min. A larger loop circumference can also explain a non-expected higher EL intensity of the sample annealed for 40 min, compared to those annealed for 20 and 60 min. The absence of thermal quenching, i.e. the anomalous increase of EL intensity with the measurement temperature, indicates that optimal annealing induces the loop distribution that enables a maximum carrier confinement, in minimising their diffusion to non-radiative recombination centres.

5 Conclusions

The results of structural and EL analysis of silicon DELEDs show a dominant role of dislocation loop density and areal coverage on light-emission efficiency. The optimal conditions were achieved for 1–5 min annealing, when the number of loops reaches a maximum of $\sim 5 \times 10^9$ /cm^2 and the areal coverage is around 50%. These findings confirm the model that spatial confinement of charge carriers at the edge of the loops is crucial for preventing their diffusion to non-radiative recombination centres, and stimulating radiative transitions at the silicon band edge.

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