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Fast digital electronics for application in dynamic force microscopy using high-Q cantilevers

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Abstract. One way to improve imaging in dynamic force microscopy is to increase the cantilever resonance frequency. Higher frequencies require faster electronics. This work presents fast new digital electronics based on the principle of phase-locked loop techniques. First results show very high frequency resolution and very stable imaging.

With the method of dynamic force microscopy [1, 2] true atomic resolution is now routinely obtained in ultra-high vacuum (UHV). This technique uses a cantilever with spring constant c, oscillating with constant amplitude A_0. The resonance frequency f_0 of the cantilever is determined by the lever's physical properties and by the interaction between the cantilever tip and the sample surface.

The goal of the electronics is to drive the cantilever at its resonance frequency f_0 with constant amplitude A_0 and to measure the frequency shift Δf of the cantilever induced by the force interaction. Many methods are used to determine the Δf of the oscillating cantilever and to control the distance between tip and sample. The most common method is the FM detection first applied to dynamic force microscopy by Albrecht et al. [3].

As shown by Lüthi et al. [4] it is important to move the tip in a so-called near contact regime to obtain true atomic resolution. In this regime the force gradient can become very high and therefore stiff cantilevers must be used to prevent jump into contact. This fact and the wish to increase sensitivity lead to stiffer and smaller cantilevers that have higher f_0, which allows faster scanning. This is why we developed new fast digital electronics based on the principle of phase-locked loop (PLL) [5]. PLL is an established method for frequency demodulation because it works for very low signal-to-noise ratio. An analog PLL was used for a scanning tunneling microscopy (STM) with force detection by Dürig et al. [6].

In this work the performance of a fully digital frequency detector is discussed. The online communication with a digital signal processor (DSP) allows the implementation of intelligent feedback control algorithms like fuzzy controllers.

1 Theory

As the name of phase-locked loop implies, a PLL circuit keeps the phase between the cantilever and the reference oscillator locked. This is done by a feedback loop (described in Fig. 1), which compares the phases of the cantilever oscillation φ_c and the reference signal φ_r. The phase difference $\Delta\varphi$ is then fed back with a loop gain k_0 to adjust the phase of the reference oscillator to the same phase as the cantilever.

Different phase detectors are used in PLL circuits. In linear technology, the most common is a multiplier followed by a lowpass filter. Multiplying the cantilever signal $U_c = \hat{U}_c \sin(\omega_c t + \varphi_c)$ with the reference signal $U_r = \hat{U}_r \cos(\omega_r t + \varphi_r)$ gives the sum and the difference of the two frequencies ω_c and ω_r.

$$U_c U_r = \frac{\hat{U}_c \hat{U}_r}{2} \cdot \sin\Big((\omega_c - \omega_r)t + (\varphi_c - \varphi_r)\Big) + \sin\Big((\omega_c + \omega_r)t + (\varphi_c + \varphi_r)\Big). \quad (1)$$

With the lowpass filter the sum in (1) is cut off and the difference frequency is received. The filter also limits the bandwidth of the detector. In a locked PLL circuit ω_c and ω_r are

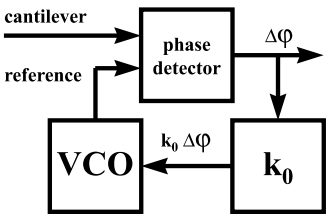

Fig. 1. Schematic of a PLL; VCO = voltage controlled oscillator

the same ($\omega_c - \omega_r = 0$). Therefore the multiplier followed by a lowpass filter extracts the phase difference $\Delta\varphi$ out of the two signals U_c and U_r:

$$U_c U_r = \underbrace{\frac{\hat{U}_c \hat{U}_r}{2}}_{K_d} \cdot \underbrace{\sin(\varphi_c - \varphi_r)}_{\sim\Delta\varphi} . \tag{2}$$

The amplitudes U_c and U_r are constant. For small changes of $\Delta\varphi$, (2) can be linearized with the phase detector replaced by a gain K_d:

$$U_c U_r \simeq K_d \Delta\varphi. \tag{3}$$

The voltage controlled oscillator (VCO) (see Fig. 1) calculates the output phase by integration of the input voltage $U_c(t)$. For the time-continuous theory the PLL can now be simplyfied by replacing the VCO by a integrator as shown in Fig. 2.

For the time discrete model this circuit is transformed by z transformation [7], which gives the circuit in Fig. 3. The phase transfer function of a digital PLL can now be calculated:

$$\frac{\phi_r(z)}{\phi_c(z)} = \frac{K_0 K_d F(z)\frac{z}{z-1}}{1 + K_0 K_d F(z)\frac{z}{z-1}}. \tag{4}$$

With the transfer function of (4) the phase response of the PLL circuit to a phase step of the input signal can be calculated. This calculations are made with $F(z)$ as a 3-kHz first-order lowpass filter. The calculated phase response in Fig. 4 shows that the PLL needs less than 1 ms to adjust its phase to the input signal phase step. This is quite sufficient for conventional data aquisition with a scanning probe microscope (SPM). The measured phase response in Fig. 5 confirmed the calculated properties of the PLL.

The hardware, of course, contains much more than the PLL. The electronics shown in Fig. 6 consists of a 20 MHz digital board with the frequency detector (PLL) and the cantilever excitation part [8]. The cantilever exciter uses the reference frequency ω_r of the NCO. A phase shifter optimizes the phase between the exciting signal and the cantilever. The amplitude of the excitation is set by an amplitude controller. This home-built hardware is linked with a digital signal processor (DSP). On the DSP board we programmed feedback controllers for the z distance and the oscillation amplitude A_0. For a constant frequency shift image, the software controller on the DSP reads Δf and sets the z piezo to keep Δf constant. The amplitude controller reads the root mean square to

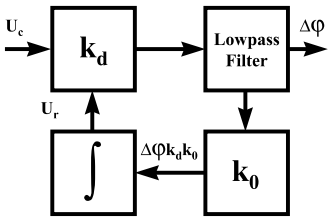

Fig. 2. Simplified circuit of a PLL, VCO replaced by an integrator

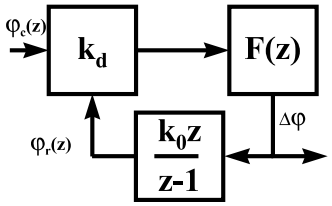

Fig. 3. Discrete-time representation of PLL, $F(z)$ is the lowpass filter transfer function

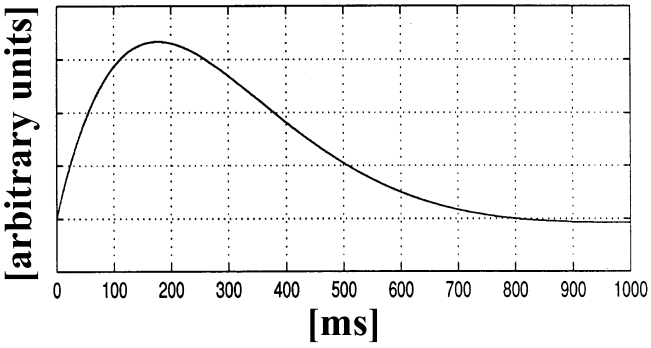

Fig. 4. Calculated phase response resulting from a phase step at the input

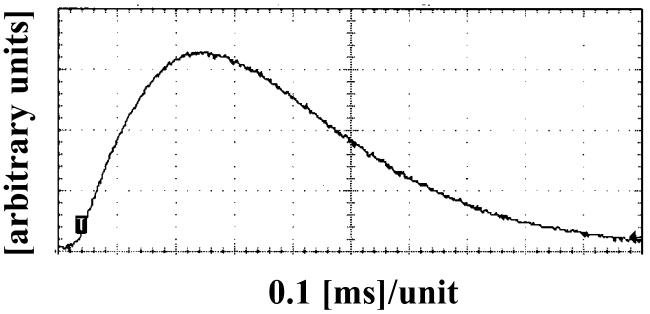

Fig. 5. Measured phase response resulting from a phase step at the input

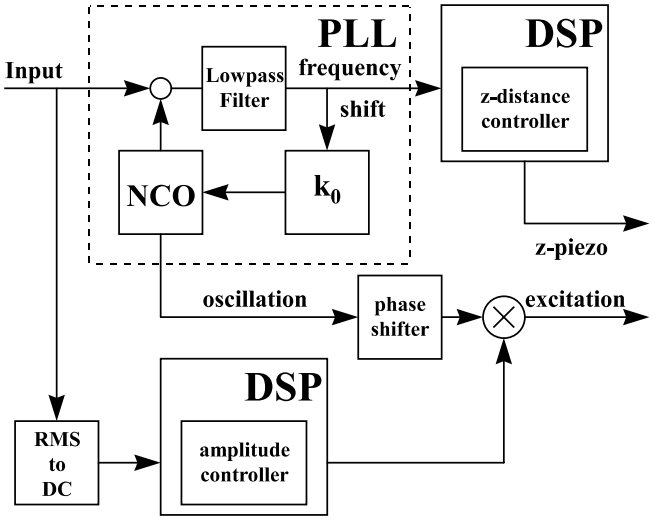

Fig. 6. Schematic of digital electronics. A software controller on the DSP controls the tip-to-sample distance by setting the z piezo. A second controller controls the cantilever oscillation by adjusting the excitation amplitude. A phase shifter optimizes the phase between cantilever and excitation signal

DC (RMS to DC) value of A_0. A feedback controller sets the excitation amplitude to a value that keeps A_0 constant.

2 Experimental

The frequency resolution limit was tested by feeding a frequency modulated signal into the PLL. A signal generator [9] was used to modulate the 280-kHz frequency by a sinusoidal signal with a rate of 100 Hz and a span of 5 mHz. The bandwidth of the PLL was set to 500 Hz by the lowpass filter (see Fig. 6). Figure 7 shows the output of the PLL that results from modulating the input signal.

The attained resolution of 5 mHz is excellent. A big advantage of the digital implementation is that there is no thermal frequency drift.

Experiments using our home-built scanning probe microscop (SPM) [10] were made under UHV conditions. In a first measurement on Si(111)7x7 the new detector tracked Δf while the z controller kept the time averaged tunneling current I_t constant. Figure Fig. 8 shows the frequency shift image with true atomic resolution [11] detected with the PLL.

The frequency demodulation part of the electronics has proved to be very stable. Therefore we could now apply the complete digital electronics to measure the surface of the insulator RbBr(001). In this case the new electronics keep the oscillation amplitude A_0 constant while detecting Δf and using this value to control the tip-to-sample distance. Figure 9 shows the topography image on the insulator RbBr(001).

The whole hardware proved very stable and true atomic resolution could be obtained, in particular along kinked monosteps.

3 Conclusion

In dynamic force microscopy, many advantages are gained by measuring at higher f_0. The new digital electronics presented in this paper is faster, has less thermal frequency drifts and shows better frequency resolution than conventional analog frequency detectors. The combination of this hardware with the DSP provides high flexibility and allows software implementation of intelligent feedback controllers. For future imaging with dynamic force microscopy it opens the door on heterogenious materials.

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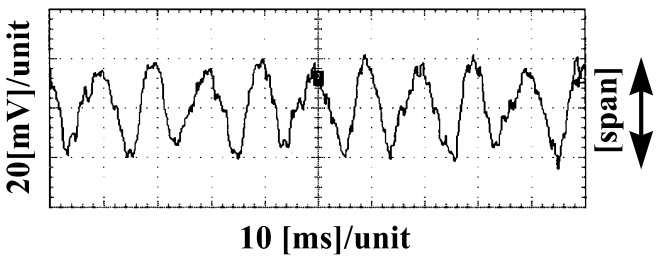

Fig. 7. Response of PLL with bandwidth set to 500 Hz to a 280-kHz input signal modulated with a sinusoidal rate of 100 Hz and span of 5 mHz

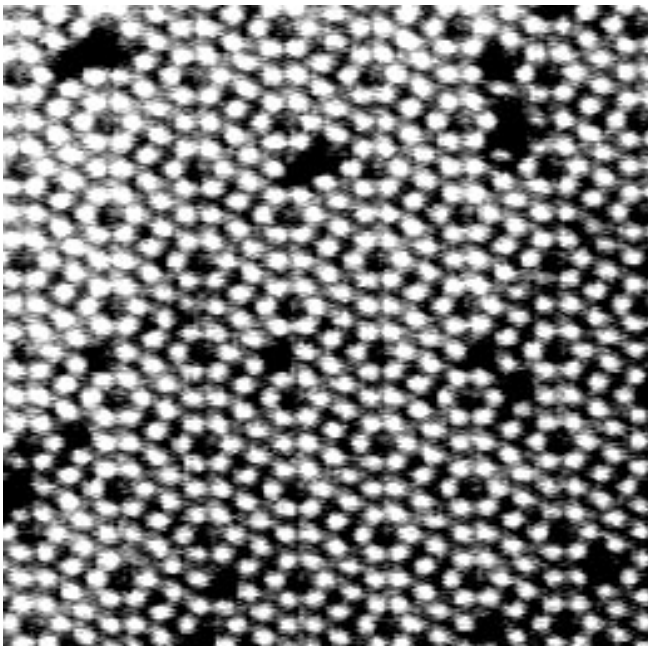

Fig. 8. Frequency shift on Si(111)7×7 detected with PLL, mean $I_t = 40$ pA controlled, $U_{\text{bias}} = 2.05$ V, $f_0 = 156$ kHz, corrugation $= 0.75$ Hz

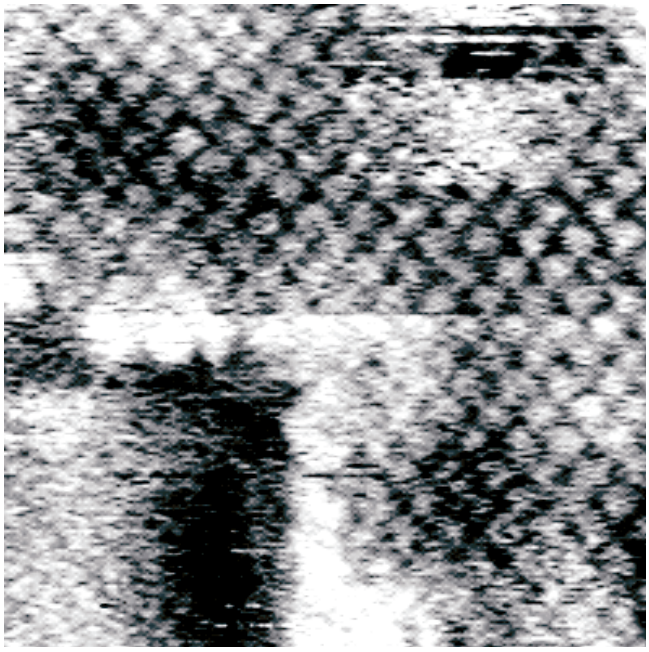

Fig. 9. Topography on RbBr(001) measured with digital electronics, constant $\Delta f = -32$ Hz was controlled, $U_{bias} = 0$ V, $f_0 = 280$ kHz

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