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Performance analysis of ITCs on analog/RF, linearity and reliability performance metrics of tunnel FET with ultra-thin source region

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Abstract
The generation and accumulation of trap charges at oxide-semiconductor contact is a crucial point to consider since it affects device performance and reliability. This paper aimed to provide a comprehensive assessment of interface trap charges on the characteristics of a ultra-thin source region-based F-shaped Tunnel FET (UTS-F-TFET) with theoretical and numerical calculation of important frequency and linearity parameters. Comparative research is carried out to opt for the best lower bandgap material for source region to optimize the analog functionality of UTS-F-TFET. With a steeper subthreshold slope, the UTS-F-TFET has increased current carrying capabilities and reduced ambipolar behavior. This research aims to investigate the impact of ITCs on DC characteristics (Thermal equilibrium state, ON and OFF state) and analog/RF performance of the simulated device. Moreover, the consequence of ITCs on linearity figure of merits with reliability consideration is also investigated. As per this investigation, the proposed TFET structure exhibited minimal distortion in linearity metrics with negligible influence of ITCs. As a result, the proposed UTS-F-TFET is compatible with ultra-low power high-frequency operations with minimum distortion.

Keywords Ultra-thin source · Band-to-band tunneling (B2BT) · Interface trap charges (ITCs) · Linearity · Reliability · Source/channel interface (SCi) · Drain/ channel interface (DCi) · Ambipolar current

1 Introduction

Device performance, power consumption, and reliability are crucial challenging concerns to resolve, according to the current rapid growth of the semiconductor industry. Moore's law is pursued to reduce power consumption and enhance device performance, resulting in reducing semiconductor device size. Billions of transistors are now integrated on single chip/microprocessors for compact size with improved device performance. But, Several fabrication challenges arise as semiconductor devices are downsized to accomplish a miniaturized criterion of ICs with the same functionality [1]. As a result, MOSFETs have been downscaled to improve device functionality in power consumption, switching speed, and package density per unit area with lower fabrication costs. Some adverse effects have been observed due to MOSFET downscaling due to an undesirable increase in leakage current. At room temperature, increased leakage current causes significant consequences like short circuit effect (SCEs), mobility degradation, impact ionization, Drain induced barrier lowing (DIBL), Hot carrier effects (HCEs), and static power consumption. Furthermore, because of the direct dependence on the thermal constant (kT/q), MOSFETs limit the subthreshold slope (SS) to 60 mV/decades [2, 3].

The tunnel field-effect transistor (TFET) shows very promising behavior to overcomes the aforementioned limitation of MOSFET. It offers steeper SS (high switching speed) compared to MOSFET, and it performs better in low-power applications with a lower threshold voltage (V_{th}) [4, 5]. TFET works on phenomena of quantum tunneling of charge carrier from source to channel, which helps to achieve steeper switching characteristics and reduced V_{th} [6]. Apart from these advantages, it also suffers from several limitations such as low current driving capability and ambipolar current behavior that degrades the device analog/RF performance [7, 8]. To overcome these limitations of

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conventional TFET, various techniques are introduced, such as gate and drain engineering, dielectric material variation, doping type and variation, material (hetero materials) engineering with structural modification, and many more.

To figure out the limitations of conventional TFET, a new structure with ultra-thin source region and reduced drain channel interface-based TFET (UTS-F-TFET) is proposed and investigated in previous work [9, 10]. Because of complete insertion of ultra-thin source region into the channel region, low V_{th} and high ON-state current (I_{on}) are achieved with steeper SS. Furthermore, to reducing V_{th} and increase current driving capability, some lower bandgap materials are used in source region of UTS-F-TFET [11]. This will justify with the help of simulation on SILVACO TCAD tool with incorporating important models and numerical methods.

ITCs accumulate at the semiconductor/oxide interface throughout the manufacturing process due to the oxidation process, stress occurs due to high temperature/hot carrier, and damage sustained during the fabrication steps. The traps are usually divided into donor trap charges (DTCs) and acceptor trap charges (ATCs). DTCs reside above the valance band and behave like positive ITCs (P-ITCs) by donating an electron. Another side, ATCs reside below the conduction band and acts like negative ITCs (N-ITCs) by accepting an electron to fill the empty state within the $Si–SiO_2$ interface region [12, 13]. These ITCs accumulate in TFETs due to a large electric field at the tunneling junction, which excites the silicon body surface, causing the electric field variation at the source/channel junction (SC-junction). As we know, the tunneling probability and drain current is proportional to the electric field at the tunneling junction of device, resulting in the deviation in current-carrying potentiality of device [14]. As a result, determining the impact of trap charges on device performance characteristics is crucial. This considerable impact of ITCs on device performance was investigated with the help of analyzing the analogue and linearity parameters with respective mathematical equations.

2 Device schematic and parameters

The 2D schematic of the proposed UTS-F-TFET device is illustrated in Fig. 1. The proposed device consists of a single gate with an ultra thin, highly doped source region that is entirely bounded by the intrinsic channel region. On the other hand, drain region of device is attached to the outside of the channel. Because of this, DCi is reduced and device looks like an L-shaped. The optimized physical parameters of UTS-F-TFET such as Gate oxide thickness (t_{ox}), Thickness above and below source (t_{cu}), Channel thickness at bottom of device ($t_{cb} = t_d + t_{ox}$), Lateral tunneling length (L_t),

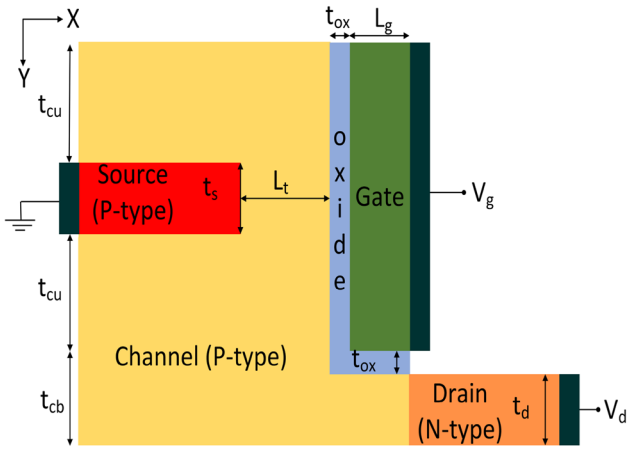

Fig. 1 2D cross-sectional view of UTS-F-TFET

Source thickness (t_s), Channel thickness ($2t_{cu} + t_{cb} + t_s$), Drain thickness (t_d) are 1, 16, 6, 4, 3, 35 and 5 nm, respectively. For simulated UTS-F-TFET, Drain doping concentration (N_D), Channel doping concentration (N_C), source doping concentration (N_S), and gate work function (WF_G) are 5×10^{18} cm^{-3}, 1×10^{15} cm^{-3}, 2×10^{20}, and 4.5 eV, respectively.

To ensure the model accuracy used during simulation, Experimental data of doped L-shaped tunnel FET (L-TFET) (Ref. [15]) have been used to calibrate the proposed device. With the same physical dimensions and materials of doped L-TFET, calibration is carried out. The simulation results authenticate with experimental data as depicted in Fig. 2a. In this work, the proposed structure is modeled using the same analytical/physical models used in Ref. [15].

For simulation purposes, the following models are incorporated: - Non-local Band to Band Tunneling Model (BTBT), Band Gap Narrowing Model (BGN), FERMI, Auger Recombination Model (Auger), Mobility Models (FLDMOB, CONMOB and SRH), Trap-Assisted Tunneling Model (TAT) etc. Along with these models, Newton's numerical method was used to provide strong coupling between the resultant equations for better convergence of current [16]. A brief description of used models are mentioned in Table 1.

3 Optimization of source material

The optimal solution of the reduced I_{on} problem in the proposed TFET is to employ a lower bandgap material for the source region. Because of this, tunneling barrier width at SCi getting reduced and helps to increased the tunneling

probability, which reflect in terms of increased I_{on}. At T = 300 K, some widely used lower bandgap materials are InAs (E_g = 0.35 eV), InGaAs (E_g = 0.57 eV) and Si–Ge (E_g = 0.68 eV) are used as source material in place of silicon (E_g = 1.11 eV) with SiO_2 as effective gate oxide. From all the above materials, Si–Ge has the higher effective density of states at the band edges ($1.92 \times 10^{19} cm^{-3}$). Because of this, higher no. of electron tunnel from source to channel and recombine at SCi. So, the UTS-F-TFET with Si-Ge as source material has increased I_{on} when compared to the other materials used in source, as depicted in Fig. 2b.

4 DC performance analysis

4.1 Thermal equilibrium state

This section enlightens the effect of ITCs on the functioning of UTS-F-TFET under the thermal equilibrium condition (V_{ds} = 0 V and V_{gs} = 0 V). For this, we analyzed the charge carrier concentration (C_{conc}) on both the interfaces (SCi and DCi) which are shown in Figs. 3 and 4, respectively. Figure 3a reveals that Negative ITC (N-ITC) helps to increase the the electron C_{conc} and opposite effect can be seen for the hole C_{conc} (in Fig. 3b) near the SCi. Another side, electron

Table 1 Descriptions of SILVACO models

S. no.	Models	Description
1.	Non-local BTBT	High field, direct transitions of carriers
2.	BGN	High doping, bipolar gain (klaassen Model)
3.	Ni.Fermi	High doping, low carrier concentration
4.	Auger	Carrier transition, (for captured or emitted)
5.	FLDMOB	For velocity (mobility) saturation
6.	CONMOB	Simple power law, temperature dependency
7.	SRH	For fixed lifetime of minority carriers
8.	TAT	Modify SRH model, tunnel via trap states

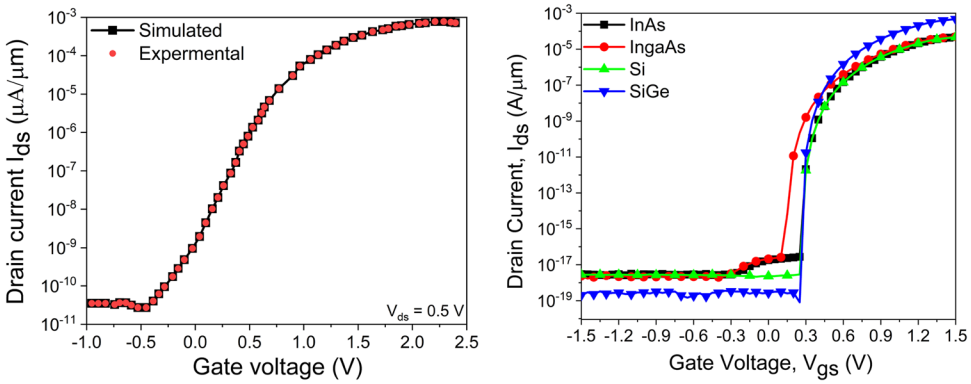

Fig. 2 Thermal equilibrium **a** calibration curve for Ref. [15] and **b** $I_{ds} - V_{gs}$ data plot for different materials

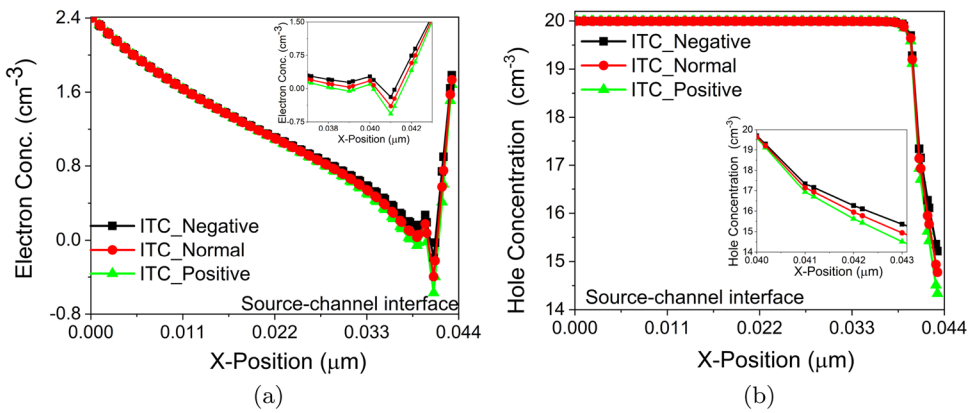

Fig. 3 Thermal equilibrium **a** Electron and **b** Hole C_{conc} at SCi junction

C_{conc} increases and hole C_{conc} decreases with Positive ITC (P-ITC) at DCi (Fig. 4a and b).

4.2 ON-state condition

The carrier concentration of UTS-F-TFET is shown in Figs. 5 and 6, along *X*-position for both interfaces. In TFET, mainly SCi and DCi junction affect the device characteristics. Hence, the ITCs impact on both interface w.r.t carrier concentrations of electron and holes has been investigated. From Fig. 5a, we can analyse that the electron concentration profile near the Si-SiO_2 interface falls (rise) for N-ITCs (P-ITCs) concerning the without ITC impact. The opposite impact can be seen for the hole concentration profile at Si–SiO_2 interface in Fig. 5b. Another side, the impact of ITCs is just opposite for the DCi junction because donor trap (P-ITCs) occupied the empty state and helps to increase the donor concentration profile (Electron conc.) in the drain region (Fig. 6a). Same

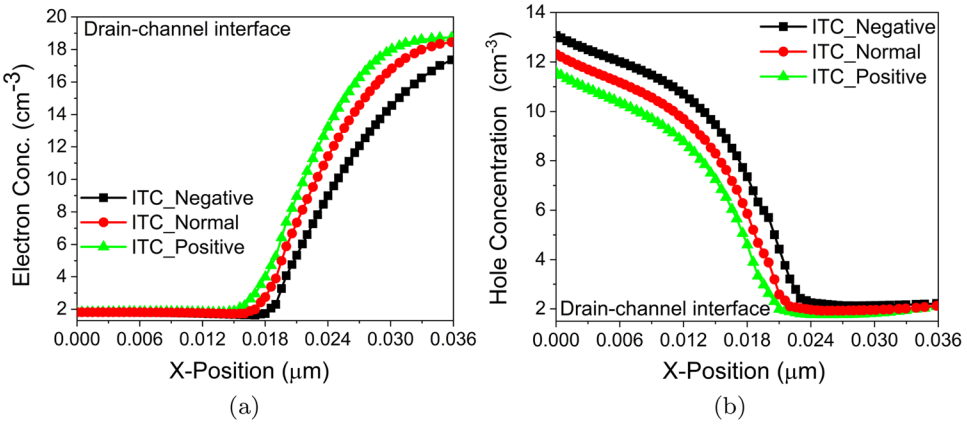

Fig. 4 Thermal equilibrium **a** Electron and **b** Hole C_{conc} at DCi junction

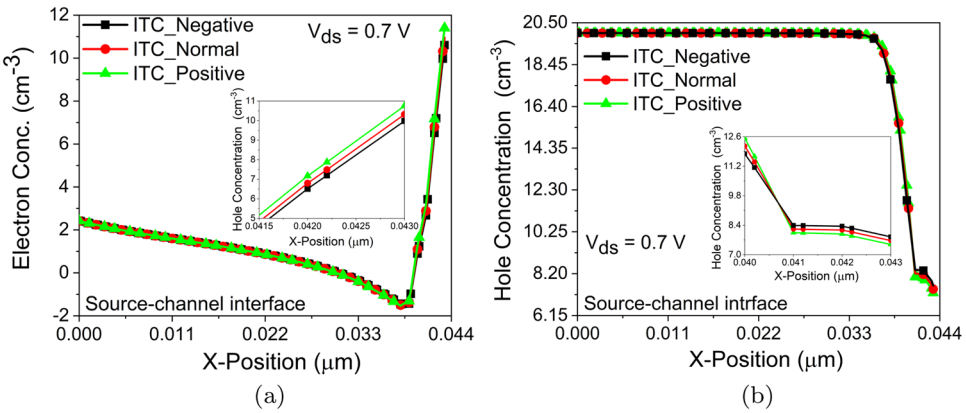

Fig. 5 ON-state **a** Electron and **b** Hole C_{conc} at SCi junction

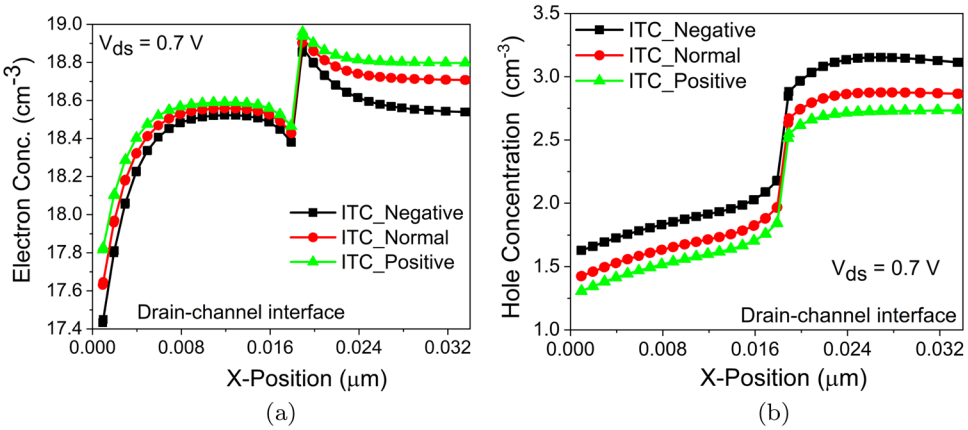

Fig. 6 ON-state **a** Electron and **b** Hole C_{conc} at DCi junction

way, P-ITCs helps to decrease the hole carrier concentration in drain region (Fig. 6b). The reduction in hole concentration is beneficial to reduce the ambipolar conduction because I_{ambi} is mainly contributed by the holes present in the region that recombine with an electron at DCi. From Fig. 7a and b, V_{th} (0.3 V) and I_{on} ($9.12 \times 10^{-4} A/\mu m$)is improved with P-ITCs when compared to without ITCs effect.

4.3 OFF-current analysis

This part discusses the impact of ITCs and Temperature (T) at both interfaces (SCi and DCi). The OFF-state condition mainly governs by the DCi junction because the OFF-current (I_{off}) is affected by the recombination at DCi. T and ITCs have a significant impact on reliability-related issues of UTS-F-TFET for circuit-level applications because both of them considerably affect the I_{on}/I_{off} ratio [17, 18]. The higher value of I_{on}/I_{off} ratio leads to high switching speed. So. an extensive investigation is carried out on UTS-F-TFET for OFF-state conditions. For this, the impact of ITCS, along with models and T variation, was carefully investigated to extract the optimum type of ITCs with T range and models. To examine the effect of ITCs and T on I_{off}, we used BTBT, SRH and TAT throughout the simulation process.

$$T(E) \propto \exp\left[-\frac{4\sqrt{2m^*}E_g^{*3/2}}{3h|e|(E_g^* + \Delta\varphi)}\sqrt{\frac{\epsilon_{si}t_{ox}t_{si}}{\epsilon_{ox}}}\right]\Delta\varphi \quad (1)$$

The consequence of BTBT model on I_{off}, were examined with the help of Eq. 1. From Eq. 1, it is seen that the BTBT mainly depends on electric field ($E = E_g^* + \Delta\varphi$), body thickness ($t_{si}$), dielectric constant of material and oxide (ϵ_{si} and ϵ_{ox}) and band gap of material (E_g^*). The BTBT models controlling the I_{on} under the high E-field and show less sensitivity towards the T variations.

By using Eq. 2, we investigate the impact of the SRH model on proposed devices for T variation (250–400 K). Constant carrier lifetimes [TAUP0 (for hole) and TAUN0 (for electron)] are used in SRH recombination model with dependency on temperature (T_L term in Eq. 2) and trap energy level (E_{TRAP}), which indicates that T variation significantly affects the OFF-state conduction with the SRH model. Similarly, from Eq. 3, TAT model also shows considerable impact on I_{off} because it depends on field-dependent functions (Γ_n^{DIRAC} and Γ_p^{DIRAC}) and all that factor which influence SRH model [19–21].

In this proposed device, we get the electric field crowding effect near the corner of source–channel interface, which helps to increase the tunneling rate at SCi. Because of this, higher I_{ds} can be obtained, as mentioned earlier in this work. So, the impact of ITCs on E-field must be investigated. The E-field deviation in the direction of channel region is illustrated in Fig. 8 for different ITCS. The E-field at both junctions (SCi and DCi) can be affected by the ITCs [22]. At SCi junction, higher E-field is achieved in comparison to DCi junction, because of this I_{ambi} is very low in proposed

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUP0\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + TAUN0\left[p + n_{ie}exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (2)$$

$$R_{TAT} = \frac{pn - n_{ie}^2}{\frac{TAUP0}{1+\Gamma_p^{DIRAC}}\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \frac{TAUN0}{1+\Gamma_n^{DIRAC}}\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (3)$$

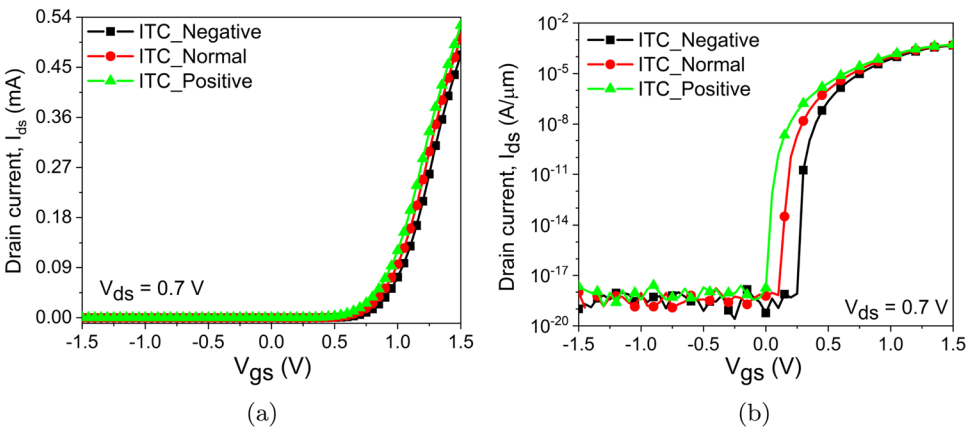

Fig. 7 $I_{ds} - V_{gs}$ data plot **a** linear scale and **b** Semi-log scale for different ITCs

device. From Fig. 8a, the highest E-field at SCi is allocated for the P-ITCs because P-ITCs helps to improve the band bending near the SCi. Similarly, the minimum E-field at DCi is achieved for N-ITCs because of the reduced band bending at DCi with an application of N-ITCs, as depicted in Fig. 8b.

The potential follows the same trend as the E-field, implying that P-ITCs lead to a rise in potential and N-ITCs lead to a drop in potential, as showing in Fig. 9a and b for the SCi and DCi junctions, respectively. For SCi, the deviation in potential is almost negligible for various ITCs compared with potential at DCi junction.

The total charge carrier density is constant at thermal equilibrium conditions because the recombination and generation rate rates are equivalent. But, when the external voltage is applied along with ITCs consideration, the generation of charge carrier increases because of this mobility saturation occurs [23]. Due to this, the recombination rate at both interfaces decrease for P-ITCs, as portrayed in Fig. 10. At DCi, deviation in recombination rate for N-ITCs

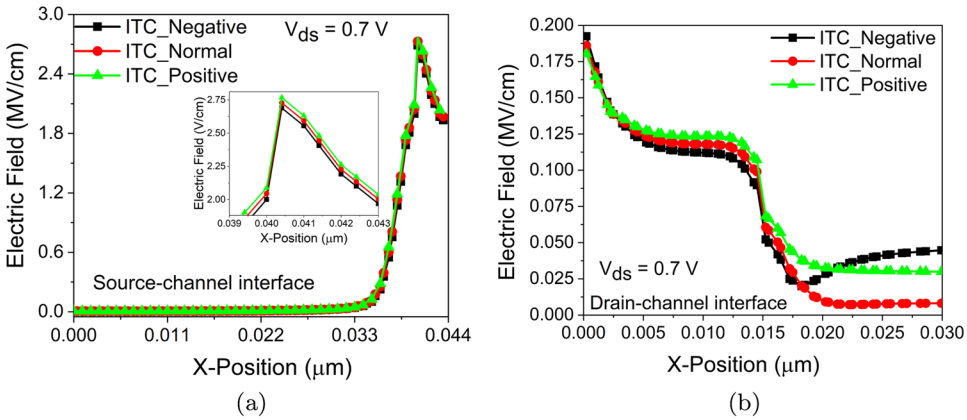

Fig. 8 Electric field strength at **a** SCi and **b** DCi of proposed device

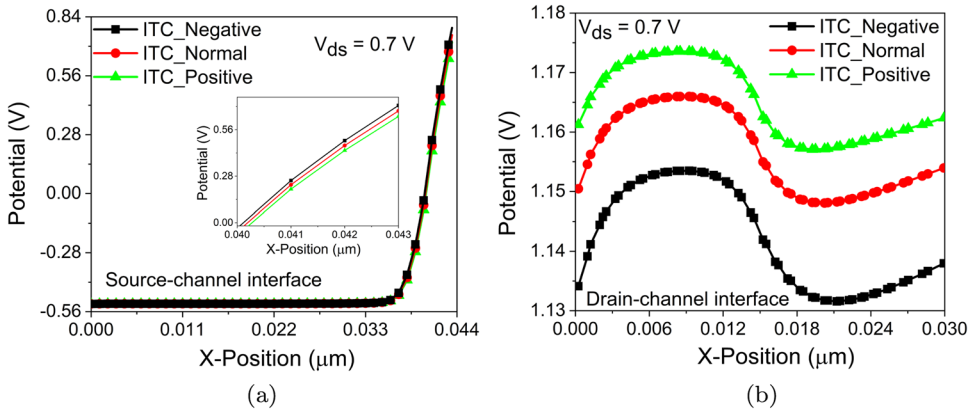

Fig. 9 Potential variation at **a** SCi and **b** DCi of proposed device

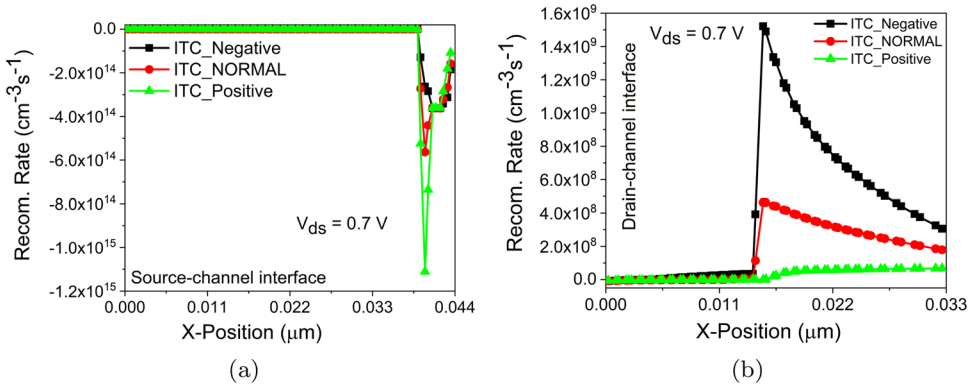

Fig. 10 Recombination rate at **a** SCi and **b** DCi of proposed device

is significantly very high as compared to Without ITCs (Fig. 10b) because N-ITCs generate more hole carriers at DCi, which recombine with the majority charge carrier (electron) present in drain region.

The significant deviations in E-field, potential and recombination rate at DCi affects the OFF-state behaviour of proposed device for various ITCs, models and temperature (250–400 K). For lower V_{gs}, TAT and SRH models become more prominent when V_{gs} decreases. When V_{gs} is very low, the potential barrier at DCi junction is getting reduced and enables the BTBT phenomenon. So, the charge carriers start tunneling across the present potential barrier. The current component of BTBT, BTBT + SRH and BTBT + SRH + TAT have their region of subjection depending upon the E-field at SCi and DCi junctions [24]. From Eq. 1, under high E-field, the BTBT model dominates the I_{ds} value and is less sensitive to T variation and different types of ITCs, as shown in Fig. 11. SRH and TAT models have seemed at lower E-field and try to increase the I_{ds} value with showing strong sensitivity to changes in ITCs and T. From Fig. 11a, the variation in I_{ambi} from 10^{-19} to 10^{-14} A/μm (10^5 time) for T variation under without ITCs consideration and with application of BTBT model. However, $I_{ambi} = 10^{-18}$ and 10^{-15} for the SRH and TAT models, it rises when T increases. A similar effect for N-ITCs and P-ITCs can be seen for the I_{ambi} when T varies from 250 to 400 K with different models (BTBT, SRH and TAT), illustrated in Fig. 11b and c, respectively. Consequently, at lower T, the SRH and TAT implications are relatively low, and the BTBT resurfaces as a significant and effective tunneling mechanism with reduced sensitivity to T variation and ITCs.

5 Impact on analog/RF parameter

In the circuit level assessment of the device, the radio frequency (RF) statistics are quite important. The parasitic capacitances (C_{gd} and C_{gs}) are investigated in this regard and depicted by Fig. 12a and b of UTS-F-TFET for different ITCs w.r.t V_{gs}. From Fig. 12a, it is seen C_{gd} increases with increasing V_{gs} because increment in V_{gs} leads to the reduction in potential barrier between channel and drain [25, 26].The significant increase in C_{gd} with P-ITCs is due to the same phenomena, i.e., P-ITCs minimize the potential barrier between channel and drain as compared to without ITCs consideration. N-ITCs have the opposite phenomenon, resulting in a decrease in C_{gd}. From Fig. 12b, it is seen that the deviation in C_{gs} is less for ITCs. The C_{gs} is decreased with increasing V_{gs} because the potential

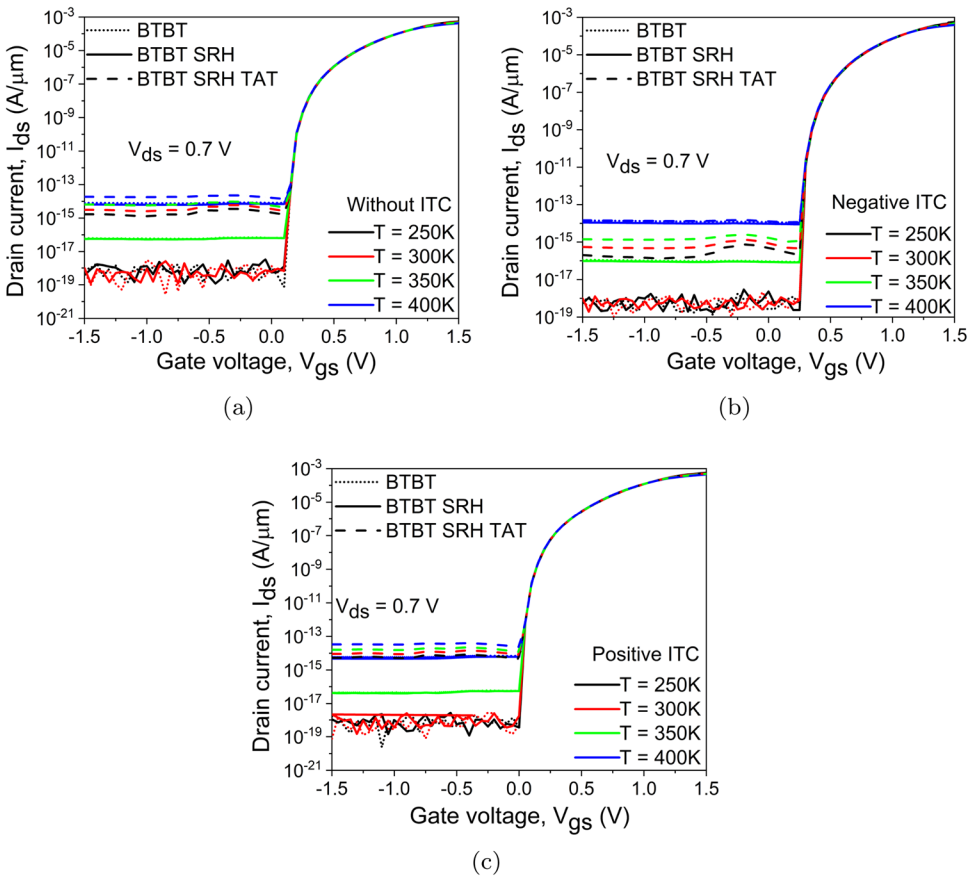

Fig. 11 I_{ds}-V_{gs} graph to analyze the impact of model under different T values for **a** Without ITC **b** Negative ITC and **b** Positive ITC

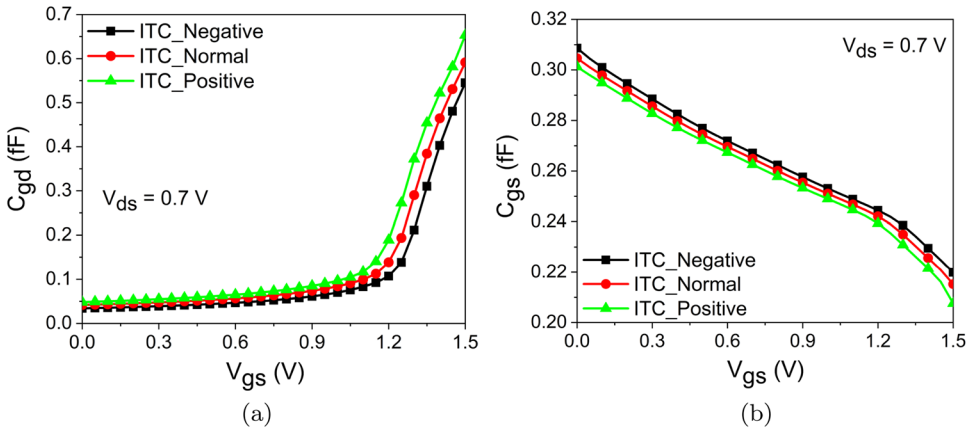

Fig. 12 The variation of parasitic capacitance **a** C_{gd} and **b** C_{gs} for different ITCs

barrier between gate and source decreases for high V_{gs} and the coupling between gate and channel is improved. C_{gs} is decreased (Increases) with P-ITCs (N-ITCs) as shown in Fig. 12b.

Transconductance (g_m) is crucial in analogue applications because it affects the intrinsic gain of device and relates the input voltage across the device and output current [27], given as

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{4}$$

When designing analog circuits, g_m is quite important. Figure 13a depicts the variation in g_m with V_{gs} for the different ITCs. The P-ITCs have a rising impact on g_m because of improving tunneling rate at SCi, and N-ITCs have a decreasing impact due to the reduced tunneling rate. The N-ITCs and P-ITCs lead to a decrease and increase in g_m by 23.46% and 33.76%, respectively.

The cut-off frequency (f_t) is another crucial design factor for the high-speed RF devices, at which input current becomes equal to short circuit output current [25]. The mathematical expression of f_t given by Eq. 5 and the impact of different ITCs on f_t for UTS-F-TFET is shown in Fig. 13b.

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{5}$$

For higher V_{gs}, f_t mainly depends on g_m and C_{gd} because both are dominating factors as compared to the C_{gs} (very less value). P-ITCs cause an increase in g_m, as previously stated, and consequently an increase in f_t when compared to without ITCs. On the other hand, N-ITCs exhibit the opposite phenomenon, i.e., f_t decreases with N-ITCs. For the proposed device, the N-ITCs and P-ITCs decrease and increase the f_t by 3.23% and 1.97%, respectively. Thus, proving that the F-shaped ultra-thin source design is much more immune to the effect of ITCs.

To analyze the device response time and delay, another critical parameter, transit time (TT), comes into the picture, and its mathematical expression is given by Eq. 6. f_t and TT are inversely proportional to each other, i.e., for higher f_t, we get a lower value of TT. The speed of UTS-F-TFET increases with P-ITCs because the f_t value significantly increases with the effect of P-ITCs, as shown in Fig. 14a.

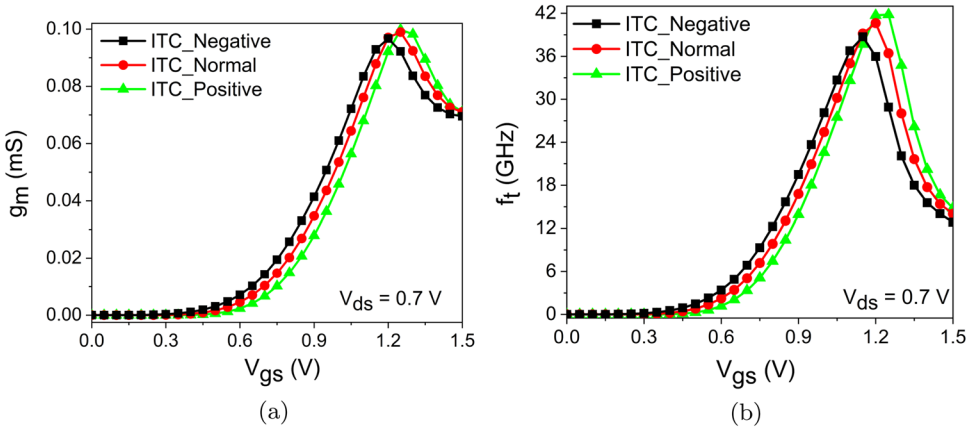

Fig. 13 The data plot of **a** g_m and **b** f_t for different ITCs

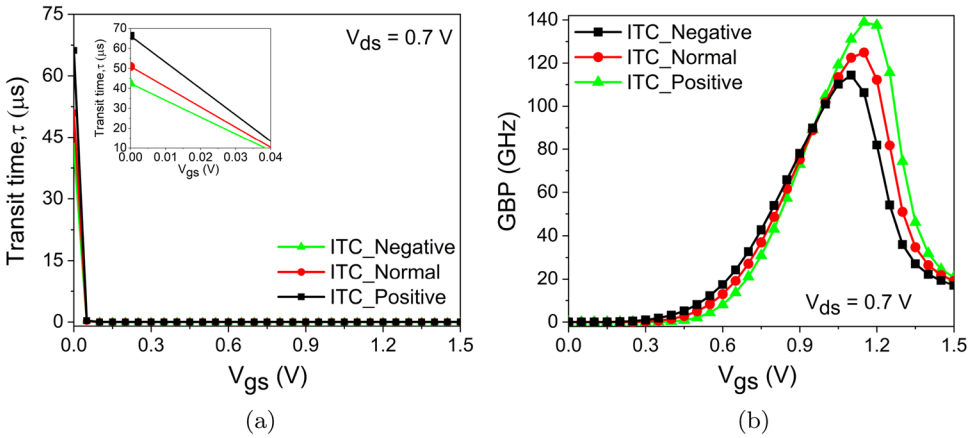

Fig. 14 The graph of **a** Transit time and **b** GBP to examine the impact of ITCs

For N-ITCs, TT is increased as f_t increases, which is not desirable for high speed and low response time.

$$\mathrm{TT} = \frac{1}{2\pi f_{\mathrm{T}}} \tag{6}$$

Figure 14b shows the consequence of different types of ITCs on the Gain bandwidth product (GBP), which is defined as the product of bandwidth of device and the gain at which the bandwidth is measured [25, 28]. It is given by Eq. 7as follows:

$$\mathrm{GBP} = \frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{gd}}} \tag{7}$$

From Eq. 7, we can say that GBP is directly proportional to $g_{\mathrm{m}}/C_{\mathrm{gd}}$. The g_{m} and C_{gd} both increase with P-ITCs, but g_{m} is very high so GBP improves with P-ITCs and deteriorate with N-ITCs. The percentage deviation of variation in GBP for P-ITC and N-ITCs is 2.56% (Increase) and 2.31% (Decrease), respectively.

Equations 8 and 9 represent the mathematical formulation of Transconductance frequency product (TFP) and Transconductance generation factor (TGF), which are the key parameters to determine the device efficiency and off-set between power dissipation and operating bandwidth [29]. The impact of different ITCs on TFP and TGF is illustrated in Fig. 15a and b, respectively. Figure 15b demonstrates that TFP rises linearly before the starting of the inversion phase, then attains its maximum value and subsequently decreases for increasing gate bias levels, which is due to mobility degradation. Along with this, an application of P-ITCs leads to a reduction of the maximum peak of TFP compared to N-ITCs (maximum value for TFP). Similarly, the impact of different ITCs on TGF is delineated in Fig. 15a. From Eq. 9, TGF is directly proportional to TFP. Hence the maximum peak of TGF is achieved for N-ITCs, and a lower peak is attained for P-ITCs because of mobility reduction of charge carriers.

$$\mathrm{TFP} = \frac{g_{\mathrm{m}} f_{\mathrm{T}}}{I_{\mathrm{d}}} \tag{8}$$

$$\mathrm{TGF} = \frac{g_{\mathrm{m}}}{I_{\mathrm{d}}} = \frac{TFP}{f_{\mathrm{T}}} \tag{9}$$

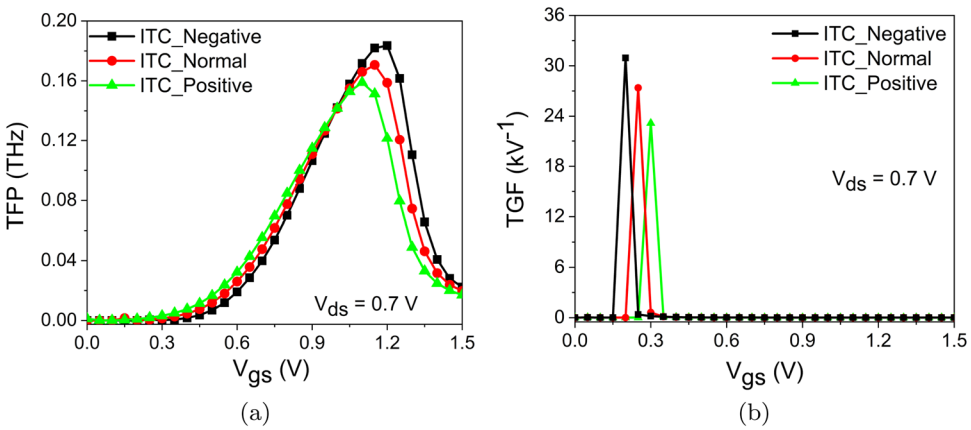

Fig. 15 The variation of **a** TFP and **b** TGF with respect to V_{gs} for ITCs

6 Effect of ITCs on linearity performance

An enhanced I_{on}, high I_{on}/I_{off} ratio, low V_{th}, and lower value of SS with suppressed ambipolar conduction are not only critical characteristics to assess device behavior in the recent trend of device and circuit applications. In addition, for RF devices to be capable of interacting with today's modern communication systems, they must have a low signal-to-noise ratio as well as a fast speed. The device should also have linear properties so that the intended output signal is not severely impacted by nonlinear distortion. The device's linearity analysis is a different statistical process control phase in which the device is integrated in a circuit, and the linear relationship between input and output is examined [30, 31]. The Volterra series can be used to write any nonlinear power series in the following format:

$$V_{out} = a1V_{in} + a2V_{in}^2 + a3V_{in}^3 + \cdots \tag{10}$$

g_m must not significantly alter owing to a change in input voltage V_{gs} to validate linearity functionalities. However, the g_m of both MOSFETs and TFETs changes with the input voltage V_{gs}, resulting in nonlinear behavior for both devices. The various frequency components of the desired inter modulated (IMS) and harmonics signal are mentioned in Table 2. The harmonic distortion is given by the integral multiples of fundamental frequencies (f_1 and f_2), which can be eliminated because they are very far from the permissible range

Table 2 Non-linear frequency components

Components	Parameters	Frequencies
Actual signal	Fundamental	f_1, f_2
2nd order	HD2	$2f_1$, $2f_2$
	IM2	$f_1 \pm f_2$
3rd order	HD3	$3f_1$, $3f_2$
	IM3	$2f_1 \pm f_2$

[32]. Eqution 11 could be used to define the small-signal model (SSM) of output current (I_{ds}) in terms of non-linear g_m for V_{gs}.

$$I_{ds} = g_m V_{gs} + g_{m2} V_{gs}^2 + g_{m3} V_{gs}^3 + \cdots \tag{11}$$

As well as V_{gs} increase, I_{ds} increase with it, but after sometime I_{ds} become saturated because of mobility saturation of charge carrier. Thus, g_m starts decreasing after attaining the peak for higher V_{gs}. Therefore, a detailed investigation was carried out in this work to examine the impact of P-ITCs and N-ITCs for the proposed device.

From Eq. 11, to affirm the device linearity, the higher-order derivative of g_m should be as minimum as possible. The 2nd and 3rd order derivative of g_m (g_{m2} and g_{m3}) are calculated by using Eqs. 12 and 13, both of them affecting the device performance as they are accountable for harmonic distortion [27].

$$g_{m2} = \frac{\partial^2 I_d}{\partial^2 V_{gs}} \tag{12}$$

$$g_{m3} = \frac{\partial^3 I_d}{\partial^3 V_{gs}} \tag{13}$$

To maintain the linear characteristics of UTS-F-TFET, g_{m2} and g_{m3} should be very low because both are responsible for amplification distortion via signals for intermodulation distortions [31]. To define the optimal bias point for linear operation, zero cross over (ZC) point should be marked. The ZC-point locates the higher value of V_{gs} for which g_{m2} and g_{m3} become equal to zero. The impact of ITCs on g_{m2} and g_{m3} is illustrated in Fig. 16a and b, respectively. For the N-ITCs, values of g_{m2} and g_{m3} are minimum. Hence, N-ITCs helps to improve the linearity performance with suppressed 2nd and 3rd order harmonics of g_m.

The crucial intercept points are 2nd order voltage intercept point (VIP_2), 3rd order voltage intercept point (VIP_3)

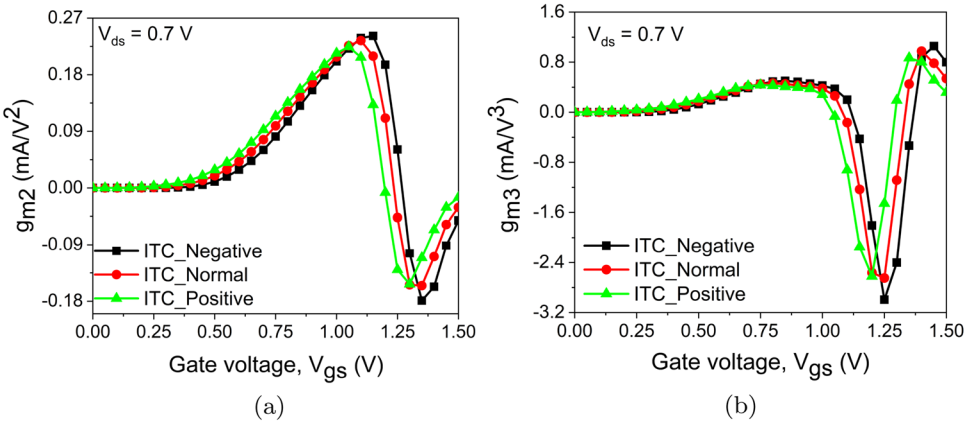

Fig. 16 The graph of **a** g_{m2} and **b** g_{m3} for different ITCs

and 3rd order input intercept point (IIP_3), these parameters should be high to exhibit distortion-less and linear characteristics of UTS-F-TFET. VIP_2 depicts the projected input voltage in which the 1st and 2nd order harmonic voltages are identical. Similarly, the VIP_3 exhibits the measured input voltage when the 1st and 3rd order harmonic voltages are equal, while the IIP_3 represents the estimated input power when the 1st and 3rd order harmonic powers are equal [33, 34].

From Fig. 17a, the peak of VIP_2 shifts towards the lower V_{gs} with the application of P-ITCs consideration, and opposite behavior can be seen for N-ITCs. But, VIP_2 attain the maximum peak for the N-ITCs. So, we can say that stronger linear properties can be achieved with higher V_{gs} and N-ITCs consideration.

$$\mathrm{VIP}_2 = 4\left(\frac{g_\mathrm{m}}{g_\mathrm{m2}}\right) \tag{14}$$

VIP_3 inversely proportional to the 3rd order derivative of g_m, as depicted in Eq. 15. To ensure the suppression of the third-order harmonic, we need a high value of VIP_3. As we previously discussed with Fig. 16b, g_{m3} reduces with P-ITCs. Hence VIP_3 is enhanced for P-ITCs with maximum peaks of 4.2 V (First peak) and 3.4 V (Second peak) with reducing V_{gs}, as shown in Fig. 17b.

$$\mathrm{VIP}_3 = \sqrt{24\left(\frac{g_\mathrm{m}}{g_\mathrm{m3}}\right)} \tag{15}$$

Relation between the product of g_{m3} R_s and IIP_3 is given by Eq. 16, where $R_s = 50\ \Omega$ for Radio Frequency applications. IIP_3 should be large for superior linearity performance since we require minimal g_{m3} and high g_m with a constant value of R_s [35]. Figure 17c exhibits the fluctuation of IIP_3 for various ITCs. IIP_3 improves with P-ITCs for lower V_{gs} (0.0–0.20 V), but its show asymmetric behavior towards ITCs variation for higher value of V_{gs} (0.75–1.5 V). The peak of IIP_3 achieved for the P-ITCs, thus best linearity performance of device can be achieved for P-ITCs.

$$\mathrm{IIP}_3 = \frac{2}{3}\left(\frac{g_\mathrm{m}}{g_\mathrm{m3}R_\mathrm{s}}\right) \tag{16}$$

The mathematical expression of IMD_3 and $1-$dB compression point ($1-$CP) is given by Eqs. 17 and 18, respectively. IMD_3 denotes the third-order intermodulation distortion,

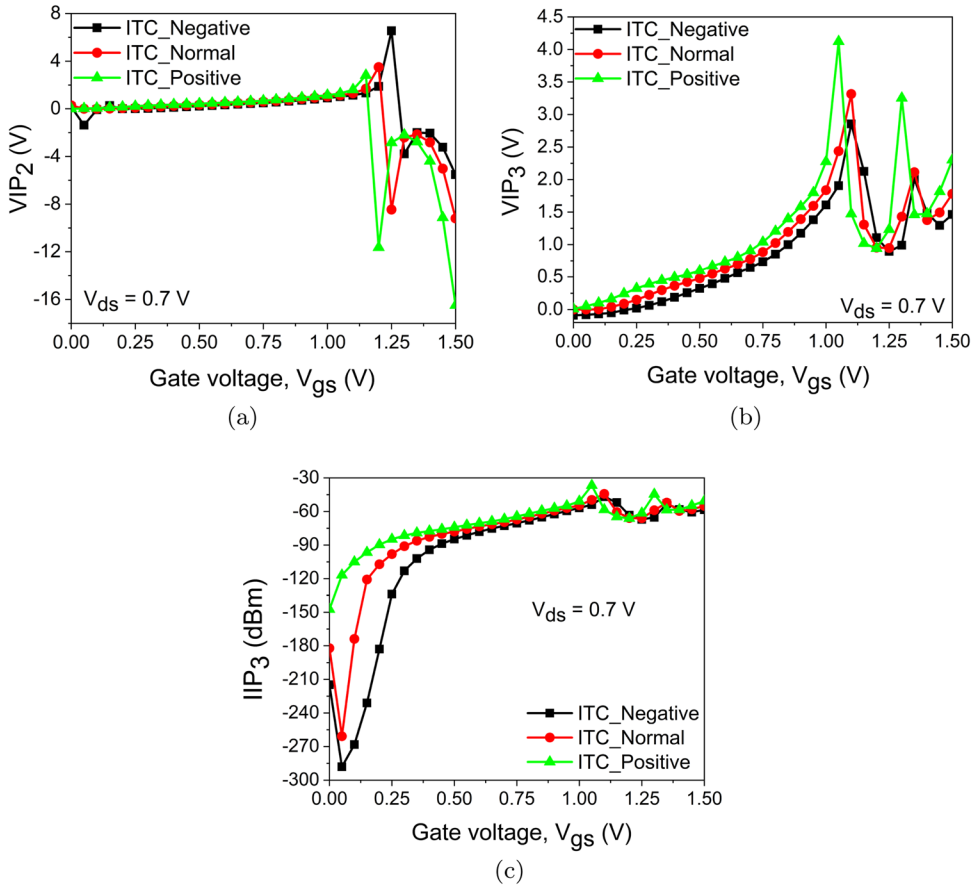

Fig. 17 The data plot of **a** VIP_2, **b** VIP_3 and **c** IIP_3 for different ITCs

which must be low amplitude to reduce the converse effect on one electrode (drain) to the second electrode (gate) when we apply voltages on both electrodes. Lower value of IMD_3 also helps to prevent the wastage of usable power [36]. From Fig. 18a, the IMD_3 level is up to 0 to − 20 dBm when the device is in saturation state (in ON-state) without the effect of ITCs impact. But, the minimum rage of IMD_3 (approx. − 700 dBm) is obtained when the device is yet to start for N-ITCs. For The P-ITCs, the minimal range of IMD_3 is approximately − 300 dBm, which may degrade the device performance.

$$\mathrm{IMD}_3 = \left[\frac{9}{2}(\mathrm{VIP}_3)^2 g_{\mathrm{m3}}\right]^2 R_{\mathrm{s}} \tag{17}$$

$$1\mathrm{dB\ compression\ point} = 0.22\sqrt{\frac{g_{\mathrm{m}}}{g_{\mathrm{m3}}}} \tag{18}$$

The 1 − CP depicts the start of distortion when the input power reduces the gain by 1 − dB [37]. The impact of P-ITCs and N-ITCs on the 1 − CP for UTS-F-TFET is shown in Fig. 18b. The value of 1 − CP is decreased in the case of P-ITCs because of low distortion in signal and enhanced value of g_{m} compared to the N-ITCs. P-ITCs lead to enhancement in 1 − CP values, and the opposite impact is shown for N-ITCs.

7 Reliability analysis

This section highlights the device's reliability issues over different ITCs. In this detailed investigation, we observed that the impact of ITCs variation on I_{on} is very low. Another side, I_{ambi} of UTS–TFET device increases with reduced V_{on} for P-ITCs. The $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio drastically deteriorates with P-ITCs, but it will improve with the N-ITCs. The OFF-state analysis is carried out to investigate the T and ITCs on impact I_{ambi} with variation in models. Because the SRH and TAT models are highly dependent on temperature, the proposed device's ambipolar behavior improves with T for P-ITCs. The high-frequency performance parameters are similarly affected by variations in ITCs. With the use of a pie chart, the percentage deviation in analog and RF parameters is investigated and portrayed in Fig. 19a. In the same way, Figure 19b shows the impact on linearity parameters. As a result of a rigorous inspection of the proposed device's ON- and OFF-state, high frequency, and linearity performance, it

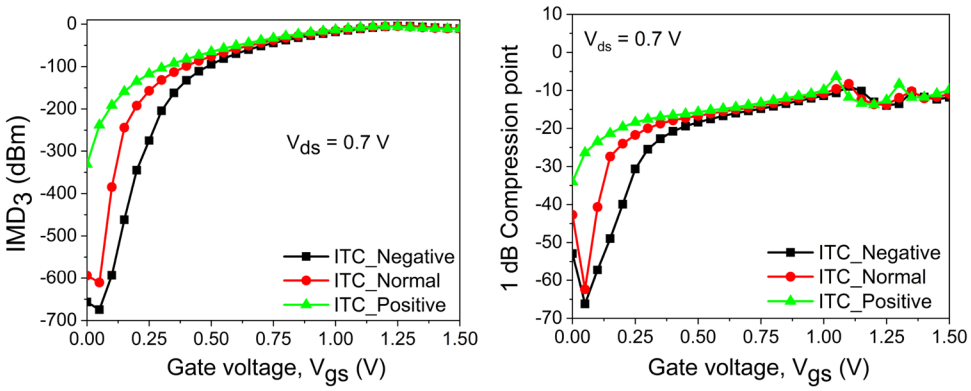

Fig. 18 The data plot of **a** IMD_3 and **b** 1 − CP for different ITCs

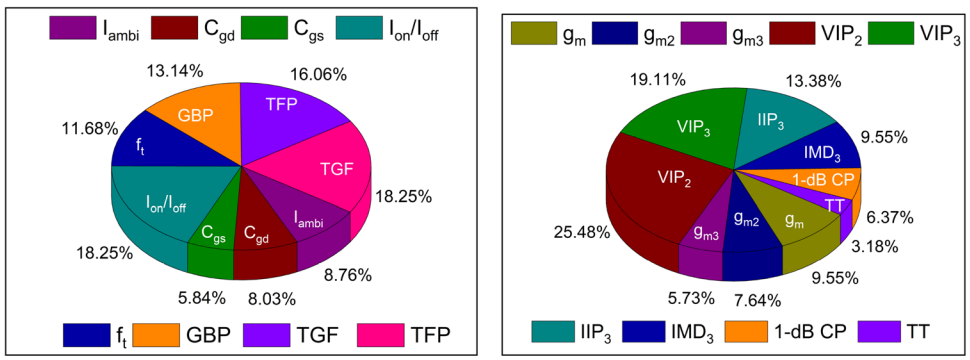

Fig. 19 Deviation in **a** analog/RF and **b** Linearity parameters of UTS-F-TFET for different ITCs

can be assessed that the UTS-F-TFET is much more insusceptible towards the effects of ITCs variation, thus making the device more reliable.

8 Conclusion

In this article, a comparative study is carried out to select the best suited lower bandgap material for the source region to enhance the I_{on} of the proposed device. Along with this, we have investigated the Analog/RF, linearity, and reliability performance of UTS-F-TFET device by examining the impact of P-ITCs and N-ITCs at the silicon/oxide interface. In addition, the impact of temperature on OFF-state current component of UTS-F-TFET is also analyzed with ITCs variation. The comprehensive study shows that the ambipolar conduction significantly increases with temperature and SRH+TAT models for P-ITCs. But g_m and f_t of the proposed device increased with P-ITCs, which indicates that switching speed and bandwidth of the proposed device are enhanced for P-ITCs. The linearity figure of merit g_{m2}, g_{m3} is enhanced for the N-ITCs, but lower value of these parameters is required to maintain the linearity of the device. The linearity and reliability of UTS-F-TFET are improved for the P-ITCs. The minor enhancement/degradation of UTS-F-TFET performance in the presence of P-ITCs/N-ITCs makes it a reliable option for high-frequency, low-power, and distortionless applications.

The manuscript follows all the ethical standards, including plagiarism.

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Declarations

Conflict of interest No conflicts of interest.

Consent for publication We are giving consent to publish.

Consent to participate We are giving consent to participate.

Research involving human participants and/or animals No.

Informed consent Not applicable.

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