Applied Physics A (2021) 127:803
https://doi.org/10.1007/s00339-021-04945-4

Applied Physics A
Materials Science & Processing

Effects of Rapid Thermal Annealing on the Structural, Optical, and Electrical Properties of Au/CuPc/*n*-Si (MPS)-type Schottky Barrier Diodes

P. R. Sekhar Reddy[1,2] · V. Janardhanam[2] · V. Rajagopal Reddy[3] · Min Hyuk Park[1] · Chel-Jong Choi[2]

Received: 27 April 2021 / Accepted: 20 September 2021 / Published online: 1 October 2021

Abstract
The effects of rapid thermal annealing temperature on structural, morphological, and optical properties of copper phthalocyanine (CuPc) films on *n*-Si are investigated. The deposited CuPc films on *n*-Si substrate form nanoparticles and are slightly elongated with an increase in surface roughness with increase in annealing temperature due to the aggregation of the native grains. The electrical and current transport properties of a fabricated Au/CuPc/*n*-Si metal-polymer-semiconductor (MPS)-type Schottky barrier diodes (SBDs) are explored at various annealing temperatures (range 100–300 °C) by current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) measurements. Results reveal that the estimated barrier height decreases with increasing annealing temperature and could be ascribed to the diffusion of Au atoms into CuPc films transferring negative charges to the molecule inducing an n-type doping of the organic film. An analysis of the forward log (*I*)–log (*V*) plot of Au/CuPc/*n*-Si (MPS)-type SBDs indicated the carrier transport domination by ohmic conduction in the lower bias and by the space-charge-limited current (SCLC) transport mechanism at higher bias regions irrespective of annealing temperatures that might be related to additional traps initiating from the CuPc. Poole–Frenkel emission governs the current transport in the reverse bias regardless of annealing temperature.

Keywords Copper phthalocyanine · Surface morphology · Optical band gap · Barrier heights · Series resistance · Current transport mechanism

1 Introduction

During the past decade, there was an emergent interest in the development of molecular material-based Schottky barrier diodes (SBDs) because of the substantiality of SBDs as basis of enormous electronic devices [1–3]. Metal/semiconductor (MS) and metal/polymer/semiconductor (MPS) have fast switching, and low forward voltage drop. Hence, many researchers have focused on enhancing the efficiency and stability of these SBDs by using an interfacial layer, since it performs crucial role in electronic and optoelectronic device technology [4–6]. In recent years, the effort of these investigations is to apply organic (polymer) or metal-blended organic layers at M/S interface, and it converts from MS- to MPS-type SBDs. MPS-type SBDs prepared via the usage of various organic semiconductor, together with polymers and low molecular materials, have received massive significance in terms of its ability for electronic devices [7, 8]. The investigation of MPS-type SBD device configurations open doorways for new functional elements by means of organic or inorganic materials independently.

The advancement in organic electronics has fascinated much interest owing to their advantages of easy device fabrication, low cost, and potential applications in various electronic and optoelectronic devices. There has been much focus on the introduction of organic modification to

✉ V. Rajagopal Reddy
reddy_vrg@rediffmail.com

Chel-Jong Choi
cjchoi@jbnu.ac.kr

[1] School of Material Science and Engineering, College of Engineering, Pusan National University, 2 Busandaehak-ro 63beon-gil, Geumjeong-gu, Busan 46241, Republic of Korea

[2] School of Material Science and Engineering, Semiconductor Physics Research Center (SPRC), Jeonbuk National University, Jeonju 561-756, Republic of Korea

[3] Department of Physics, Sri Venkateswara University, Tirupati 517502, India

semiconductor materials with an ultimate goal to molecularly manipulate the formation and tune the properties of metal–molecule-semiconductor devices [9, 10]. The key issue in employing these organic molecules involves the control of the electronic properties of metal–semiconductor contacts owing to its functional variety and flexibility [11, 12]. The utmost feature of the organic materials is that they can be chemically tuned so as to adjust the band gap, valence and conduction band energies and the charge transport as well as the solubility or other structural properties [13, 14]. Due to its stability and barrier height enhancement properties, organic materials have been employed in electronic devices [15, 16]. On the deposition of a thin organic film intentionally between metal and the inorganic semiconductor substrate, the film modifies some of the properties of the Schottky diodes because the barrier heights can be manipulated by the insertion of a dipole layer between the semiconductor and the organic film [17]. It is believed that the organic–inorganic semiconductor structures could eventually enhances the quality of the fabricated semiconductor devices [18]. The organic film acts as a physical barrier between the metal and the semiconductor, thus preventing the direct contact of the metal with the semiconductor. The organic interlayer seems to cause a substantial variation in the interface states despite the organic–inorganic interface is abrupt and unreactive [19, 20]. Depending on the choice of the organic molecule and interlayer thickness, the semiconductor device can be designed to exhibit desired properties. Modifying the interface electronic states through organic molecules could lead to efficient barrier height modification of the metal/inorganic semiconductor structure [21]. Organic thin layer-based Schottky diodes are superior to conventional Schottky diodes due to their modified contact barriers. Organic compounds can provide a general route for continuous control of the Schottky barrier height at the semiconductor interface.

Phthalocyanine-based organic materials have attracted considerable interest in the last few years in the fabrication of organic based devices. Its chemical and thermal stability and the tendency to form highly ordered layers results in increased device efficiency. The metal phthalocyanine is promising for applications in organic light emitting diodes, photovoltaics, gas sensors, and solar cells [22–26]. Particularly, the semiconducting copper phthalocyanine (CuPc) is employed in a wide variety of optoelectronic devices and as an active channel layer in organic field effect transistors. A few studies have made to characterize the electronic parameters of CuPc-based devices by different research groups [27–30]. For instance, Hassan et al. [27] fabricated the Ag/CuPc/*n*-Si diode and then the samples were annealed at different temperature, reported the leakage current density decreased with increasing annealing temperature under light illumination. Ahmad et al. [28] studied the electrical properties of Au/CuPc/*n*-Si heterojunction at different annealing temperatures in the range of 30–50 °C and reported the leakage current decreased with increasing annealing temperature. Ullah et al. [29] investigated the effect of temperature (ranging from 300 to 330 K) on electronic parameters of Al/CuPc/*n*-Si heterostructure and reported that the electronic parameters were improved at all temperatures. Elgazzar et al. [30] investigated the structural, and optical properties of Au/CuPc/*n*-Si Schottky diode. Although there have been some reports available on the fabrication CuPc/*n*-Si diode structures using various electrodes and its electrical characterization, despite the potential features of the CuPc films as organic semiconductor, the information on the effect of annealing the CuPc films on the electrical properties and the current transport mechanism is still lacking in the literature.

The intention of the present work is to fabricate Au/CuPc/n-Si (MPS)-type SBDs with a CuPc layer in-between the metal and semiconductor by way of thermal evaporation process, and explored its structural, optical, and electrical properties at different annealing temperatures. The current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements of Au/CuPc/*n*-Si (MPS)-type SBDs have been investigated at different annealing temperatures measured at room temperature in the dark. The key parameters of the SBD such as ideality factor, barrier height and series resistance of the Au/CuPc/*n*-Si (MPS)-type SBD had been evaluated and cross-checked by applying different methods through the forward *I–V*, *C–V*, Cheung, and Norde methods for their consistency and validity. Also, the possible forward and reverse leakage current mechanism of Au/CuPc/*n*-Si (MPS)-type SBDs is described and discussed at different annealing temperatures.

2 Experimental details

Metal-polymer-semiconductor (MPS)-type SBDs were prepared on *n*-Si substrate that has 525 μm thickness, (100) orientation and 1–10 Ω. cm resistivity. The *n*-Si substrates were cleaned by way of RCA [31, 32] as followed: (1) First, the *n*-Si substrates were ultrasonically degreased with organic solvents using acetone and methanol sequentially for 10–15 min in each, (2) then the organic residuals were removed from the substrate utilizing piranha solution by mixing H_2SO_4/H_2O_2 in the ratio of 1:1 for 10 min, and (3) the native oxide layer on the Si wafers was removed with the help of HF/H_2O in the ratio of 1:10 for 10 min and then rinsed in DI water followed by dried in N_2 gas flow. After that, high purity aluminum (Al) (99.99%) was deposited with the thickness of 50 nm on the back side of the *n*-Si substrate by thermal evaporation process (at pressure of 10^{-7} Torr) and then annealed at 350 °C for 5 min in N_2 atmosphere in a rapid thermal annealing (RTA) system. 40-nm-thick CuPc films were deposited on the smooth side of cleaned

n-Si substrate with the growth rate of 0.2 ± 0.5 Å/s, that was monitored by a quartz crystal microbalance. Later, 30-nm-thick gold (Au) Schottky electrode was made on the CuPc thin film layer using a metal mask with an area of 500 µm by e-beam evaporation system. Then, the fabricated Au/CuPc/*n*-Si (MPS)-type SBDs were annealed at 100 °C, 200 °C and 300 °C for 1 min in nitrogen atmosphere in an RTA system. During the RTA process, the temperature was ramped up from room temperature to the desired temperature of annealing in 30 s, maintained at that temperature for 1 min, and then cooled down to 100 °C, followed by finally lowering down to room temperature. Figure 1a, b shows the schematic diagram of Au/CuPc/*n*-Si/Al SBD and molecular structure of the copper phthalocyanine (CuPc) film. Atomic force microscopy (AFM) and scanning electron microscopy (SEM) measurements were applied to characterize the surface morphology of CuPc thin films. The optical absorbance measurements were recorded using a JASCO V-570 ultraviolet–visible–near-infrared (UV–Vis–NIR) spectrophotometer. Finally, current–voltage (*I*−*V*) and capacitance−voltage (*C*−*V*) measurements were performed by using a precision semiconductor parameter analyzer (Agilent 4156C) and a precision LCR meter (Agilent 4284A), respectively.

3 Results and discussion

3.1 Structural properties

The surface topography and morphology of the CuPc thin films on *n*-Si substrate are characterized by atomic force microscopy (AFM) and scanning electron microscopy (SEM) before and after annealing at 100 °C, 200 °C and 300 °C, respectively. The SEM images of the CuPc thin films are depicted in Fig. 2. It can be noted that the deposited CuPc films on Si formed dense, uniform nanoparticles and are well adhered to the Si substrate (Fig. 2a). The nanoparticles of the CuPc films exhibited a slight elongation on annealing at 100 °C (Fig. 2b) and remained similar after annealing at 200 °C (Fig. 2c). However, on annealing at 300 °C (Fig. 2d), the nanoparticles showed a much increase in the elongation of the nanoparticles and could be associated with the aggregation of the native grains into larger grains. The images in the inset of Fig. 2 show the stacking of nanoparticles at relatively higher magnification. Figure 3 shows 2D and 3D AFM images of the CuPc films before and after annealing from 100 to 300 °C. Figure 3a clearly shows the formation of nanoparticles with the deposition of CuPc films on Si substrate exhibiting a root-mean-square surface roughness of 2.38 nm. It can be clearly noted that on annealing the CuPc films at 100 °C (Fig. 3b), the size of the CuPc particles increase slightly and the size nearly remained similar on increasing the annealing temperature to 200 and 300 °C (Fig. 3c, d). The RMS surface roughness of the CuPc films deposited on Si substrate increased to 3.46 nm on annealing at 100 °C and later increased to 3.62 and 3.71 nm on rising the annealing temperature to 200 and 300 °C, respectively. The increase in the RMS surface roughness with increasing annealing temperature could be related to the aggregation of the native grains into larger grains/cluster upon annealing.

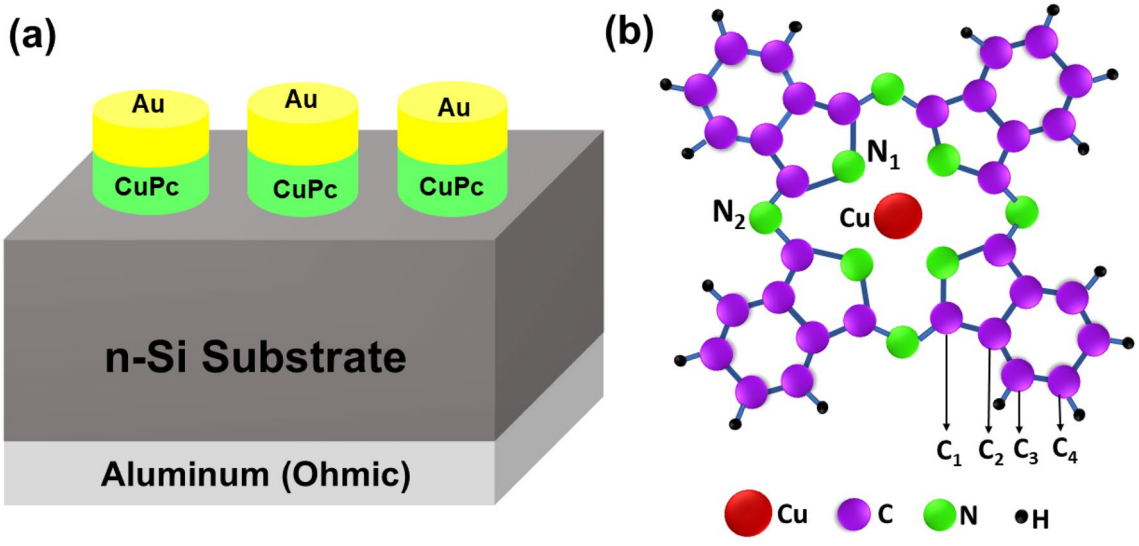

Fig. 1 **a** Schematic diagram of a fabricated Au/CuPc/*n*-Si/Al (MPS) Schottky barrier diode, and **b** Molecular structure of copper phthalocyanine (CuPc)

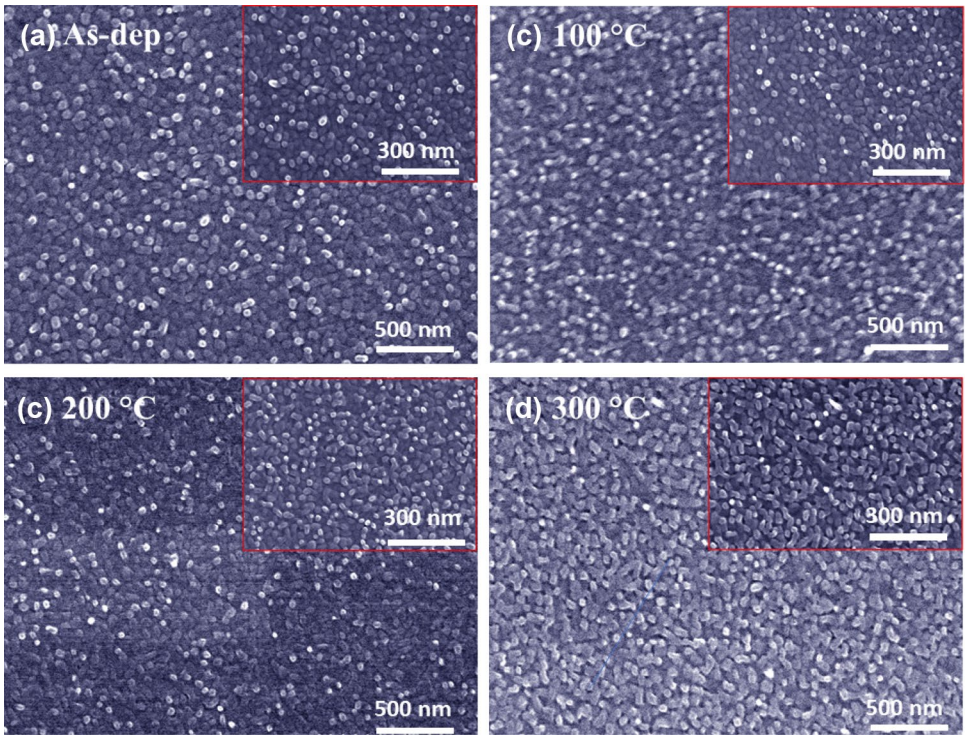

Fig. 2 Scanning electron microscopy (SEM) images of CuPc thin films: **a** as-deposited, **b** 100 °C, **c** 200 °C and **d** 300 °C

3.2 UV–Vis spectroscopy properties

To analyze the optical absorption properties of CuPc thin films, UV–Vis absorption spectroscopy was employed and measured in the range of 300–900 nm. Conceptually, there are five dominating electronic transitions in phthalocyanine compounds absorption spectrum in the range of 1.5–6.2 eV, usually labeled as Q, B, N, L and C, respectively [33, 34]. The UV–VIS spectrum of the phthalocyanines arises from the molecular orbitals within the aromatic 18π electron system and from overlapping orbitals on the central metal atom [33, 35]. Figure 4a depicts the absorption spectrum of the CuPc films before and after annealing from 100 to 300 °C. It is clearly noted that the CuPc films do not exhibit considerable changes in the absorption coefficient with annealing temperature. The absorption spectrum consists of three peaks, a single peak in the low wavelength (300–400 nm) UV region, called the B-band (Soret-band) and doublet peaks in visible region called the Q-band [36, 37]. The B-band is attributed to the transitions from the deeper π-HOMO to π*-LUMO energy levels. The Q-band peaks are associated with the transitions from the π-HOMO to π*-LUMO energy levels consisting of the phthalocyanine ring. The B-band and Q-band peak positions remained unchanged, however, with a slight decrease in the peak intensity with increasing annealing temperature. This behavior could be attributed to the increase in grain size and crystallinity [38, 39]. The optical band gap of the CuPc films was determined from the intercept of the extrapolation of the linear part of $(\alpha h\nu)^2$ versus E plot, where E represents the photon energy ($h\nu$) following the relation $\alpha(h\nu) = A.\ (h\nu\text{-}E_g)^2$ [33]. The terms α is the absorption coefficient, $h\nu$ is the incident photon energy, A is constant, and E_g is optical energy gap of the semiconductor. Figure 4b shows the $(\alpha h\nu)^2$ versus $h\nu$ plot for the CuPc films before and after annealing from 100 to 300 °C. From the plot, the values of optical band gap of the CuPc films is obtained as 3.25 eV (as-deposited), 3.25 eV (at 100 °C), 3.26 (at 200 °C), and 3.27 eV (at 300 °C), respectively. It is noted that the band gap of the CuPc films varied slightly with the annealing temperatures, attributed to the changes in the crystal structure and morphology of CuPc films. The bandgap values obtained were comparable with previously reported values [31, 33]. In addition, the Urbach tail is determined by the following relation $\alpha = \alpha_0 \exp[(h\nu\text{-}E_0)/E_U]$, where α_0 and E_0 are constant, $h\nu$ is the incident photon energy, and E_U is the Urbach energy, which refers to the width of the exponential absorption edge [40, 41]. The Urbach energy can be determined from the reciprocal slope of the curve of ln α versus $h\nu$. Figure 4c shows the plot of ln (α) against the photon energy ($h\nu$) for the as-deposited and annealed samples. The value of E_0 is obtained from the slope of linear region. The value of Urbach energy (E_U) is found to be 0.253 eV (as-deposited), 0.258 eV (at 100 °C), 0.252 eV (at 200 °C) and 0.251 eV (at 300 °C), respectively. Clearly, it is noted that there are no significant changes in the Urbach energy with annealing temperature. Figure 4d shows the plot of ln(α) versus ($h\nu$) for the as-deposited, 100 °C, 200 °C, and 300 °C, respectively. The extrapolations of the

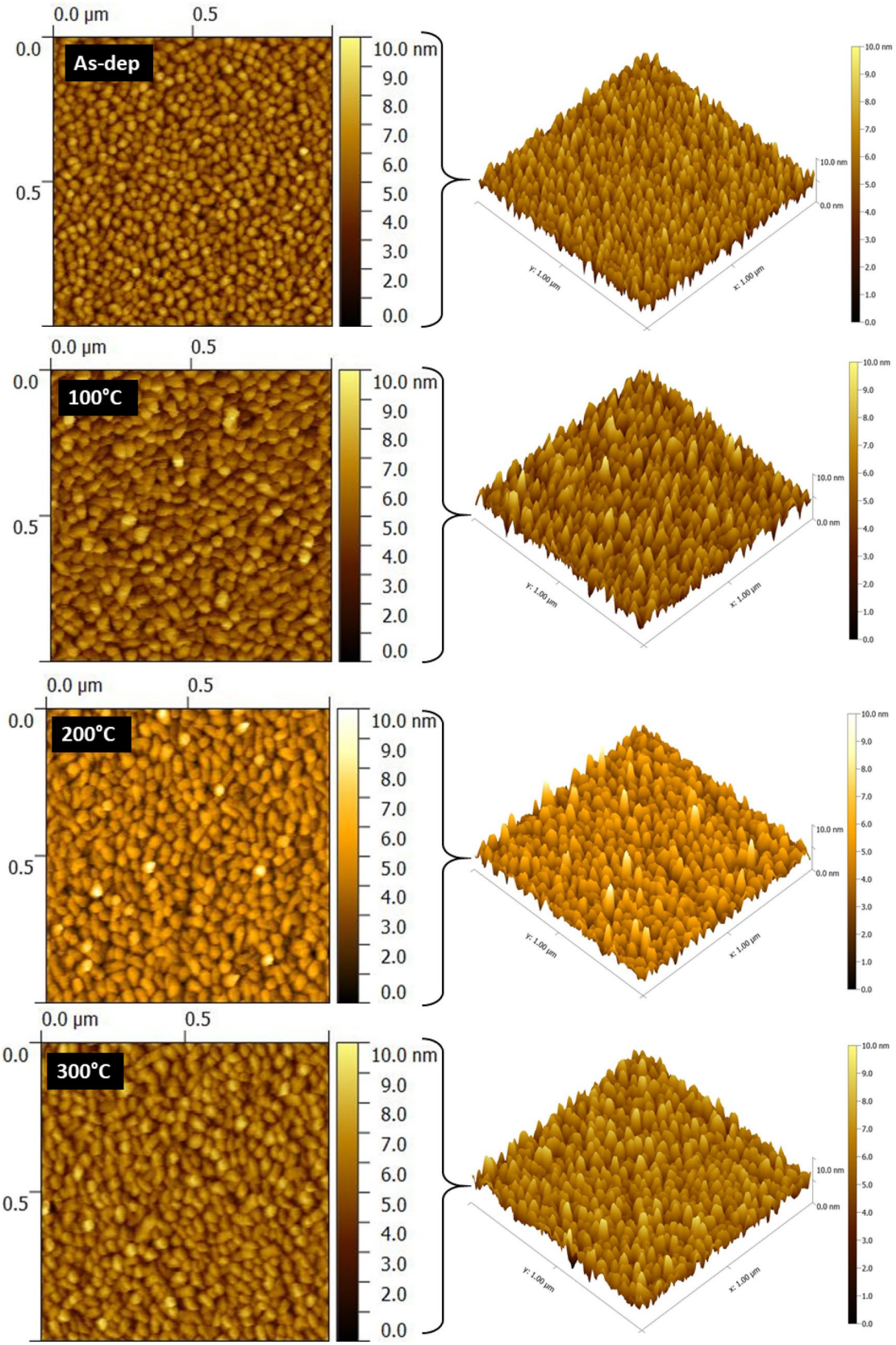

Fig. 3 2D and 3D AFM images of CuPc films on n-type Si: **a** as-deposited, **b** 100 °C, **c** 200 °C and **d** 300 °C

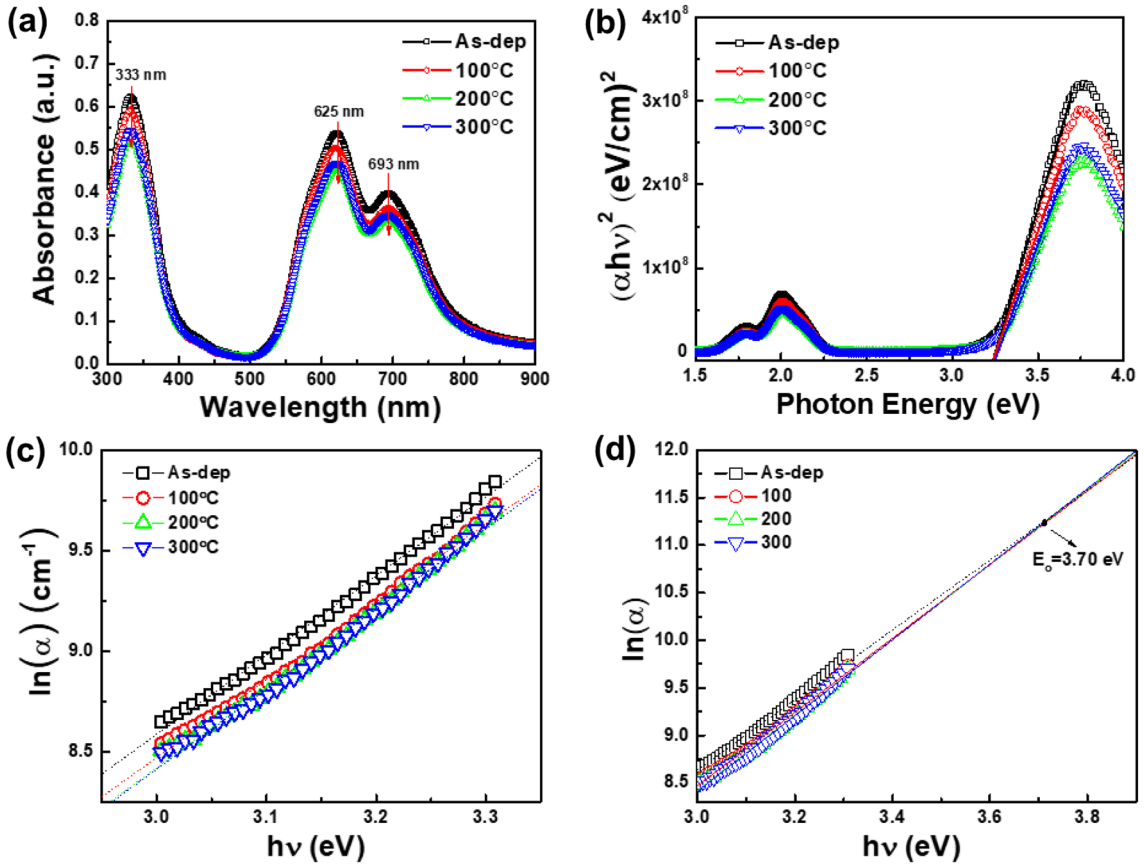

Fig. 4 **a** Optical absorption spectra of CuPc on glass substrates with varying annealing temperature, **b** plot of $(\alpha h\nu)^2$ versus photon energy ($h\nu$) achieved from the optical absorption spectra, **c** Urbach energy plot, and **d** ln(α) versus $h\nu$ for the as-deposited, 100 °C, 200 °C, and 300 °C, respectively

plot converged to a point with the coordinate giving a value of $E_o = 3.70$ eV and $\alpha_o = 4.3 \times 10^3$ cm^{-1}.

3.3 Electrical characterizations

In order to investigate the effect of CuPc layer on electrical characteristics, we fabricated Au/CuPc/*n*-Si (MPS)-type SBDs with a CuPc interlayer between the Au and *n*-Si and explored its electrical properties at different annealing temperatures. Figure 5 shows the semi-logarithmic current–voltage ($I-V$) characteristics of the Au/CuPc/*n*-Si (MPS)-type SBDs as a function of annealing temperature. The fabricated Au/CuPc/*n*-Si (MPS)-type SBDs exhibits an excellent rectification behavior at all annealing temperatures. It was noted that the current increases exponentially in the forward bias and the current shows weak voltage dependence in the reverse bias as a function of annealing temperature. The currents increased with increasing annealing temperature in both the bias associated with the enhancement in electrical conductivity as will also be confirmed from the decrease in series resistance values with increasing annealing temperature that will follow later. This could be due to improvement

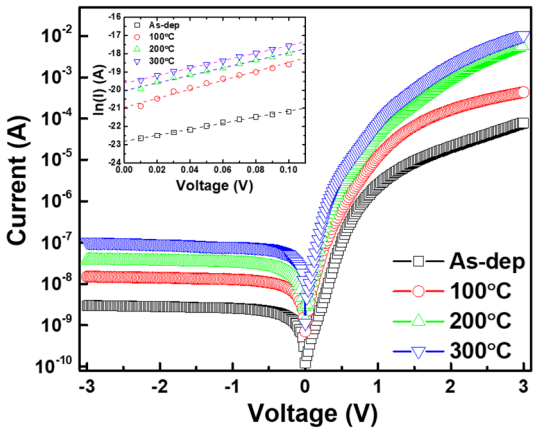

Fig. 5 Current–voltage ($I-V$) characteristics of the Au/CuPc/*n*-Si (MPS) Schottky barrier diodes as a function of annealing temperature

in the grain size and crystallinity as mentioned in the optical properties added with the transformation of the nanoparticles into elongated nanoparticles that provides the path for the carriers to flow easily, thus increasing the charge transfer

rate [42]. The measured reverse leakage current increases with increasing annealing temperature as 2.58×10^{-9} A for the as-deposited and 2.9×10^{-8} A for 100 °C, 3.22×10^{-8} A for 200 °C and 8.32×10^{-8} A at—1 V for 300 °C, respectively. The reverse leakage currents decrease with increasing annealing temperature. The Schottky barrier height (Φ_b) and ideality factor (n) of the Au/CuPc/n-Si SBDs can be determined by way of $I-V$ characteristics based on the thermionic-emission (TE) theory, described elsewhere [43]. Inset of Fig. 5 shows the ln(I) versus V plot for the Au/CuPc/n-Si SBDs before and after annealing temperatures. From this plot, the saturation current (I_o) can be obtained from the straight lines of intercept at zero voltage. The experimental values of Schottky barrier height (Φ_b) and ideality factor (n) for the Au/CuPc/n-Si (MPS)-type SBDs are obtained from y-axis intercept and the slope of the linear region of forward I–V data. The extracted Φ_b and n values are 0.85 eV, 0.83 eV, 0.80 eV, and 0.78 eV and 1.56, 1.43, 1.34 and 1.25, respectively, for the as-deposited, 100 °C, 200 °C and 300 °C. The obtained values are summarized in Table 1 as a function of annealing temperature. Further, a Table 2 showing the comparison of the obtained parameters in the present work with those obtained in previously reported works in the literature. As can be seen from Table 1, the Φ_b and n of the Au/CuPc/n-Si (MPS)-type SBDs significantly decreases with increasing annealing temperature. This decrease in the barrier heights with annealing temperature could be due to the diffusion of the Au atoms inside the CuPc films, transferring negative charges to the molecules, thus inducing an n-type doping of the organic film leading to a shift of the LUMO state toward the Fermi level and hence shift of HOMO level toward higher binding energies [39]. The calculated ideality factor value for the SBDs is greater than one, that may be attributed to the several effects which includes image force effect, barrier inhomogeneity at the interface, and series resistance, non-uniform distribution of interfacial charges. Higher ideality factor can also be due to the recombination-generation currents in the depletion region, tunneling and recombination via the interface states [46, 47].

Table 1 The extracted electrical parameters of Au/CuPc/n-type Si Schottky barrier diodes with different annealing temperatures

Parameter	As-deposited	100 °C	200 °C	300 °C
From I–V characteristics				
Barrier height, Φ_b (eV)	0.85	0.83	0.80	0.78
Ideality factor, n	1.56	1.43	1.34	1.25
From Cheung's method				
dV/d(ln$I$) versus I				
Series resistance, R_S (kΩ)	41.16	3.97	2.98	1.40
Ideality factor, n	6.58	5.61	5.03	4.64
H(I) versus I				
Series resistance, R_S (kΩ)	40.63	4.13	2.96	1.42
Barrier height, Φ_b (eV)	0.73	0.71	0.69	0.68
From Norde's method				
Series resistance, R_S (MΩ)	142.22	20.51	5.36	2.33
Barrier height, Φ_b (eV)	0.83	0.80	0.77	0.76
From C-V characteristics				
Barrier height, Φ_b (eV)	1.21	1.18	1.16	1.13

Table 2 Comparison of various determined Schottky barrier diode parameters with those reported in the literature

CuPc deposition technique	Device structure fabricated	n	Φ_b (eV)	Rs (Ω)	Temperature (K)	Remarks	Ref.
Spin coating	Ag/n-Si/CuPc/Ag solar cell	–	–	–	323–573 (annealing)	CuPc films annealed at 373 K exhibited best photovoltaic behavior	[27]
Thermal evaporation	Au/CuPc/n-Si/Au	–	–	–	300–320 (annealing)	Applicable as humidity and temperature sensor	[28]
Thermal evaporation	Al/CuPc/n-Si	13.4–6.02	0.80–0.96	2.69–1.93 M	300–330	–	[29]
Spin coating	Al/CuPc/n-Si/Al	3.91	0.59	2460	300	Exhibited photodiode behavior	[30]
Thermal evaporation	Al/CuPc/n-Si/ Al	10–8.4	0.73–0.94	–	288–373	–	[44]
Thermal evaporation	Ag/CuPc/Au	85	1.1	1.49 M	300	–	[45]
Thermal evaporation	Au/CuPc/n-Si/Al	1.56–1.25 at 300 K	0.85–0.78at 300 K	40.6–1.42 K at 300 K	373–573	–	This work

Moreover, the Au/CuPc/*n*-Si (MPS)-type SBDs reveal the nonlinear current–voltage behavior at higher forward voltages, which may be because of the impact of series resistance (R_S) and the presence of an interfacial layer. Consequently, the R_S, and other diode parameters which include ideality factor (n) and barrier height (Φ_b) can be determined by using a method developed by Cheung and Cheung [48]. Figure 6a, b shows the plots of dV/d(ln I) and H(I) versus I for the Au/CuPc/*n*-Si (MPS)-type SBDs as a function of annealing temperature. The n and R_S values are determined from the dV/d(ln I) versus I plot (Fig. 6a), and the values are 6.58, 5.61, 5.03 and 4.64, and 41.16 kΩ, 3.97 kΩ, 2.98 kΩ and 1.40 kΩ for the as-deposited, 100 °C, 200 °C and 300 °C, respectively. The Φ_b and R_S values are estimated from the H(I) versus I plot (Fig. 6b) and the respective values are 0.73 eV, 0.71 eV, 0.69 eV, and 0.68 eV, and 40.63 kΩ, 4.13 kΩ, 2.96 kΩ, and 1.42 kΩ for the as-deposited, 100 °C, 200 °C, and 300 °C, respectively. The estimated values are given in Table 1. The R_S values determined from the plot of dV/d(ln I) versus I are very close to those obtained from the H(I) versus I plot, implying their consistency and validity. As can be seen from Table 1, there is a quite a large difference between the ideality factor values determined from the linear forward bias ln(I)–V and nonlinear region of forward bias I–V, which could be ascribed to R_S and interface states, and the bias dependence of the Φ_b caused by the voltage drop across the interfacial layer [49]. The values of ideality factor obtained from the downward curvature regions of the forward bias I–V plots in the Cheung's method are higher than those obtained from the linear regions of the same I–V characteristics using TE theory. This can be ascribed to the existence of effects such as series resistance and the bias dependence of Schottky barrier height caused by the voltage drop across the interfacial layer and change of the interface states with the bias in the low-voltage region of the current–voltage plot. Moreover, it is noted that there may be distinction in the Φ_b determined by forward bias ln (I) –V and Cheung's methods that is probably attributed to the extraction from different regions of the forward bias I–V plot.

Also, the R_S and Φ_b of the Au/CuPc/*n*-Si (MPS)-type SBDs are extracted by using modified Norde's function [50]. Figure 7 shows the $F(V)$ versus V plot for the Au/CuPc/*n*-Si (MPS)-type SBDs at different annealing temperatures. From the Norde's plot, the Φ_b and R_S values are determined to be 0.83 eV, 0.80 eV, 0.77 eV, and 0.76 eV, and 142.22 MΩ, 20.51 MΩ, 5.36 MΩ, and 2.33 MΩ for the as-deposited, 100 °C, 200 °C, and 300 °C respectively, and the values are shown in Table 1. The Φ_b and R_S values determined from the Norde functions are rather different with those acquired from the Cheung's methods, which could be related to a deviation of the $I-V$ characteristics from the ideal TE mechanism. Further, Norde's functions may not be appropriate approach for the SBDs with a high ideality factor that are not compatible with pure TE theory. Therefore, the R_S extracted from the Norde's functions is much higher than those extracted from the Cheung's functions. On the whole, it is clear that the series resistance values decreased with increasing annealing temperature. This decrease in series resistance could be due to the n-type doping of the organic film associated with the

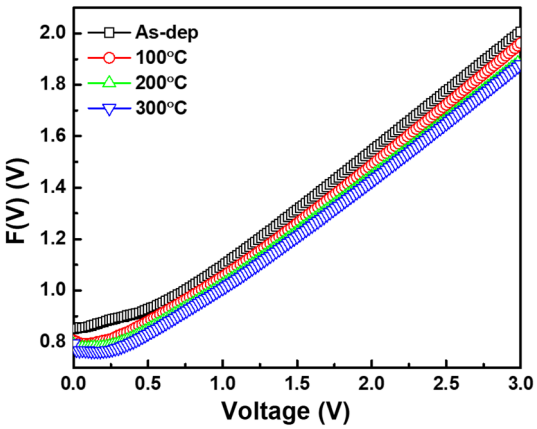

Fig. 7 $F(V)$ versus V plot of Au/CuPc/*n*-Si (MPS) Schottky barrier diode as a function of annealing temperature

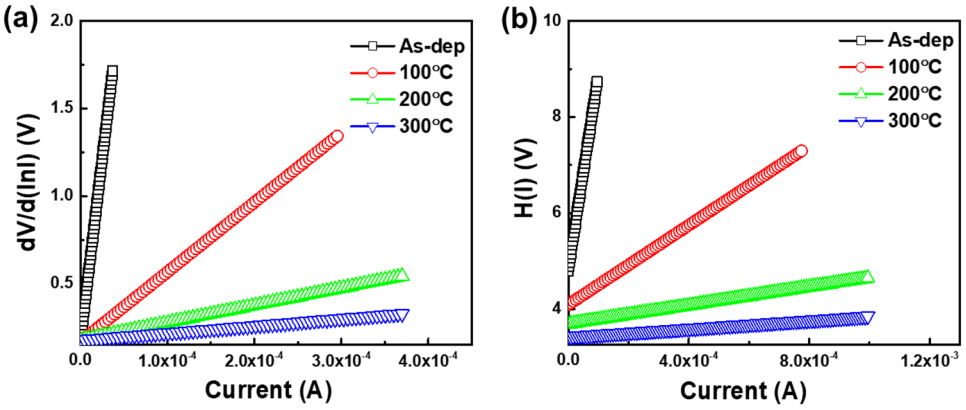

Fig. 6 **a** Plot of dV/d(ln$I$) versus I and H(I) versus I of the Au/CuPc/*n*-Si (MPS) Schottky barrier diode as a function of annealing temperature

diffusion of Au atoms in CuPc films transferring negative charges to the molecules and as well to the improvement in grain size and crystallinity [39].

Figure 8a shows the forward and reverse bias *C–V* characteristics of as-deposited and 100 °C-, 200 °C-, and 300 °C-annealed Au/CuPc/*n*-Si SBDs measured at 1 MHz. It is noticed that the capacitance of Au/CuPc/*n*-Si SBDs decreases gradually with increasing annealing temperature. Particularly, it can be noted that the capacitance is strongly dependent on annealing temperature. Further, it is noticed that the capacitance of Au/CuPc/*n*-Si (MPS) SBDs decreases gradually with increasing annealing temperature. Particularly, it can be noted that the capacitance is strongly dependent on annealing temperature. Capacitance values of all the fabricated Au/CuPc/*n*-Si (MPS) SBDs exhibit peak around ~ 1.2 V to 1.4 V. After this value, it decreases with increasing voltage thus having a concave curvature in the *C–V* plots in the accumulation region due to the effect of series resistance and the interfacial layer. Particularly, surface states are dominant in the depletion and inversion regions, while series resistance and the interfacial layer are only dominant in the accumulation region [43, 51–53]. Figure 8b shows the plot of reverse bias $1/C^2$–*V* characteristics of Au/CuPc/*n*-Si (MPS)-type SBDs before and after annealing at 100 °C, 200 °C, and 300 °C. Based on the relation between capacitance and voltage following the Schottky–Mott model [54, 55], the donor concentration, built-in potential and barrier height of the Au/CuPc/*n*-Si (MPS)-type SBD are estimated to be 5.42×10^{14} cm^{-3}, 5.52×10^{14} cm^{-3}, 5.85×10^{14} cm^{-3} and 5.94×10^{14} cm^{-3} and 0.92 V, 0.89 V, 0.87 V and 0.85 V for the as-deposited, 100 °C, 200 °C and 300 °C, respectively. The estimated barrier height (Φ_b) values are 1.21 eV (as-deposited), 1.18 eV (at 100 °C), 1.16 eV (at 200 °C) and 1.13 eV (at 300 °C), respectively, and are given in Table 1 at different annealing temperatures. As can be seen from Table 1, the barrier heights extracted from the *C–V* method being greater than those extracted from the *I–V* method. This discrepancy in the barrier heights extracted from the *I–V* and *C–V* methods is due to the spatial inhomogeneous barriers, image force lowering and presence of interface states at the junction. Other reasons may be due to surface contamination at the interface, insulating layer, barrier inhomogeneity, edge leakage currents and deep impurity levels [43]. The barrier inhomogeneities that consists of low and high barrier patches mostly affect the *I–V* data and that the current chooses to flow via the low barrier height patches ensuing a lower barrier height. However, the capacitance of the SBDs relies upon the mean value of the barrier height distribution [56].

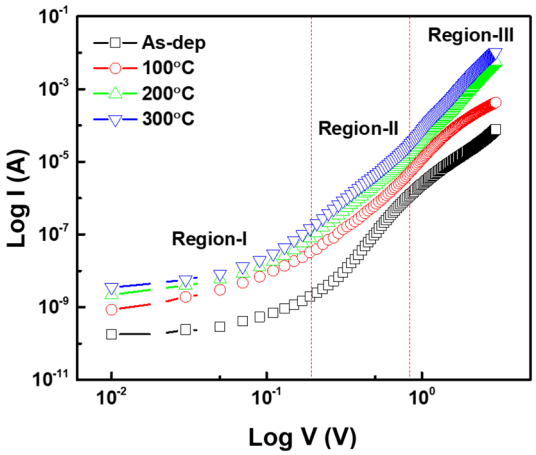

Fig. 9 Forward Log (*I*)−log (*V*) characteristics of the Au/CuPc/*n*-Si (MPS) Schottky barrier diode as a function of annealing temperature

In order to analyze the forward current transport mechanism via the Au/CuPc/*n*-Si (MPS)-type SBDs, the log (*I*)- log (*V*) plot was drawn at different annealing temperatures and is shown in Fig. 9. The plot of log (*I*)- log (*V*) for the as-deposited and 100 °C-, 200 °C-, and 300 °C-annealed Au/CuPc/*n*-Si

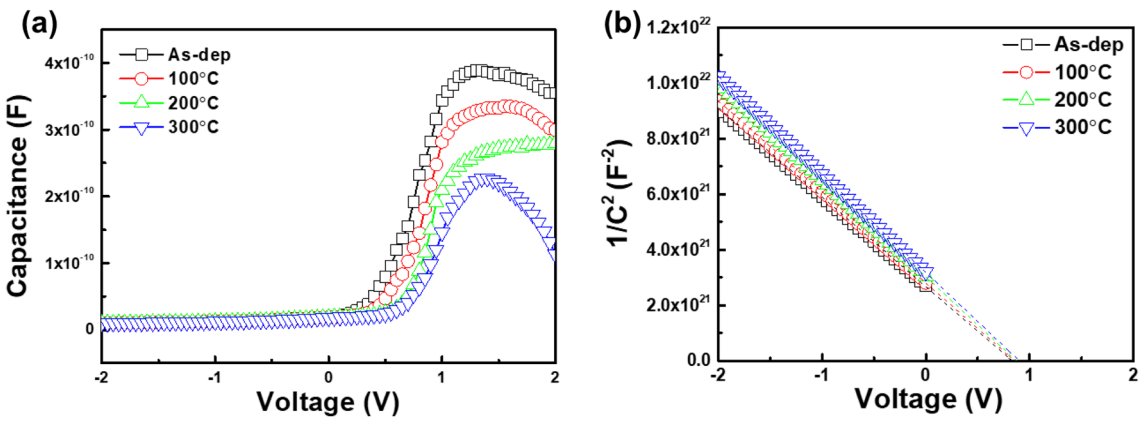

Fig. 8 **a** Capacitance–voltage (*C*−*V*) and **b** $1/C^2$−*V* plot of the Au/CuPc/*n*-Si (MPS) Schottky barrier diode as a function of annealing temperature

(MPS)-type SBDs shows the existence of three distinct linear regions which are labeled as region-I, region-II, and region-III with different power-law exponents of the equation $I \alpha V^m$; here the value of exponent m can be determined from the slope of the linear fit to the log (I) log (V) plot. In region-I, region-II and region-III, the slope values are obtained to be 1.12, 4.30 and 3.04 for as-deposited, 1.14, 3.56 and 3.01 for 100 °C, 1.17, 3.34 and 4.56 for 200 °C, and 1.14, 3.45 and 4.60 for 300 °C, respectively. In region-I, the values are close to unity indicating a linear dependence of the current as I–V. This implies that the current transport at low voltages follow ohm's law, governed by the background doping and by the thermally generated carriers that are predominant over the injected charge carrier [57, 58]. In intermediate stage, the current increases exponentially that is clearly observed in region-II. The slope values are > 2 in the region-II represent that the current transport mechanism could be dominated by space-charge-limited current (SCLC). On the other hand, the voltages becoming most significant than the region-I, and the density of injections free charge is much higher than the thermally generate free charge carrier density [55, 57]. At higher bias region, the slope values are tending to decrease or increase that specifies the device approaches the trap-filled limit current (TCLC), while the injection level is high, whose dependence is the same as in the trap-free SCLC [59–61].

As can be seen from Fig. 5, the as-deposited and annealed Au/CuPc/n-Si (MPS)-type SBDs exhibits the exponential dependence of reverse leakage current (I_R) on applied reverse voltage (V_R), which indicates that Poole–Frenkel emission (PFE) and Schottky emission (SE) mechanism was operative in the junction. In other words, the ln(I_R) versus $V_R^{1/2}$ plot (Fig. 10) for the as-deposited and annealed Au/CuPc/n-Si (MPS)-type SBDs demonstrates a linear variation irrespective of annealing temperature, which leads to expect the reverse current being occupied by PFE or SE for the junction. The reverse current due to PFE is described by [62, 63]

$$I_R = I_o \exp\left(\frac{\beta_{PF} V^{1/2}}{kTd^{1/2}}\right) \quad (1)$$

and the Schottky emission is defined as

$$I_R = AA^*T^2 \exp\left(-\frac{\Phi_b}{kT}\right) \exp\left(\frac{\beta_{SC} V^{1/2}}{kTd^{1/2}}\right) \quad (2)$$

here β_{PF} and β_{SC} are the Poole–Frenkel and Schottky field lowering coefficients, respectively.

The theoretical values for β_{PF} and β_{SC} are designated by

$$2\beta_{SC} = \beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon_r}\right)^{1/2} \quad (3)$$

where q, ε_r and ε_0 are the electric charge, relative permittivity of the semiconductor and the free space. Always, the β_{PF} value is twice the values of the β_{SC}. The estimated theoretical values for PFE and SE are 9.53×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ and 4.77×10^{-5} eV m$^{1/2}$ V$^{-1/2}$. The experimental values extracted from the slope of the linear fitting of the ln (I_R) versus $V_R^{1/2}$ plot, and the corresponding values are 6.63×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ for the as-deposited, 5.15×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ for 100 °C, 2.49×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ 200 °C, and 2.10×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ 300 °C, respectively. The experimental values are well matched with the theoretical values of PFE, suggesting that the reverse current is dominated by the PFE irrespective of annealing temperature, in which the carrier transport occurred from the metal into conductive dislocations through trap states before direct emission from the metal [64, 65].

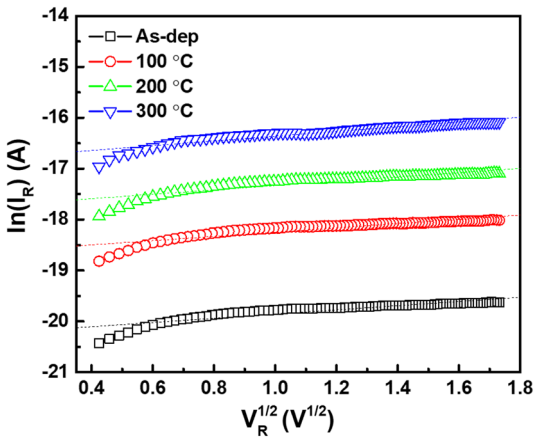

Fig. 10 ln($I^{1/2}_R$) versus $V^{1/2}_R$ plot of the Au/CuPc/n-Si (MPS) Schottky barrier diode as a function of annealing temperature

4 Conclusions

We explored the surface morphological and optical properties of thermally evaporated copper phthalocyanine (CuPc) films on n-Si substrate as a function of annealing temperature by atomic surface morphology (AFM), scanning electron microscopy (SEM), and UV–Vis–NIR spectroscopy approaches. The surface properties indicated that the deposited CuPc films form nanoparticles followed by an increase in surface roughness with increasing annealing temperature and could be associated with the aggregation of native grains into clusters. The CuPc film is highly transparent, and the optical band gap is slightly varied with increasing annealing temperature. The Au/CuPc/n-Si MPS-type Schottky barrier diodes (SBDs) were fabricated using Au as Schottky electrode, and its electrical and current transport properties were studied at different annealing temperatures by I–V and C–V approaches. The barrier heights and series resistance of the SBDs decreases with increasing annealing temperature and

could be due to the diffusion of Au atoms into CuPc films transferring negative charges to the molecules, thus inducing an n-type doping of the organic film. An analysis of the forward *I–V* characteristics demonstrates the domination of the current transport mechanism by ohmic conduction at low-bias and space-charge-limited conduction (SCLC) mechanisms at higher bias regardless of the annealing temperature. Poole–Frenkel emission mechanism dominates the reverse leakage current in Au/CuPc/*n*-Si (MPS)-type SBDs in the as-deposited and annealed SBDs. The results obtained in this study indicate the suitability of CuPc films in the fabrication of high-performance organic–inorganic heterojunction devices.

Acknowledgements This work was supported by the National Research Foundation of Korea (NRF) Grant (NRF-2017R1A2B2003365) funded by the Ministry of Education, Republic of Korea, and by Korea Evaluation Institute of Industrial Technology (KEIT) Grant (Project No. 20004314) funded by the Ministry of Trade, Industry & Energy, Republic of Korea. This study was also financially supported by the 2020 Post-Doc. Development Program of Pusan National University, Republic of Korea.

References

1. B. SH Barkhalov, YU.A. Vidadi, Thin Solid Films **40** (1977)
2. R.K. Gupta, R.A. Singh, Compos. Sci. Techn. **65**, 677 (2005)
3. A.K Hassan, R.D. Gould, J. Phys. D: Appl. Phys. **22** (1989)
4. Y. Osada, A. Mizumoto, J. Appl. Phys. **59**, 1 (1986)
5. K. Kudo, T Sumimoto, K Hiraga, S Kuniyoshi, K. Tanaka, Jpn. J. Appl. Phys. **36** (1997)
6. F. Yakuphanoglu, Solar Energy Mater. Solar Cells **91** (2007)
7. V. Bobnar, A. Levstik, Phys. Rev. B, **71** (2005)
8. R.D. Gould, A.K. Hassan, Thin Solid Films **223** (1993)
9. Y.J. Liu, H.Z. Yu, J. Phys. Chem. B **107**, 7803 (2003)
10. T.V. Basova, R.G. Parkhomenko, M. Polyakov, A.G Gurek, D. Atilla, F. Yuksel, E.I. Ryabchikova, B.Y. Kadem, A.K. Hassan, Dyes Pigments **125** (2016)
11. H. Haick, M. Ambrico, T. Ligonzo, R.T. Tung, D. Cahen, J. Am. Chem. Soc. **128**, 6854 (2006)
12. M. Zhang, C. Shao, Z. Guo, Z. Zhang, J. Mu, T. Cao, Y. Liu, ACS Appl. Mater. Interfaces **3** (2011)
13. C. Tang, S. VanSlyke, Appl. Phys. Lett. **51** (1987)
14. G.A. Chamberlain, P.J. Cooney, Chem. Phys. Lett. **66** (1979)
15. C.S. Kuo, F.G. Wakim, S.K. Sengupta, S.K. Tripathy, Jpn. J. Appl. Phys. **33** (1994)
16. R. Gupta, S.C.K. Misra, B.D. Malhotra, N.N. Beladakere, S. Chandra, Appl. Phys. Lett. **58** (1991)
17. Z. Caldiran, A.R. Deniz, S. Aydogan, A. yesildag, D. Ekinci, Superlattice Microstruct. **56** (2013)
18. P.R.S. Reddy, V. Janardhanam, I. Jyothi, C.S. Harsha, V. Rajagopal Reddy, S.N Lee, J. Won, C.J. Choi, Appl. Phys. A **124** (2018)
19. T. Kampen, A. Schuller, D.R.T. Zahn, B. Biel, J. Ortega, R. Perez, F. Flores, Appl. Surf. Sci. **234**, 341 (2004)
20. M. Cakar, N. Yildirim, S. Karatas, C. Temirci, A. Turut, J. Appl. Phys. **100** (2006)
21. S. Okur, F. Yakuphanoglu, M. Ozsoz, P.K. Kadayifcilar, Microelectron. Eng. **86** (2009)
22. S.-F. Chen, C.-W. Wang, Appl. Phys. Lett. **85**, 765 (2004)
23. T. Kudo, M. Kimura, K. Hanabusa, H. Shirai, T. Sakaguchi, J. Porphyr, Phthalocyanin **3**, 65 (1999)
24. I. Kim, G.E. Jabbour, Synth. Met. **162**, 102 (2012)
25. H. Bentin, N. Kudo, H. Ohkita, S. Ito, Thin Solid Films **517**, 6 (2009)
26. A.A.A. Darwish, S.R. Alharbi, M.M Hawamdeh, A. M Alsharari, S.I Qashou, J. Electron. Mater. **49** (2020)
27. H. Hassan, N.B. yah Ibrahim, Z. Ibarahim, Sains Malaysiana. **39**, 627 (2010)
28. Z. Ahmad, M.H. Sayyad, K.S. Karimov, J. Semicond. **31**, 074002 (2010)
29. I. Ullah, M. Shah, Shaukat Ali Khattak, and Gulzar Khan. J. Electron. Mater. **48**, 5609 (2019)
30. E. Elgazzar, Mater. Res. Express **7**, 095102 (2020).
31. A.A. Kumar, V. Rajagopal Reddy, V. Janardhanam, M.-W. Seo, H. Hong, K.-S. Shin, C.-J. Choi, J. Electrochem. Soc. **159**, H33 (2011)
32. H.A. Çetinkara, M. Sağlam, A. Türüt, N. Yalçin, Eur. Phys. J. Appl. Phys. **6**, 84 (1999)
33. M.E. Azim-Araghi, R. Sahebi, Phys. B Condens. Matter **433**, 165 (2014)
34. S.S Mali, D.S. Dalavi, P.N. Bhosale, C.A. Betty, A.K. Chauhan, P.S. Patil, RSC Adv. **2** (2012)
35. M. Yoneyama, M. Sugi, M. Saito, K. Ikegami, S. Kuroda, S. Iizima, Jpn. Appl. Phys. **25**, 961 (1986)
36. R. Koshy, C.S. Menon, E-Journal Chem. **9**, 294 (2012)
37. S. Karan, B. Mallik, J. Phys. Chem. C **111**, 7352 (2007)
38. S.R. Forrest, M.L. Kaplan, P.H. Schmidt, W.L. Feldmann, E. Yanowski, Appl. Phys. Lett. **41**, 90 (1982)
39. L. Lozzi, S. Santucci, J. Chem. Phys. **134** (2011)
40. F. Yakuphanoglu, S. Ilican, M. Caglar, Y. Caglar, J. Optoelectron. Adv. Mater. **9**, 2180 (2007)
41. E. Feizi, A.K. Ray, J. Mater. Sci. Mater. Electron. **26**, 4691 (2015)
42. N.S. Kumar, S.K. Naveen Kumar, L.Yesappa, Mater. Res. Express **7**, 015071 (2020)
43. E.H. Rhoderick, R.H. Williams, *Metal-Semiconductor Contacts*, 2nd edn. (Clarendon press, Oxford, 1988), p. 33
44. R. Kumar, R. Kaur, M. Sharma, M. Kaur, S.K. Tripathi, AIP Conf. Proc. (2015)
45. M. Shah, M.H. Sayyad, Kh.S. Karimov, J. Semicond. **7**, 31 (2010)
46. R.T. Tung, Electron transport at metal-semiconductor interfaces: general theory, Phys. Rev. B. (1992)
47. S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, 3rd ed. (2006)
48. S.K. Cheung, N.W. Cheung, Appl. Phys. Lett. **49**, 85 (1986)
49. A. Tataroğlu, Ş. Altındal, Y. Azizian-Kalandaragh, Phys. B: Condens Matter, **576** (2020)
50. H. Norde, J. Appl. Phys. **50**, 5052 (1979)
51. S.M. Sze, *Physics of Semiconductor Devices*, 2nd edn. (Wiley, New York, 1981)
52. E.H. Nicollian, J.R. Brews, *Metal Oxide Semiconductor (MOS) Physics and Technology*, 2nd edn. (Wiley, New York, 1982)
53. E.H. Nicollian, A. Goetzberger, Bell Syst. Tech. J. **46** (1967)
54. H.G. Çetinkay, M.Yıldırım, P. Durmus, S. Altındal, J. Alloys Compd. **721** (2007)
55. V. Rajagopal Reddy, P.R.S. Reddy, I.N. Reddy, C.J. Choi, RSC Adv. **6** 105760 (2016)
56. J.F Matoko-Ngouma, B.R. Malonda-Boungou, A.T. Raji, P.S. Moussounda, B.Mpassi-Mabiala, J. Mol. Struct. **1211** (2020)
57. M.E. Aydin, A. Türüt, Microelectron. Eng. **84**, 2875 (2007)
58. K.H.S. Karimov, I. Qazi, S.A. Moiz, I. Murtaza, Optoelectron. Adv. Mater. Rapid Commun. **2**, 4 (2008)
59. S.M. El-Sayed, H.M. Abdel Hamid, R.M. Radwan, Radiat. Phys. Chem. **69**, 339 (2004)
60. S.R. Forrest, Chem. Rev. **97**, 1793 (1997)

61. A. Tataroglu, A. Buyukbas Ulusan, Ş. Altındal, Y. Azizian-Kalandaragh, J. Inorg. Organomet. Polym. Matt. **31** (2021)
62. T.G Abdel-Malik, Organic Photovoltaics, **5520** (2004)
63. Ç. Ş. Güçlü, A. F. Özdemir, D. A. Aldemir, Ş. Altındal, J. Mater. Sci. Mater. Electron. **32** (2021)
64. S. Altındal Yerişkin, J Mater Sci: Mater Electron. **30** (2019)
65. A. Buyukbas-Ulusan, S. Altındal-Yerişkin, A. Tataroğlu, J. Mater. Sci. Mater. Electron. **29** (2018)